CONFIGURABLE LOGIC

PLD • FPGA • GATE ARRAY

DATA BOOK

ATMEL

Atmel Programmable Logic Devices (PLDs)

PLDs	Pins	V_{cc}	Technology	tpd	I_{cc}(mA)	Page
AT22V10-	24	5	UV CMOS	25,30	55	1-109
AT22V10-	24	5	UV CMOS	15,20	90	1-109
AT22V10B-	24	5	UV CMOS	7.5,10	140	1-109
AT22V10L-	24	5	UV CMOS	20,25,30	12	1-97
AT22LV10-	24	3	UV CMOS	20,25	35	1-119
AT22LV10L-	24	3	UV CMOS	25,30	4	1-119
ATF22V10B-	24	5	EE CMOS	7.5,10,15,25	120	1-65
ATF22V10BL-	24	5	EE CMOS	15	10	1-65
ATF22V10BQ-	24	5	EE CMOS	15	55	1-65
ATF22V10BQL-	24	5	EE CMOS	25	12	1-65
ATF22V10C-	24	5	EE CMOS	5,7.5	120	1-77
ATF22V10CZ-	24	5	EE CMOS	10,15	0.01	1-81
ATF22LV10C-	24	3	EE CMOS	10,15	35	1-79
ATF22LV10CZ-	24	3	EE CMOS	15,25	0.01	1-83
ATF16V8B-	20	5	EE CMOS	7.5,10,15,25	120	1-3
ATF16V8BQ-	20	5	EE CMOS	10	55	1-3
ATF16V8BQL-	20	5	EE CMOS	15,25	12	1-3
ATF16V8C-	20	5	EE CMOS	5,7.5	115	1-23
ATF16V8CZ-	20	5	EE CMOS	10,15	0.01	1-37
ATF16LV8C-	20	3	EE CMOS	10,15	30	1-35
ATF16LV8CZ-	20	3	EE CMOS	15,25	0.01	1-39
ATF20V8B-	20	5	EE CMOS	7.5,10,15,25	120	1-41
ATF20V8BQ-	20	5	EE CMOS	10	55	1-41
ATF20V8BQL-	20	5	EE CMOS	15,25	12	1-41
ATF20V8C-	24	5	EE CMOS	5,7.5	115	1-57
ATF20V8CZ-	24	5	EE CMOS	10,15	0.01	1-61
ATF20LV8C-	24	3	EE CMOS	10,15	30	1-59
ATF20LV8CZ-	24	3	EE CMOS	15,25	0.01	1-63
ATV750-	24	5	UV CMOS	20,25	120	1-143
ATV750L-	24	5	UV CMOS	25	12	1-131
ATV750B-	24	5	UV CMOS	7.5,10,15,25	180	1-143
ATV750BL-	24	5	UV CMOS	15,25	4	1-143
ATV750BQ-	24	5	UV CMOS	10	90	1-143
ATV750BQL-	24	5	UV CMOS	15,25	4	1-143
ATLV750B-	24	3	UV CMOS	15	45	1-159
ATLV750BL-	24	3	UV CMOS	25	2	1-159
ATF1500	44	5	EE CMOS	7.5,10,12,15	70	1-85
ATF1500L-	44	5	EE CMOS	15,25	3	1-85
ATV2500H-	40	5	UV CMOS	25,30,35	160	1-161
ATV2500L-	40	5	UV CMOS	30,35	5	1-161
ATV2500B-	40	5	UV CMOS	12,15	160	1-175
ATV2500BL-	40	5	UV CMOS	20	2	1-175
ATV2500BQ-	40	5	UV CMOS	20,25	90	1-175
ATV2500BQL-	40	5	UV CMOS	25,30	2	1-175
ATLV2500B-	40	3	UV CMOS	20	110	1-191
ATLV2500BL-	40	3	UV CMOS	25	1	1-191
ATV5000-	68	5	UV CMOS	25,30,35	350	1-193
ATV5000L-	68	5	UV CMOS	30,35	40	1-193
ATV5100-	68	5	UV CMOS	25,30,35	350	1-207
ATV5100L-	68	5	UV CMOS	30,35	40	1-207

Atmel Field Programmable Gate Arrays (FPGAs)

FPGAs	Usable Gates	V_{cc}	Registers	I/O	F_{max}	Page
AT6002	2000-4000	5	1024	96	250 MHz	2-3
AT6003	3000-6000	5	1600	120	250 MHz	2-3
AT6005	5000-10000	5	3136	108	250 MHz	2-3
AT6010	10000-20000	5	6400	204	250 MHz	2-3

See inside back cover for an index to Atmel CMOS gate arrays.

Atmel Corporation

Configurable Logic Design and Application Book August 1995

PLD • FPGA • Gate Array

Important Notice

Atmel guarantees that its circuits will be free from defects of material and workmanship under normal use and service, and that these circuits will perform to current specifications in accordance with, and subject to, the Company's standard warranty which is detailed in Atmel's Purchasing Order Acknowledgment.

Atmel reserves the right to change devices or specifications detailed in this data book at any time without notice, and assumes no responsibility for any errors within this document. Atmel does not make any commitment to update this information. Atmel assumes no responsibility for the use of any circuits described in this data book, nor does the Company assume responsibility for the functioning of undescribed features or parameters.

In the absence of a written agreement to the contrary, Atmel assumes no liability with respect to the use of semiconductor devices described in this data book for applications assistance, customers' product design or infringement of patents or copyrights of third parties.

Atmel's products are not authorized for use as critical components in life support devices or systems and the use as such implies that user bears all risk of such use.

If Atmel is an approved vendor on a Standard Military Drawing (SMD), the Atmel similar part number specification is compliant with the SMD.

Trademarks or registered trademarks used in this document may be the property of others.

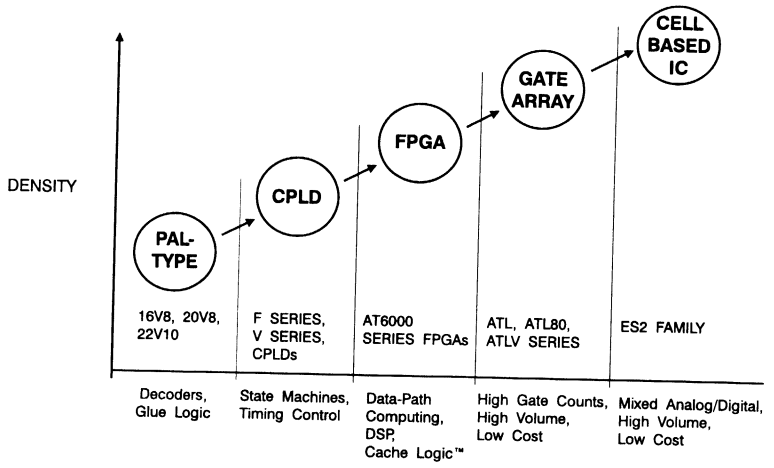
Printed on recycled paper.

Configurable Logic Overview

Thank you for your interest in Atmel's family of fast, flexible PLDs, FPGAs and Gate Arrays. Atmel offers the broadest range of configurable logic (programmable and custom ASIC, see figure) in the industry:

- Industry standard PAL- and GAL-type devices (16V8, 20V8, 22V10):
  - Low power
  - Very high speed
  - 3-volt and 5-volt operation
- High density CPLD devices (ATV750, ATF1500, ATV2500, ATV5000, ATV5100):
  - Up to 5,000 PLD gates using standard PLD design tools
  - Simple extensions of industry-standard 22V10 architecture
  - Wide gate fan-in capability
- FPGAs with *Cache Logic*™ capability, the ability to build adaptive, reusable hardware (AT6002, AT6003, AT6005, AT6010):
  - Up to 20,000 usable gates
  - Thousands of registers (ideal for pipelined, data path applications)
  - Flip-flop toggle rates > 250 MHz, system speeds to 70 MHz
  - Very low power (500 µA standby)
  - Very low profile (PCMCIA) packages (1mm thick)
  - 100% factory-tested

Atmel's Configurable Logic Spectrum



- High density, high performance Gate Arrays:
  - Fast CMOS, 50 MHz and up
  - Low Voltage CMOS, 1.8-volt, 3.3-volt and 5-volt options
  - Gate Array/Standard Cell translation
  - Multiple FPGA/PLD conversions
- Mixed Mode Cell Based ICs:
  - Mixed Analog/Digital
  - High Volume
  - Low Cost

If you are new to PLDs and FPGAs you'll appreciate the simple, easy-to-learn architecture and tools. If you are already using FPGAs you'll find the AT6000 FPGAs are especially suited for high speed, data path applications. The thousands of registers allow for designs to be extensively pipelined, enabling ultra-fast system throughput.

When your design becomes fixed and enters high volume production, the tools let you migrate your pure digital design easily to Atmel's masked Gate Arrays or your mixed mode (analog/digital) design to the ES2 cell based IC family for even more cost effective production.

The ES2 cell based IC products are described in separate documents.

Atmel Corporation designs, manufactures, and markets high quality and high performance CMOS memory, logic and analog integrated circuits. Founded in 1984, the Company serves the manufacturers of computation, communications and instrumentation equipment in commercial, industrial and military environments.

Atmel's broad line of products provide customers with a variety of solutions to their memory and logic applications. Atmel offers high-density, high-speed memory and logic standard products as well as custom gate arrays.

Atmel guarantees quality and reliability by fabricating all products— no matter what their intended application— to meet or exceed the specifications of Military Standard 883.

Whether you are new to programmable logic or an experienced user, Atmel is committed to your success. If you have any questions or would like to place an order, please contact your local Atmel sales office as listed in the back of this data book, or contact Atmel's corporate headquarters:

Atmel Corporation
2125 O'Nel Drive
San Jose, CA 95131
PHONE: (408) 441-0311
FAX: (408) 436-4300

FAX-ON-DEMAND:
U.S. (1-800) 29-ATMEL (292-8635)
International (1-408) 441-0732
PLD Hotline: (408) 436-4333
FPGA ASIC Hotline: (408) 436-4119
E-mail PLD questions: pld@atmel.com

We thank you for considering Atmel semiconductors.

Overview

Table of Contents

Section 4 Programmable Logic Development Tools

Section 5 CMOS Gate Arrays

Table of Contents

Contents

1

Section 1 CMOS Programmable Logic Devices (PLDs)

Flash PLDs

UV Erasable PLDs

Atmel's Broad EPLD Product Line

Atmel has two major EPLD lines: PAL-type SPLDs and high-density V-Series CPLDs. Each has a particular feature set that may be just right for specific design requirements.

Atmel's PAL-Type Products

The Atmel PAL-type family of products is a modified version of the popular industry standard 16V8, 20V8, and 22V10s. Already in wide use, and supported by many development tools, these versions also offer features such as quarter-power and low standby power. Atmel's family of Flash-based devices combines proven high-performance and low-power technologies. As a result, no matter how diverse the application, Atmel has the products to fit the socket.

Atmel CPLD Products

The V-Series CPLDs are based on a 22V10-type architecture and provide market-leading capacity and flexibility in 28, 44, and 68 pins. The ATV750/B has a 22V10 footprint with twice the registers and additional features for better logic utilization. The ATV2500/B offers 24 I/O pins, 48 registers, 17 product terms per macro, and 100% connectivity. The ATV5000/V5100 offer advanced logic density in a 68-pin package with 52 I/O pins and 128 registers, 20 product terms per macro, and high connectivity.

Atmel's Broad EPLD

Device Family	Pins	I/Os	I_S	FF	Speed	$I_{CC(mA)}$
ATF16V8B/BQ/BQL	20	8	10	8	7.5-25 ns	5 mA
ATF20V8B/BQ/BQL	24	8	12	8	7.5-25 ns	5 mA
ATF22V10B/BQ/BQ	24	10	12	10	7.5-25 ns	5 mA
ATV750B/BQ/BQL	24	10	12	20	7.5-25 ns	2 mA
ATV2500B/BQ/BQL	44	24	14	48	12-25 ns	2 mA
ATV5000/L	68	52	8	128	25-30 ns	40 mA
ATV5100/L	68	52	8	128	25-30 ns	40 mA

Standard Development Tools

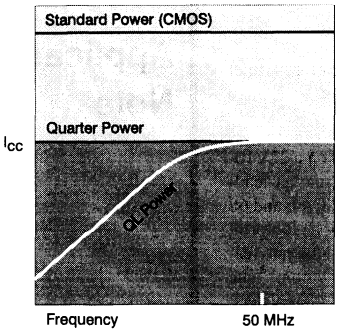
Atmel's philosophy is that designers should be able to use known development tools. Third-party design tools such as ABEL™, CUPL™, PPLDesigner-XL™, LOG/iC™, and PLDsyn™ are supported in Atmel's EPLDs. Also Atmel-specific versions of the popular ABEL, ProPLD, and CUPL design tools are offered. In addition, workstation support is available on popular platforms with Viewlogic, MINC, Cadence, Mentor, RacalRedac, and Synopsys.

No Limits to EPLD Designs with Atmel

Designers are continuously challenged to add more features to their products while using the same board space, and at the same time maintain or decrease the overall power consumption of their system. To meet these challenges, Atmel offers a broad range of high-density, low-power, and cost-effective solutions enabling designers to create products that are "just what the market ordered."

Based on a standard architecture, which uses industry standard development tools, Atmel's EPLDs offer the unique low-power or "L" feature while providing 100% connectivity. These devices are processed with Atmel's proprietary 0.65-micron, electrically erasable and UV-erasable memory processes.

Power Curve[1]



Note: 1. "Atmel's QL products benefit from quarter-power savings and the low standby power feature all in one device."

Power Savings

Atmel's low-power EPLDs are high-performance products with significantly reduced power consumption compared to standard-power devices. Save up to 80% of the power required by competing solutions. Lower power consumption allows for smaller, lower cost power supplies and provides lower junction temperatures that, in turn, result in higher system reliability.

Low-Power Feature

Ideally suited for power sensitive applications, Atmel's low-power devices save power at low frequencies by applying the patented "L" feature. This feature enables the device to power down automatically to a standby mode. The Power Curve graph above shows the Icc vs. Frequency curves for standard-and low-power devices.

At low frequencies, Atmel's low-power devices automatically cycle through the wake up and standby modes to save power while a standard-power device remains powered at all times. The "L" feature provides dramatic power savings for designs with a standby mode ("Green PC") and for those that operate below 50 MHz. Applications that are combinatorial in nature (no clock) also benefit by using Atmel's low-power devices.

Quarter-Power Feature

Atmel's quarter-power devices offer lower active power than a standard-power device. This feature saves power at any frequency, and the parts are compatible with industry standard quarter-power devices available on the market today.

"QL" Products

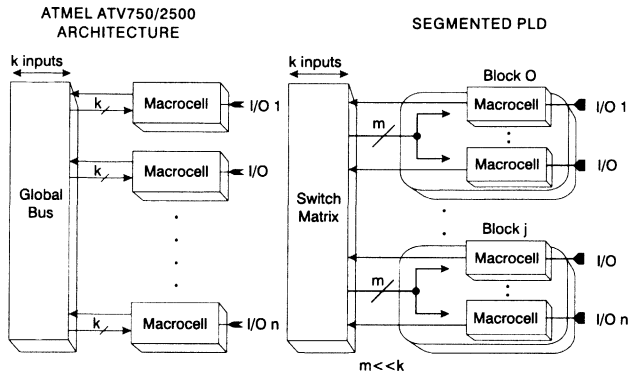
Atmel's quarter-power devices are available with the "L" feature. These "QL" devices benefit from quarter-power savings and the low standby power feature all in one Atmel device—the ultimate in power savings!

No Limits To Connectivity

Connectivity measures how easily and effectively signals are routed between logic blocks within a PLD. In simple EPLDs, such as the industry standard 16V8/20V8/22V10, every input and feedback is connected to every product term of every macrocell—providing 100% connectivity. For CPLDs, it has become common practice to trade off connectivity for speed and die size. Atmel's CPLDs, however, use a global interconnect, architecture that combines speed and the highest connectivity—even 100% connectivity up through 44 pins.

The Atmel 24-pin V750 and 44-pin V2500 devices provide the benefits of true 100% connectivity. Every input and feedback is connected to every product term of every macrocell. This means higher utilization of product density and easier routing. As a result, design modifications are easily made without changing pin assignments.

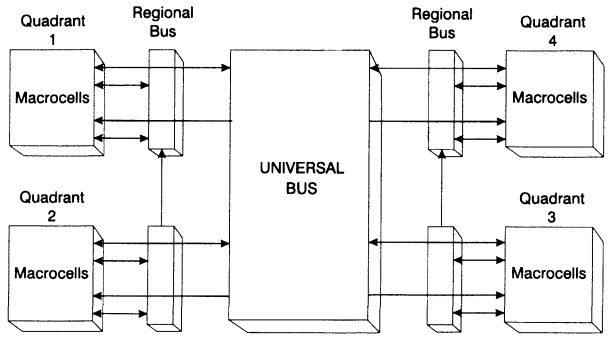
ATV2500 Connectivity(1)



Note: 1. Atmel's global architecture provides "real" 100% connectivity. Other segemented CPLD architectures provide limited connectivity, often in the 10-30% range, increasing the chances of routing difficulties and design delays when changes must be made.

Atmel's focus on connectivity extends even further to the V5000/V5100 architecture. At this density, it is not practical to maintain 100% connectivity. The unique regional/universal bus structure of Atmel's V5000s offers the highest advantage in connectivity, compared to other 68-pin CPLDs. With 49% connectivity, the V5000/V5100 provide a 2 to 4x advantage over other 68-pin CPLDs—the highest connectivity by far. And, when combined with the high density of the V5000/V5100, logic capability increases.

ATV5000/5100 Architecture(1)



Note: 1. The Atmel ATV5000 has a universal bus which connects signals between all four quadrants. Regional buses route signals within each quardrant.

High Performance Flash PLD

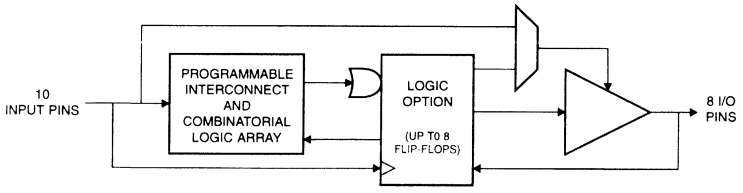
Features

- **Industry Standard Architecture**
  - **Emulates Many 20-Pin PALs®**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Several Power Saving Options**

Device	Icc, Stand-By	Icc, Active
ATF16V8B	50 mA	55 mA
ATF16V8BQ	35 mA	40 mA
ATF16V8BQL	5 mA	20 mA

- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

Block Diagram



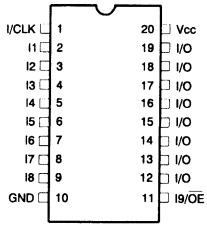
Description

The ATF16V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% for commercial temperature ranges.

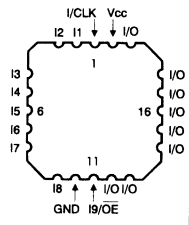
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
VCC	+5 V Supply

DIP/SOIC



PLCC



0364B

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

The ATF16V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

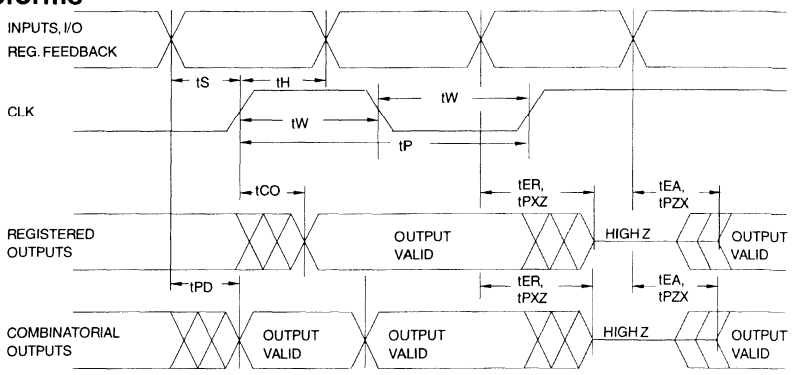
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		55	85	mA
				Ind.		55	95	mA
			B-15, -25	Com.		50	75	mA
				Ind.		50	80	mA
			BQ-10	Com.		35	55	mA
			BQL-15, -25	Com.		5	10	mA
				Ind.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BQL-15, -25	Com.		1		mA/MHz(2)
				Ind.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=15 MHz	B-7, -10	Com.		60	90	mA
				Ind.		60	100	mA
			B-15, -25	Com.		55	85	mA
				Ind.		55	95	mA
			BQ-10	Com.		40	55	mA
			BQL-15, -25	Com.		20	35	mA
				Ind.		20	40	mA
I_{OS}(1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OL} = -24 mA Com., Ind.				0.5	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.

A.C. Waveforms [1]



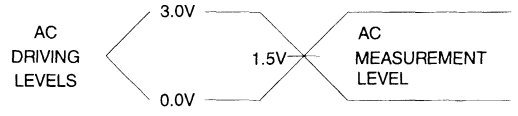
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics [1]

Symbol	Parameter		-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-25 Min	-25 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	7.5	3	10	3	15	3	25	ns
		1 output switching		7							ns
t_{CF}	Clock to Feedback			3		6		8		10	ns
t_{CO}	Clock to Output		2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Setup Time		5		7.5		12		15		ns
t_H	Hold Time		0		0		0		0		ns
t_P	Clock Period		8		12		16		24		ns
t_W	Clock Width		4		6		8		12		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			100		68		45		37	MHz
	Internal Feedback $1/(t_S + t_{CF})$			125		74		50		40	MHz
	No Feedback $1/(t_P)$			125		83		62		41	MHz
t_{EA}	Input to Output Enable — Product Term		3	9	3	10	3	15	3	20	ns
t_{ER}	Input to Output Disable — Product Term		2	9	2	10	2	15	2	20	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	6	2	10	2	15	2	20	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	6	1.5	10	1.5	15	1.5	20	ns

Note: 1. See ordering information for valid part numbers and speed grades.

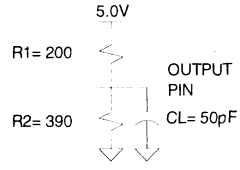
Input Test Waveforms and Measurement Levels:



tR, tF < 5ns (10% to 90%)

Output Test Loads:

Commercial



Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

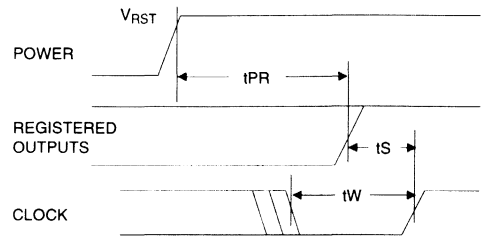
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF16V8Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

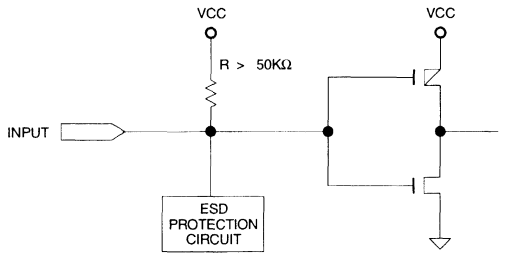
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

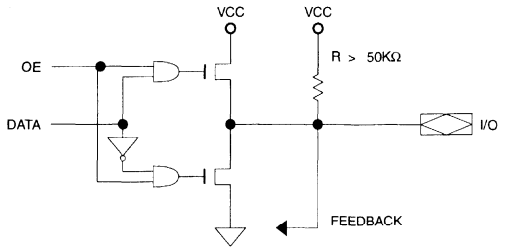
Input and I/O Pull-Ups

All ATF16V8B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B can be configured in one of three different modes. Each mode makes the ATF16V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF16V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R [1]	GAL16V8_C7 [1]	GAL16V8_C8 [1]	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Only applicable for version 3.4 or lower.

Macrocell Configuration

Software compilers support the three different OMC modes as different device types. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

ATF16V8B Registered Mode

PAL Device Emulation / PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

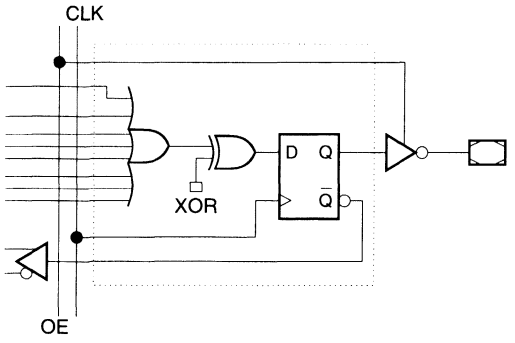
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

16R8 16RP8

16R6 16RP6

16R4 16RP4

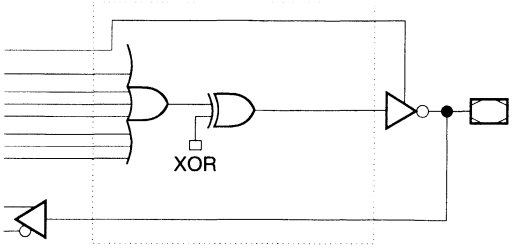
Registered Configuration for Registered Mode (1,2)



Notes:

1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

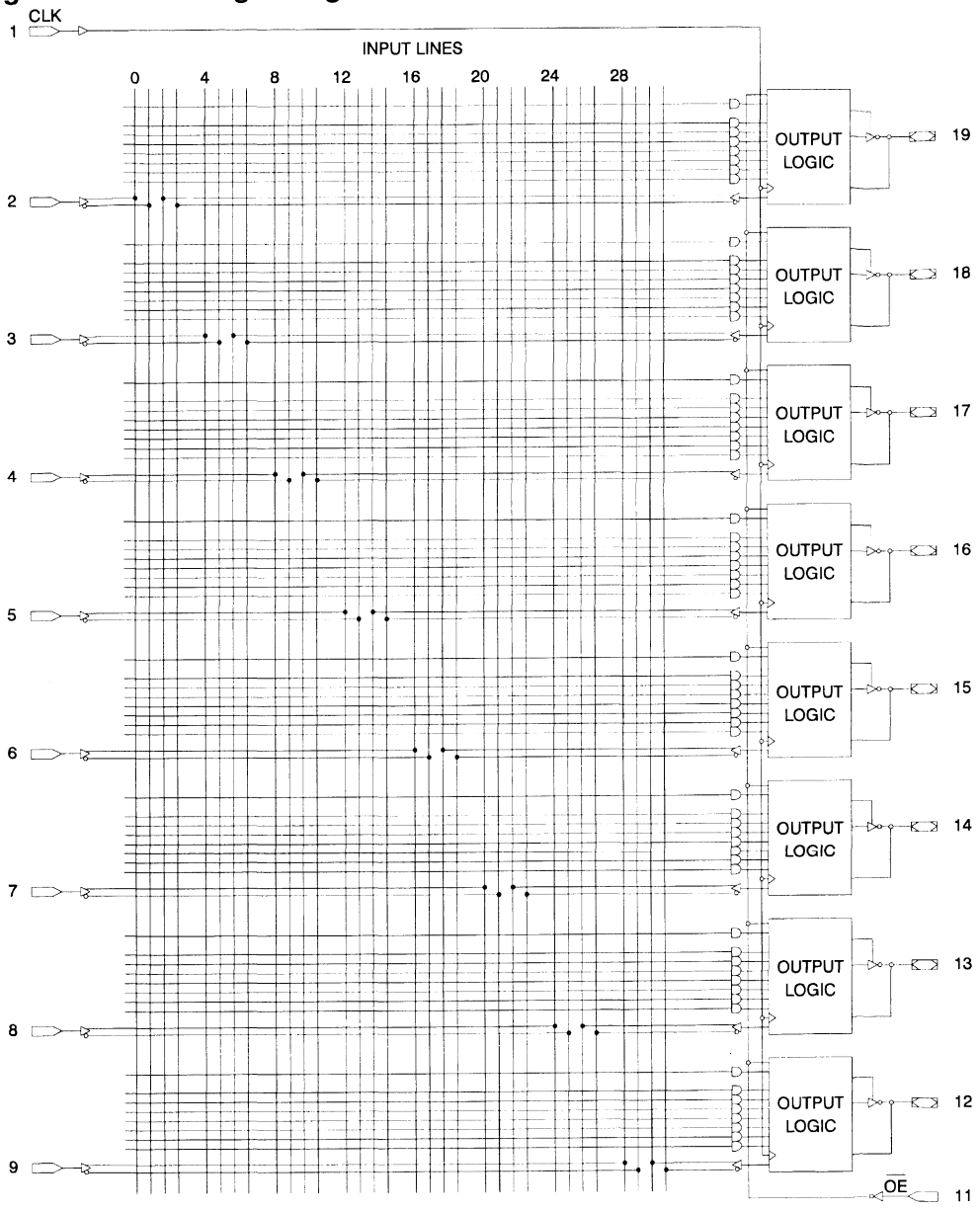
Combinatorial Configuration for Registered Mode (1,2)



Notes:

1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram



ATF16V8B Complex Mode

PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

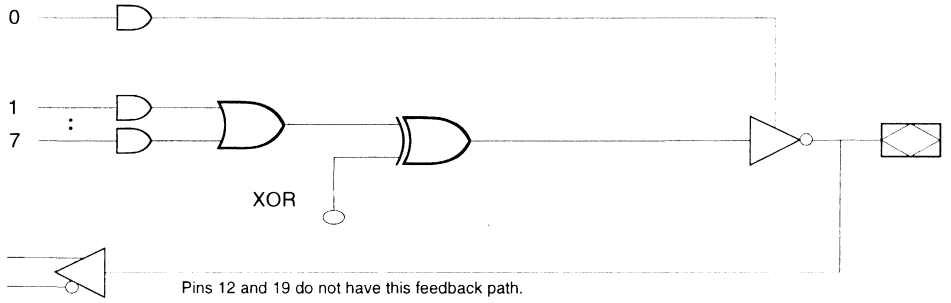
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8

16H8

16P8

Complex Mode Option



ATF16V8B Simple Mode

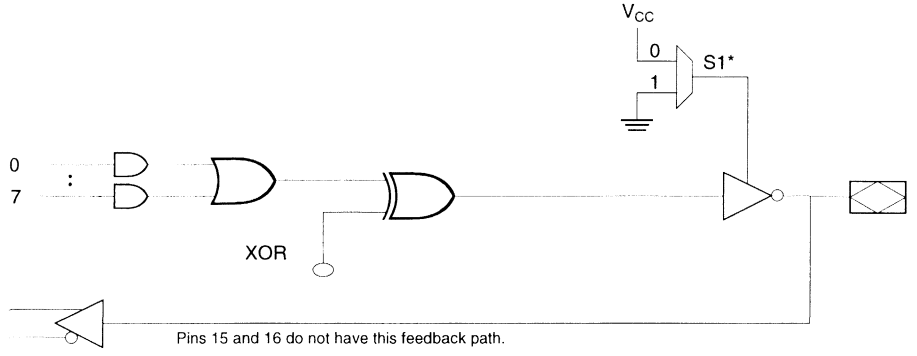
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

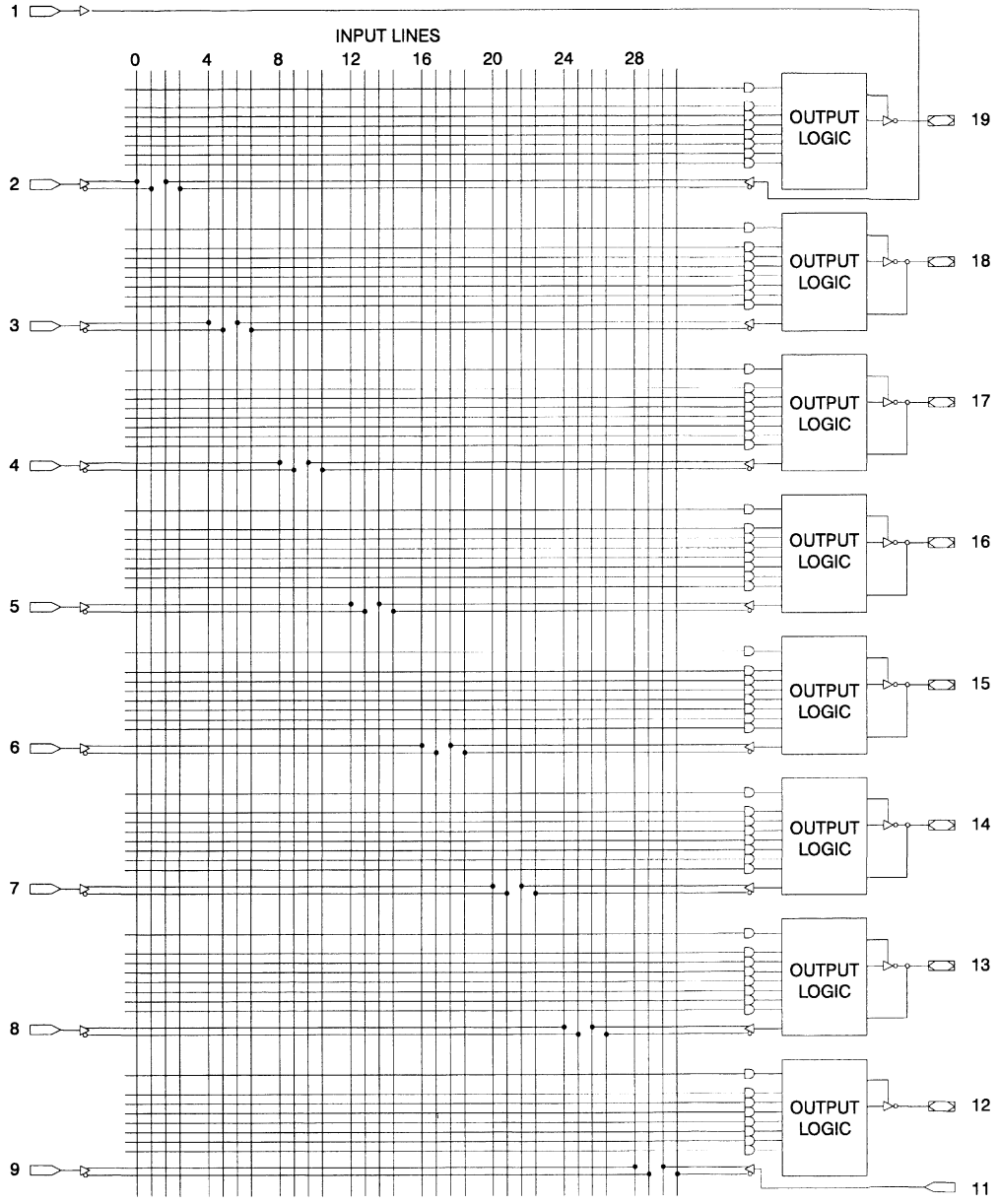
10L8	10H8	10P8
12L6	12H6	12P6
14L4	14H4	14P4
16L2	16H2	16P2

Simple Mode Option

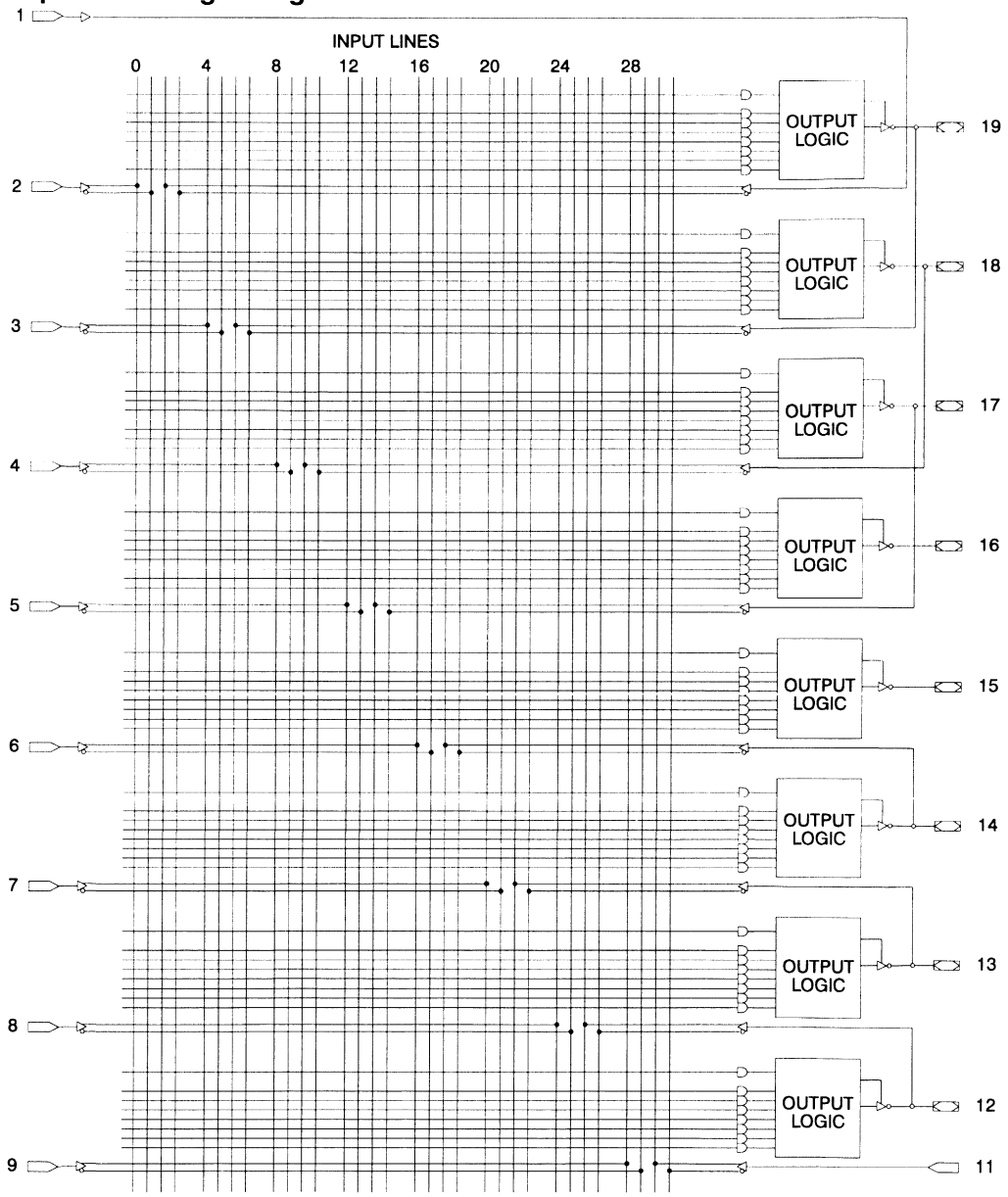


* - Pins 15 and 16 are always enabled.

Complex Mode Logic Diagram

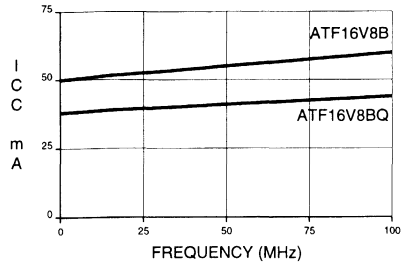


Simple Mode Logic Diagram



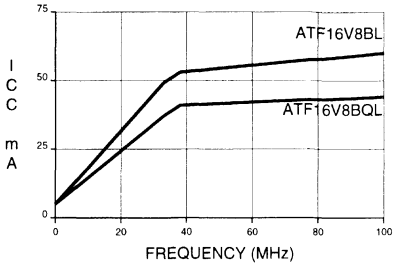
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8B/BQ (VCC = 5V, TA = 25C)



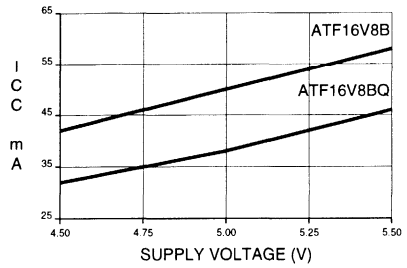
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8BL/BQL (VCC = 5V, TA = 25C)



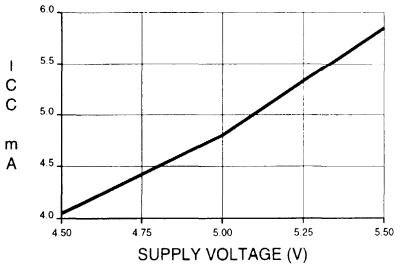
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8B/BQ (TA = 25C)



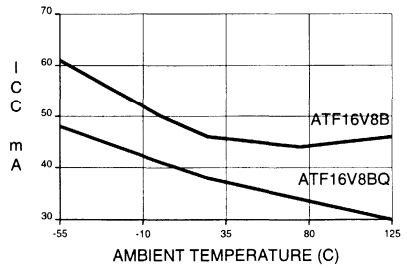
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8BL/BQL (TA = 25C)



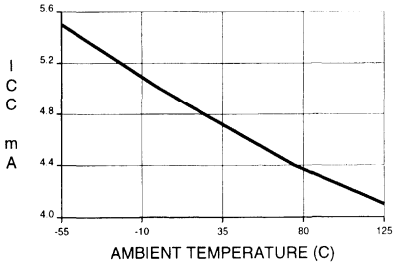
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8B/BQ (VCC = 5V)



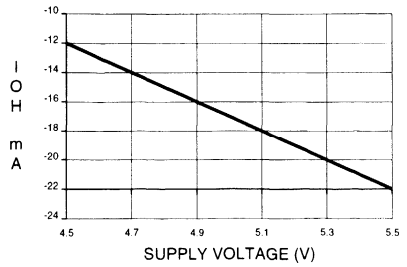
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8BL/BQL (VCC = 5V)



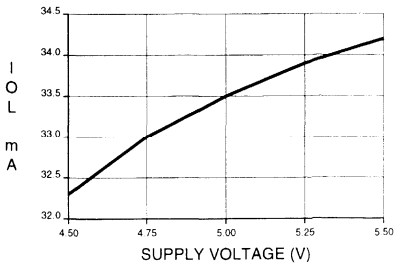
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)

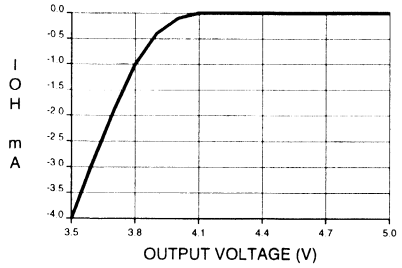


OUTPUT SINK CURRENT

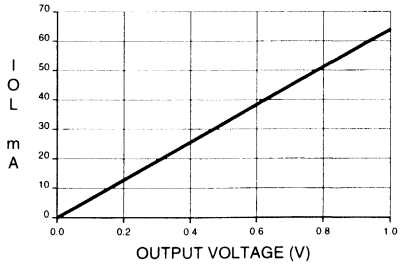
vs. SUPPLY VOLTAGE (TA = 25C)



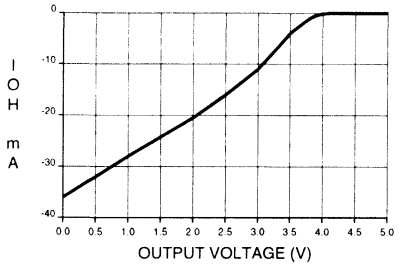
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



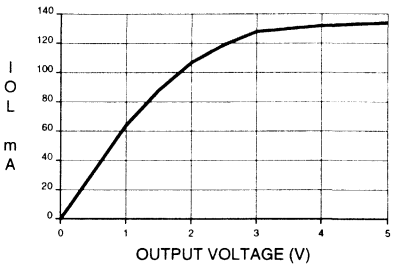
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



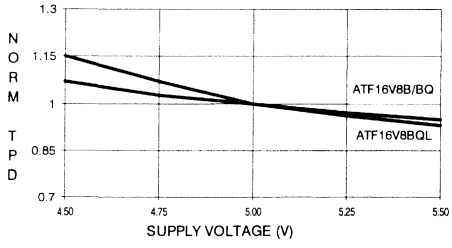
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



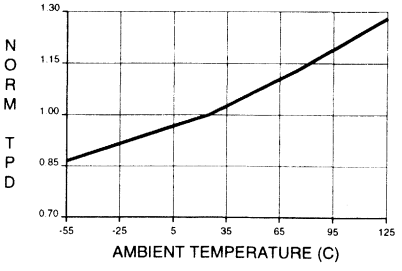
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



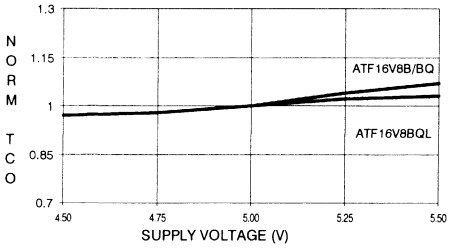
NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA=25°C)



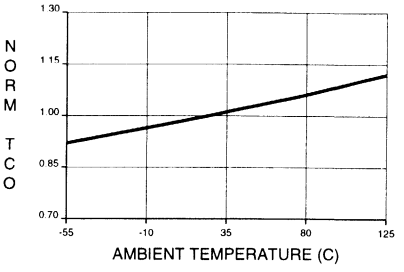
NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC = 5V)



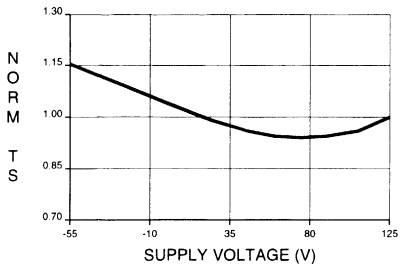
NORMALIZED TCO
vs. SUPPLY VOLTAGE (TA=25°C)



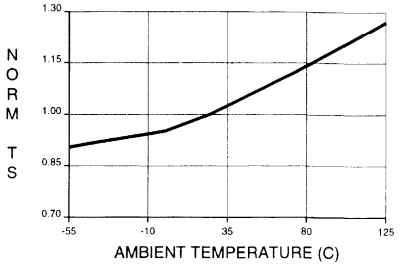
NORMALIZED TCO
vs. AMBIENT TEMPERATURE (VCC = 5V)



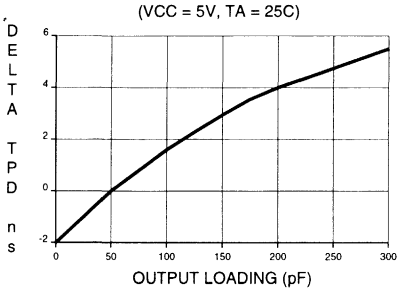
NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)



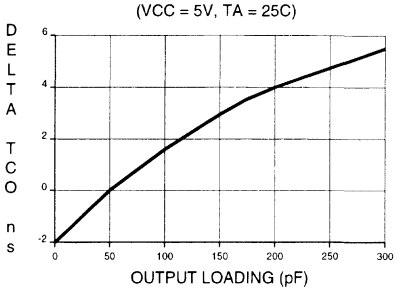
NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)



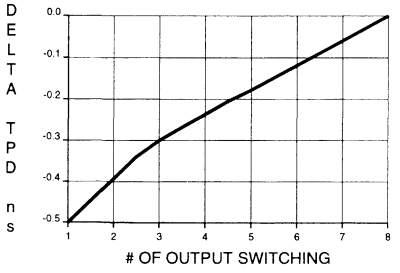
DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



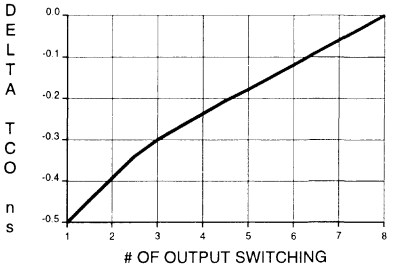
DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



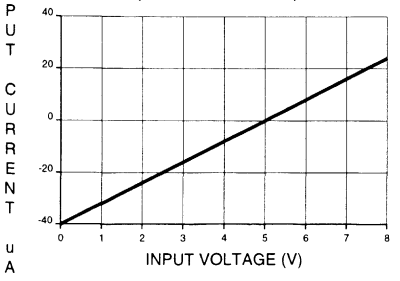
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



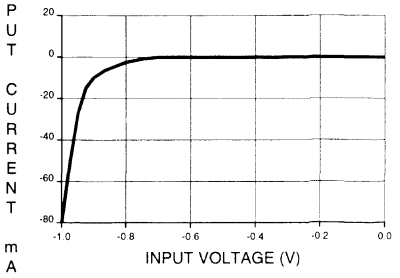
DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	5	5	ATF16V8B-7JC ATF16V8B-7PC ATF16V8B-7SC	20J 20P3 20S	Commercial (0°C to 70°C)
10	7.5	7	ATF16V8B-10JC ATF16V8B-10PC ATF16V8B-10SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8B-10JI ATF16V8B-10PI ATF16V8B-10SI	20J 20P3 20S	Industrial (-40°C to 85°C)
15	12	10	ATF16V8B-15JC ATF16V8B-15PC ATF16V8B-15SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8B-15JI ATF16V8B-15PI ATF16V8B-15SI	20J 20P3 20S	Industrial (-40°C to 85°C)
25	15	12	ATF16V8B-25JC ATF16V8B-25PC ATF16V8B-25SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8B-25JI ATF16V8B-25PI ATF16V8B-25SI	20J 20P3 20S	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7.5	7	ATF16V8BQ-10JC ATF16V8BQ-10PC	20J 20P3	Commercial (0°C to 70°C)
15	12	10	ATF16V8BQL-15JC ATF16V8BQL-15PC ATF16V8BQL-15SC	20J 20P3 20S	Commercial (0°C to 70°C)
25	15	12	ATF16V8BQL-25JC ATF16V8BQL-25PC ATF16V8BQL-25SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8BQL-25JI ATF16V8BQL-25PI ATF16V8BQL-25SI	20J 20P3 20S	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

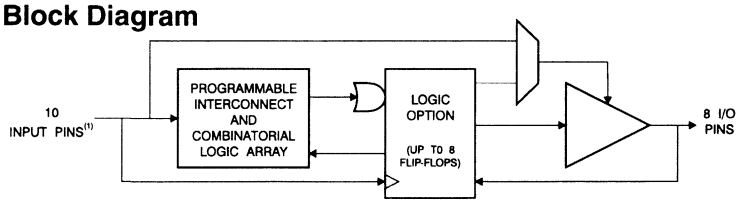
Features

- **Industry Standard Architecture**
  - **Emulates Many 20-Pin PALs®**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **5 ns Maximum Pin-to-Pin Delay**
- **Low Power - 10 µA Standby and Power Down Modes**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Bus-friendly Input and I/O Pin Keeper Circuits**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

High Performance Flash PLD

Preliminary

Block Diagram



Note: 1. Includes optional PD control pin

Description

The ATF16V8C is a high performance EECMOS Programmable Logic Device which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and a 10 µA power down mode are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges; 5 V ± 5% for commercial range 5-Volt devices.

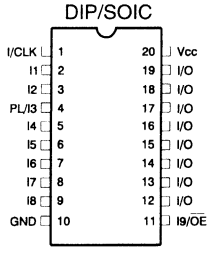
The ATF16V8C incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

The ATF16V8C can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When pin 4 is configured as the power down control pin , supply current drops to less than 10 µA whenever the pin is high. If the power down feature isn't required for a particular application, pin 4 may be used as a logic input. Also, the bus-friendly pin keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

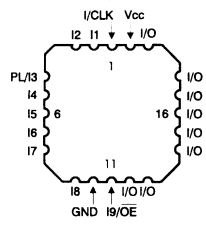
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
VCC	+5 V Supply
PD	Power Down

DIP/SOIC



PLCC



0425A

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

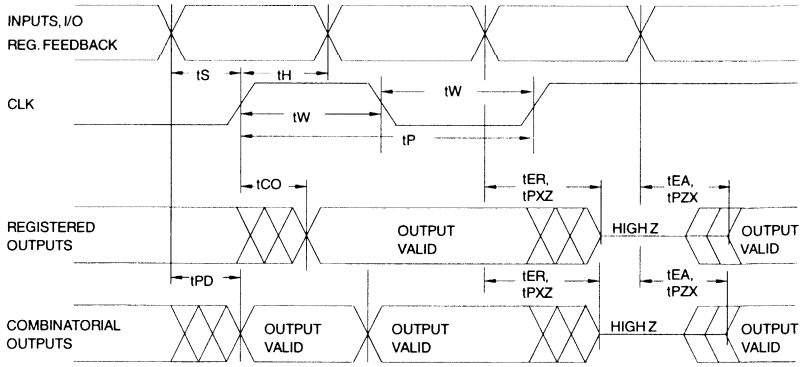
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition		Min	Type	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10	µA
I_{CC1}(1)	Power Supply Current, Standby	MHz, VCC = MAX, V_{IN} = 0, V_{CC}, Outputs Open	Com.			115	mA
			Ind.			130	mA
I_{CC2}(1)	Power Supply Current, Power Down Mode	V_{CC} = MAX, V_{IN} = 0, V_{CC}	Com.			10	µA
			Ind.			15	µA
I_{CC3}(1)	Clocked Power Supply Current	F=15, V_{CC} = MAX, V_{CC}, Outputs Open	Com.		1		mA/MHz
			Ind.		1		mA/MHz
I_{OS}	Output Short Circuit Current	VOUT = 0.5 V; V_{CC}= 5 V; TA=25 C				-150	mA
V_{IL}	Input Low Voltage	MIN < V_{CC} < MAX		-0.5	-0.5	0.8	V
V_{IH}	Input High Voltage			2.0	2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = MIN; All Outputs	Com., Ind.				
V_{OH}	Output High Voltage	V_{CC} = MIN		2.4	2.4		V
I_{OL}	Output Low Voltage	V_{CC} = MIN	Com., Ind.				
I_{OH}	Output High Voltage	V_{CC} = MIN		-4	-4		mA

Note: 1. All I_{CC} parameters measured with outputs open.

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

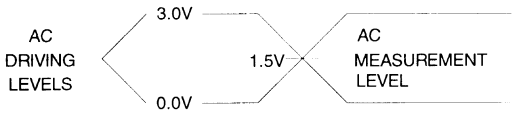
Symbol	Parameter	-5		-7		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output	1	5	3	7.5	ns
t_{CF}	Clock to Feedback		3		3	ns
t_{CO}	Clock to Output	1	4	2	5	ns
t_S	Input or Feedback Setup Time	3		5		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	6		8		ns
t_W	Clock Width	3		4		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$		142		100	MHz
	Internal Feedback $1/(t_S + t_{CF})$		166		125	MHz
	No Feedback $1/(t_P)$		166		125	MHz
t_{EA}	Input to Output Enable — Product Term	2	6	3	9	ns
t_{ER}	Input to Output Disable — Product Term	2	5	2	9	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	5	2	6	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	5	1.5	6	ns

Power Down A.C. Characteristics

Symbol	Parameter	-5 Min	-5 Max	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	Units
t_{IVDH}	Valid Input Before PD High	5		7.5		10		15		ns
t_{GVDH}	Valid $\overline{OE}$ Before PD High	0		0		0		0		ns
t_{CVDH}	Valid Clock Before PD High	0		0		0		0		ns
t_{DHIX}	Input Don't Care After PD High		10		15		18		20	ns
t_{DHGX}	$\overline{OE}$ Don't Care After PD High		10		15		18		20	ns
t_{DHCX}	Clock Don't Care After PD High		10		15		18		20	ns
t_{DLIV}	PD Low to Valid Input		1		1		1		1	µs
t_{DLGV}	PD Low to Valid $\overline{OE}$		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1	µs

Notes: 1. Output data is latched and held.
2. HI-Z outputs remain HI-Z.
3. Clock and input transitions are ignored.

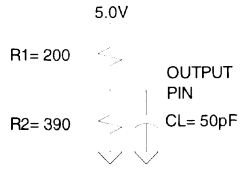
Input Test Waveforms and Measurement Levels:



tR, tF < 1.5ns (10% to 90%)

Output Test Loads:

Commercial



Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

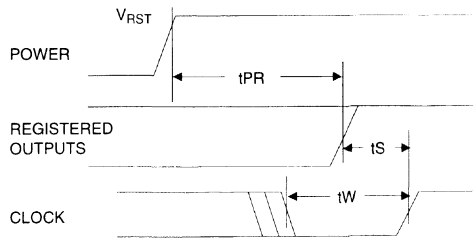
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The ATF16V8C's registers are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Power Down Mode

The ATF16V8C includes an optional pin controlled power down feature. Device pin 4 may be configured as the power down pin. When this feature is enabled and the power down pin is high, total current consumption drop to less than 10 µA. In the power down mode, all output data and internal logic states are latched and held. All registered and combinatorial output data remains valid. Any outputs which were in a HI-Z state at the onset of power down will remain at HI-Z. During power down, all input signals except the power down pin are blocked. The input and I/O pin keeper circuits remain active to insure that pins do not float to indeterminate levels. This helps to further reduce system power.

Selection of the power down option is specified in the ATF16V8C logic design file. The logic compiler will include this option selection in the otherwise standard 16V8 JEDEC fuse file. When the power down feature is not specified in the design file, pin 4 is available as a logic input, and there is no power down pin. This allows the ATF16V8C to be programmed using any existing standard 16V8 fuse file.

Registered Output Preload

The ATF16V8C's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

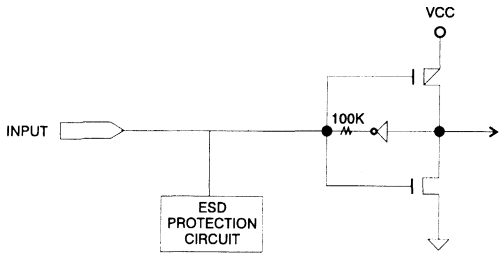
The security fuse should be programmed last, as its effect is immediate.

Input and I/O Pull-Ups

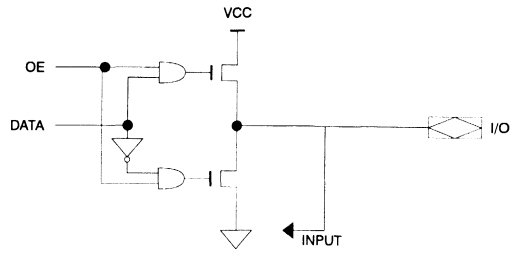
The ATF16V8C contains internal input and I/O bus-friendly pin keeper circuits. These circuits allow each ATF16V8C pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 µA.

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8C architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8C can be configured in one of three different modes. Each mode makes the ATF16V8C look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8C universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8C can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF16V8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R [2]	GAL16V8_C7 [2]	GAL16V8_C8 [2]	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Not applicable when using Pin-controlled PD (Power-down) feature.
2. Only applicable for version 3.4 or lower.

Macrocell Configuration

Software compilers support the three different OMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

ATF16V8C Registered Mode

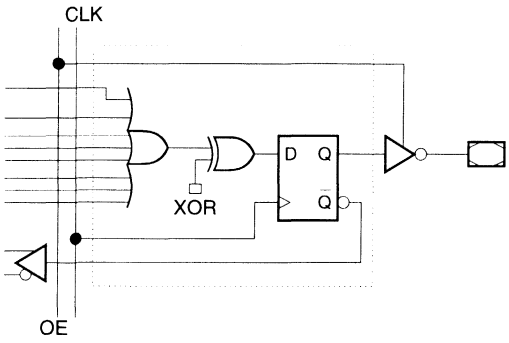
PAL Device Emulation / PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

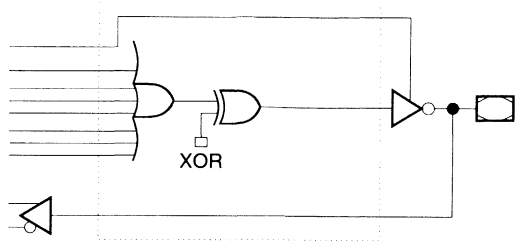
16R8	16RP8
16R6	16RP6
16R4	16RP4

Registered Configuration for Registered Mode (1,2)



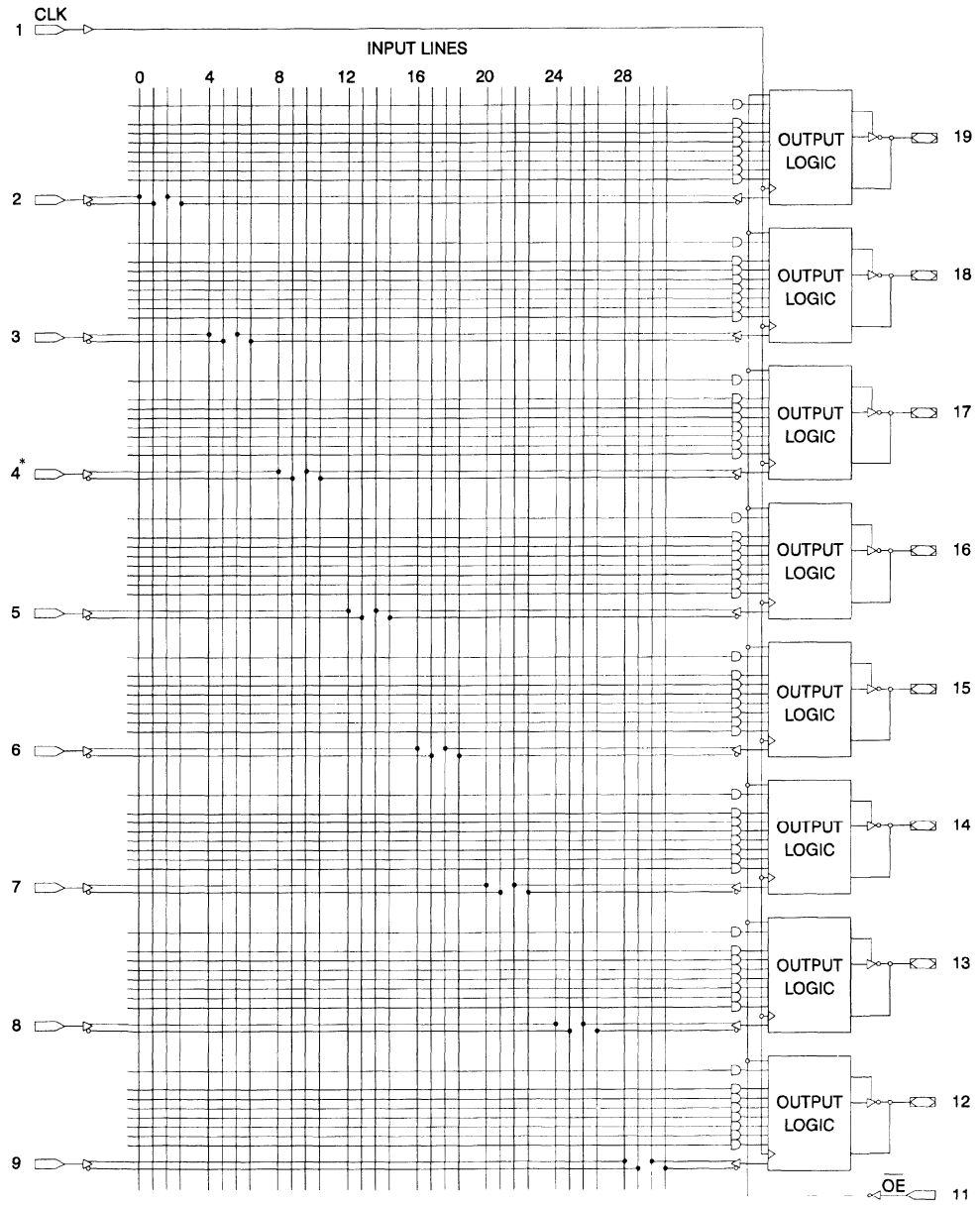
Notes:
1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Configuration for Registered Mode (1,2)



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram



* Input not available if power down mode is enabled.

ATF16V8C Complex Mode

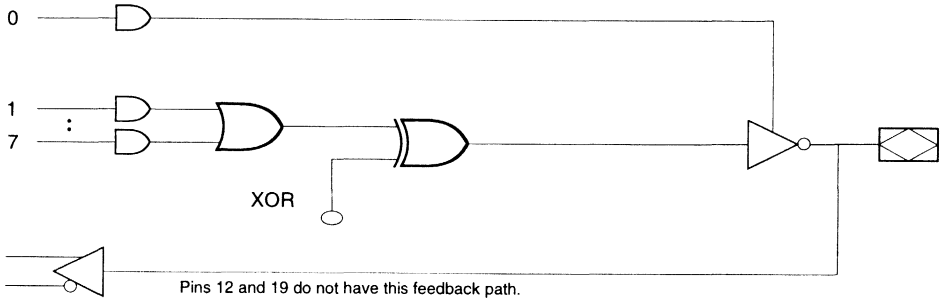
PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8
16H8
16P8

Complex Mode Option



ATF16V8C Simple Mode

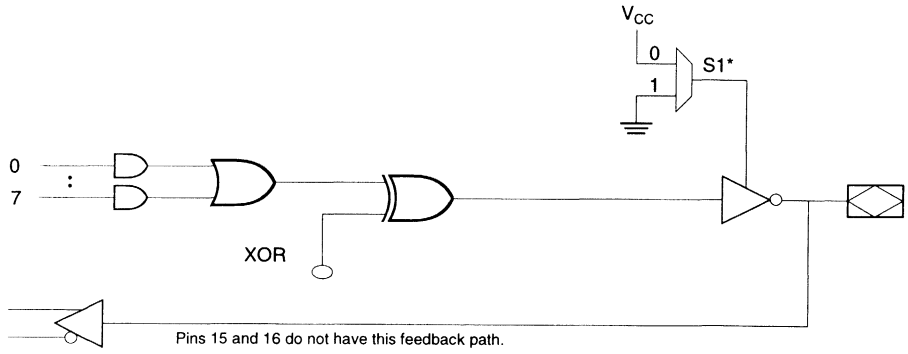
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

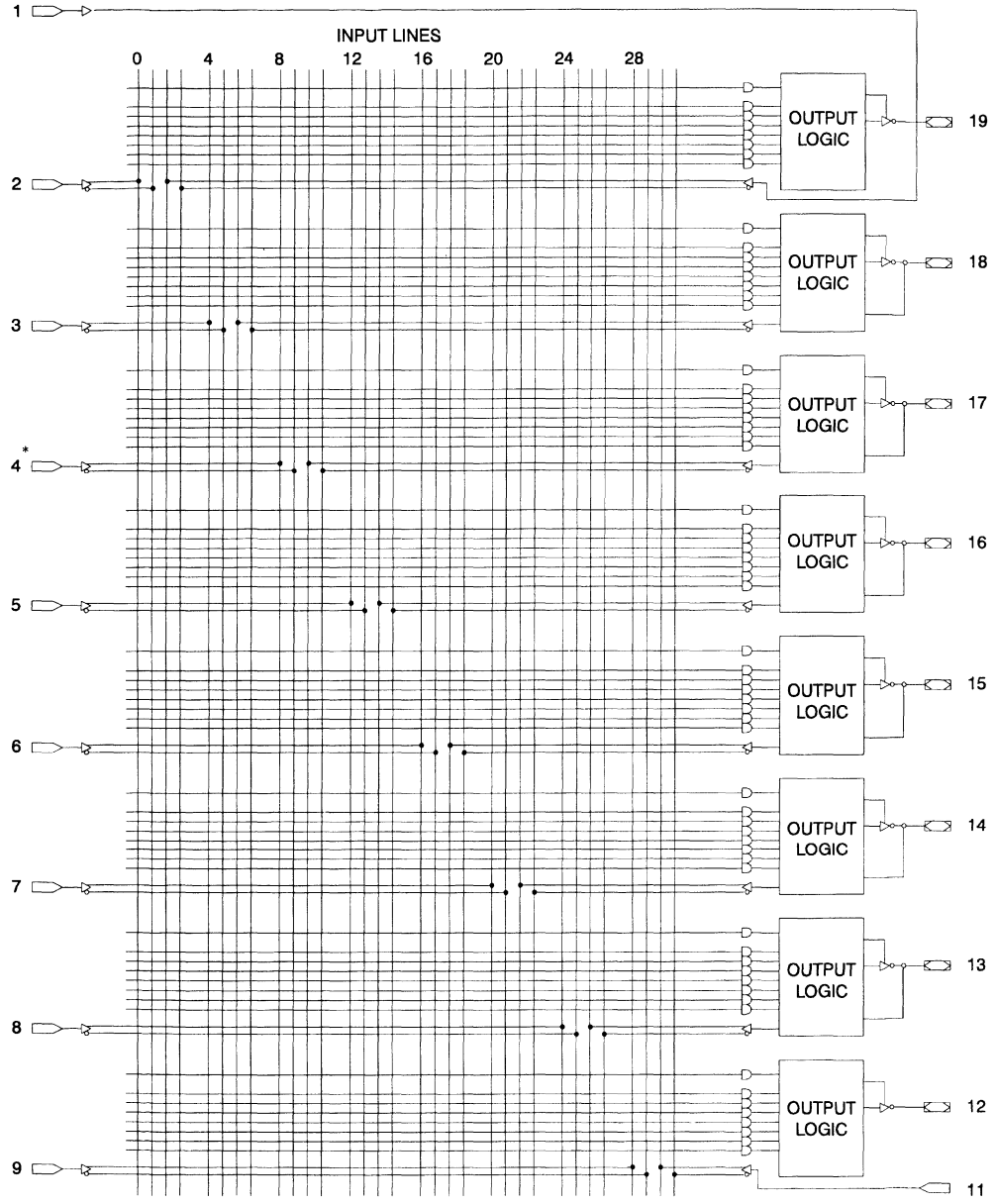
10L8	10H8	10P8
12L6	12H6	12P6
14L4	14H4	14P4
16L2	16H2	16P2

Simple Mode Option



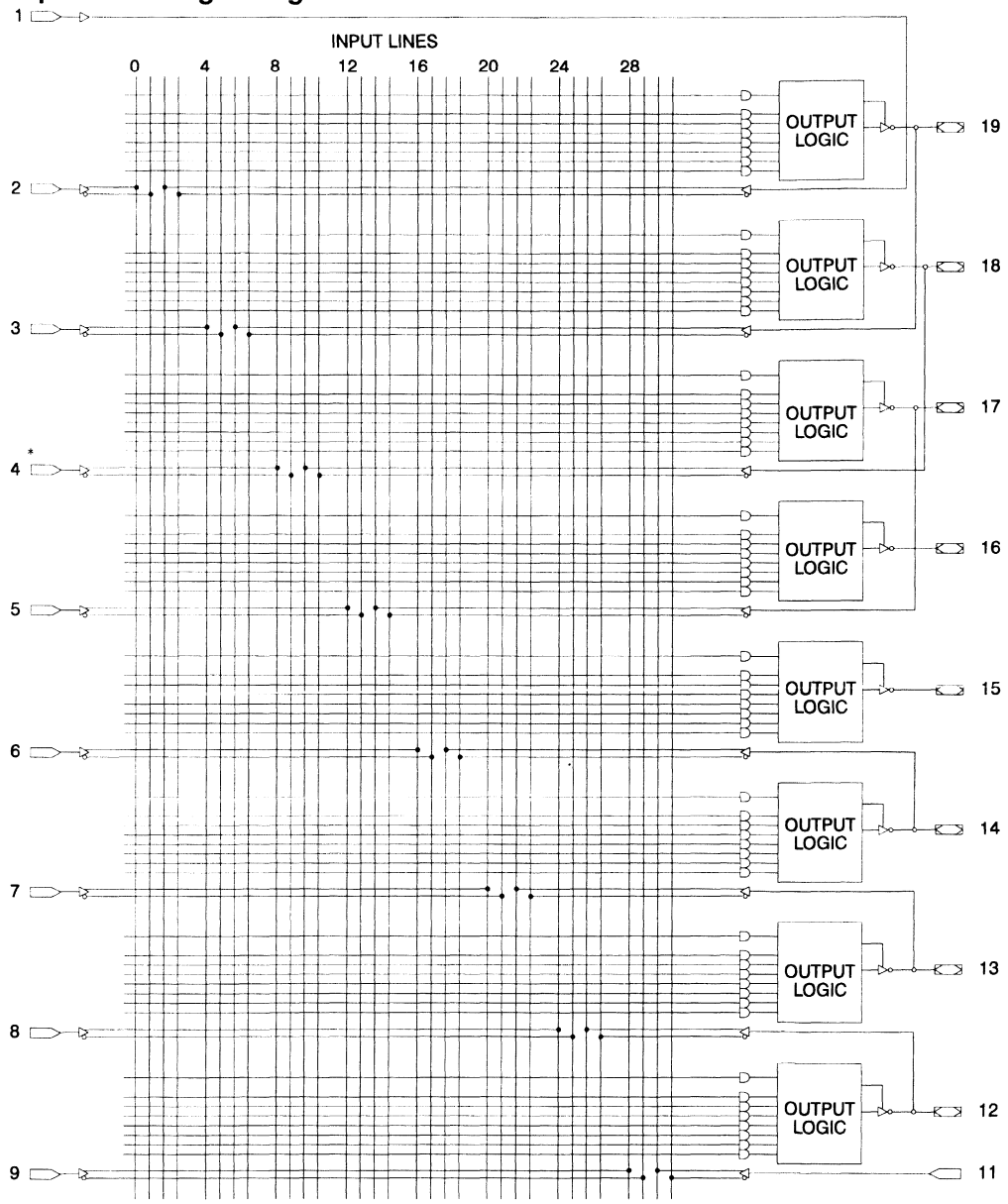
* - Pins 15 and 16 are always enabled.

Complex Mode Logic Diagram



* Input not available if power down mode is enabled.

Simple Mode Logic Diagram



* Input not available if power down mode is enabled.

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	3	4	ATF16V8C-5JC	20J	Commercial (0°C to 70°C)
7.5	5	5	ATF16V8C-7JC ATF16V8C-7PC ATF16V8C-7SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8C-7JI ATF16V8C-7PI ATF16V8C-7SI	20J 20P3 20S	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

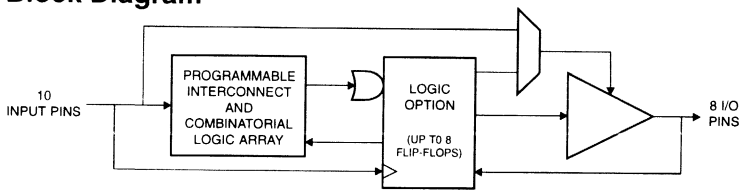
Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF16V8B
- Operates down to 2.7 V
- Pin-Controlled Zero Standby Power (10 µA Typical)
- Ideal For Battery Power Systems
  - Emulates Many 20-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 10 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Holds Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

The ATF16LV8C is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with zero standby power dissipation are offered. All pins offer low ± 10 µA leakage.

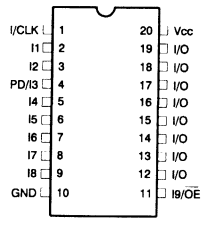
The ATF16LV8C provides a low voltage and user controlled "zero" power CMOS PLD solution with operating voltages down to 2.7 V. The ATF16LV8C has a user-controlled power down feature, offering "zero" (10 µA typical) standby power. This feature allows the user to

(continued)

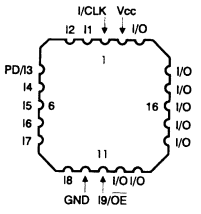
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
VCC	+5 V Supply
PD	Power Down

DIP



PLCC



0403A

Description (Continued)

manage total system power to meet specific application requirements, enhance reliability, all without sacrificing speed. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors.

The ATF16LV8C incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3 V ± 5%	3 V ± 10%

Functional Description

The ATF16LV8C macrocell can be configured in one of three different modes. Each mode makes the ATF16LV8C look like a different device. The ATF16LV8C can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16LV8C is capable of operating at supply voltages down to 2.7 V. A user-controlled power down pin is offered which, when active, allows the user to place the device into a "zero" standby power power-down mode, thereby further decreasing overall system power consumption. When the power down pin is not used or active, the device operates in a full power low-voltage mode. Static power loss due to pull-up resistors is reduced through input and output pin "keeper" circuits which hold pins to their previous logic levels when idle. (The ATF16LV8CZ provides edge-sensing "zero" standby power (10 µA typical), see the ATF16LV8CZ Data Sheet in this Data Book.)

The universal architecture of the ATF16LV8C can be programmed to emulate many 20-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF16LV8C can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF16LV8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Not applicable when using pin controlled PD (Power-down) feature.

1

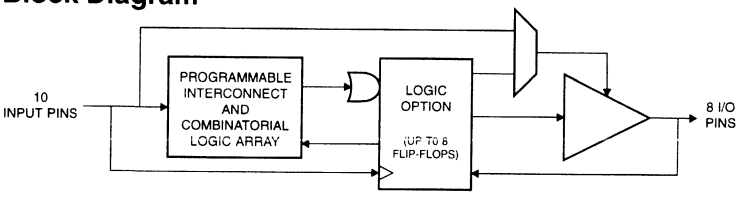
High Performance Flash PLD

Advance Information

Features

- Edge-Controlled Power Down Pin
- Zero Power Equivalent of ATF16V8B
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Industry Standard Architecture
  - Emulates Many 20-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 10 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Holds Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

Block Diagram



Description

The ATF16V8CZ is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% for commercial ranges.

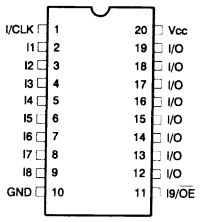
The ATF16V8CZ provides the zero power CMOS PLD solution, with "zero" standby power (10 µA typical). The ATF16V8CZ powers down automatically through Atmel's patented In-

(continued)

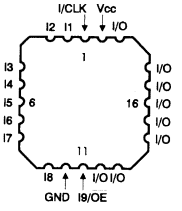
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
VCC	+5 V Supply

DIP



PLCC



0453A

Description (Continued)

put Transition Detection (ITD) circuitry to the "zero" standby power mode when the device remains idle. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors.

The ATF16V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

Functional Description

The ATF16V8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF16V8CZ look like a different device. The ATF16V8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8CZ powers down automatically to a "zero" standby power mode (10 µA typical) through the ITD circuitry when all inputs are idle. This feature allows the user flexibility to manage total system power and enhance reliability all without sacrificing speed. Static power loss due to pull-up resistors is reduced through input and output pin "keeper" circuits which hold pins to their previous logic levels when idle.

The universal architecture of the ATF16V8CZ can be programmed to emulate many 20-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF16V8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF16V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

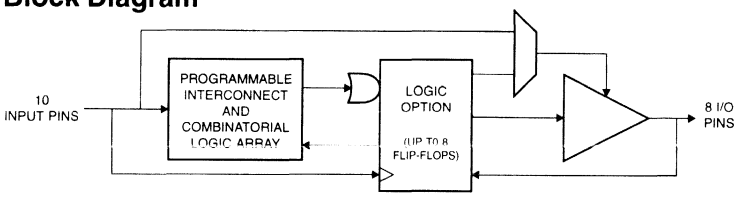
Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF16V8B
- Operates down to 2.7 V
- Edge Sensing Zero Standby Power (10 µA Typical)
- Ideal For Battery Power Systems
  - Emulates Many 20-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 10 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Holds Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

The ATF16LV8CZ is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with zero standby power dissipation are offered. All pins offer low ± 10 µA leakage.

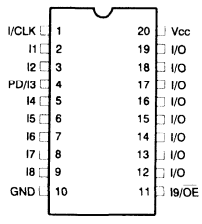
The ATF16LV8CZ provides a low voltage and "zero" power CMOS PLD solution with operating voltages down to 2.7 V. The ATF16LV8CZ has an edge sensing power down feature, offering "zero" (10 µA typical) standby power. This feature allows the user to manage total

(continued)

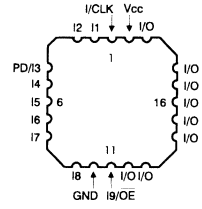
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
VCC	+5 V Supply
PD	Power Down

DIP



PLCC



0404A

Description (Continued)

system power to meet specific application requirements, enhance reliability, all without sacrificing speed. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors.

The ATF16LV8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3 V ± 5%	3 V ± 10%

Functional Description

The ATF16LV8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF16LV8CZ look like a different device. The ATF16LV8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16LV8CZ is capable of operating at supply voltages down to 2.7 V. The ATF16LV8CZ provides edge-sensing "zero" standby power (10 µA typical).

The universal architecture of the ATF16LV8CZ can be programmed to emulate many 20-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF16LV8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF16LV8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

Note: 1. Not applicable when using pin controlled PD (Power-down) feature.

High Performance Flash PLD

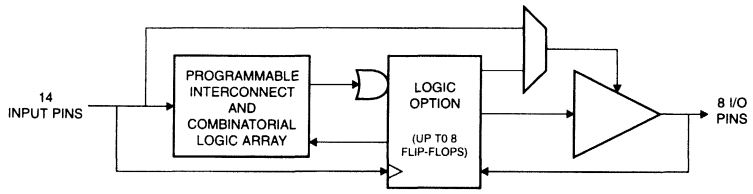
Features

- Industry Standard Architecture
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 7.5 ns Maximum Pin-to-Pin Delay
- Several Power Saving Options

Device	Icc, Stand-By	Icc, Active
ATF20V8B	50 mA	55 mA
ATF20V8BQ	35 mA	40 mA
ATF20V8BQL	5 mA	20 mA

- CMOS and TTL Compatible Inputs and Outputs
  - Input and I/O Pull-Up Resistors
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

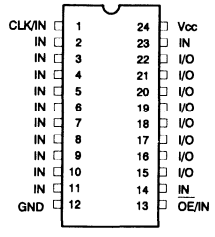
Block Diagram



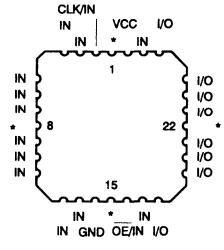
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



PLCC



0407A

Description

The ATF20V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% for commercial temperature ranges.

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

The ATF20V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation,

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

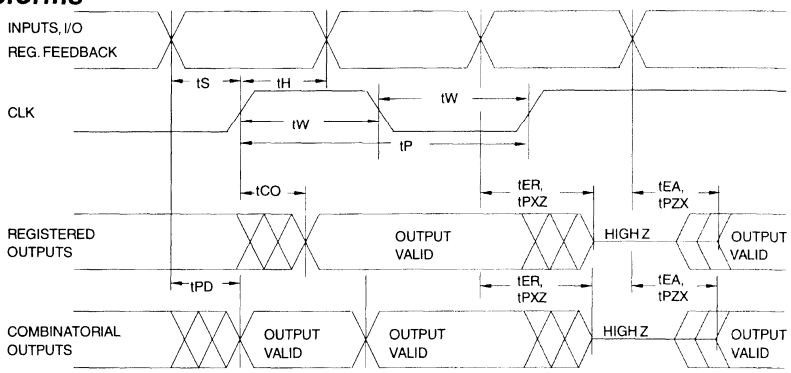
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}(MAX)$				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		60	90	mA
				Ind.		60	100	mA
			B-15, -25	Com.		60	80	mA
				Ind.		60	90	mA
			BQ-10	Com.		35	55	mA
			BQL-15, -25	Com.		5	10	mA
				Ind.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BQL-15, -25	Com.		1		mA/MHz(2)
				Ind.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=15 MHz	B-7, -10	Com.		80	110	mA
				Ind.		80	125	mA
			B-15, -25	Com.		60	90	mA
				Ind.		60	105	mA
			BQ-10	Com.		40	55	mA
			BQL-15, -25	Com.		20	35	mA
				Ind.		20	40	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OL} = 24 mA	Com., Ind.			0.5	V
			I_{OL} = 16 mA				0.5	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.

A.C. Waveforms [1]



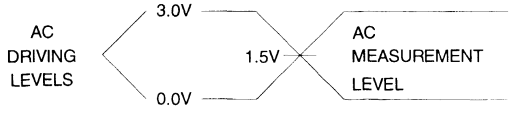
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics [1]

Symbol	Parameter		-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-25 Min	-25 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	7.5	3	10	3	15	3	25	ns
		1 output switching		7							ns
t_{CF}	Clock to Feedback			3		6		8		10	ns
t_{CO}	Clock to Output		2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Setup Time		5		7.5		12		15		ns
t_H	Hold Time		0		0		0		0		ns
t_P	Clock Period		8		12		16		24		ns
t_W	Clock Width		4		6		8		12		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			100		68		45		37	MHz
	Internal Feedback $1/(t_S + t_{CF})$			125		74		50		40	MHz
	No Feedback $1/(t_P)$			125		83		62		41	MHz
t_{EA}	Input to Output Enable — Product Term		3	9	3	10	3	15	3	20	ns
t_{ER}	Input to Output Disable — Product Term		2	9	2	10	2	15	2	20	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	6	2	10	2	15	2	20	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	6	1.5	10	1.5	15	1.5	20	ns

Note: 1. See ordering information for valid part numbers and speed grades.

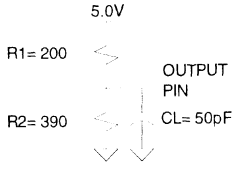
Input Test Waveforms and Measurement Levels:



tR, tF < 5ns (10% to 90%)

Output Test Loads:

Commercial



Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

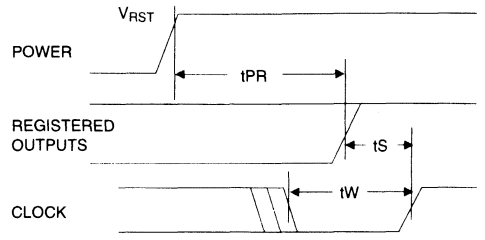
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF20V8Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF20V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

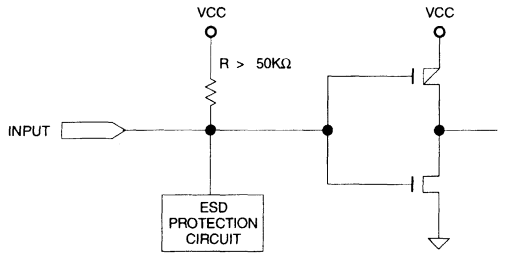
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

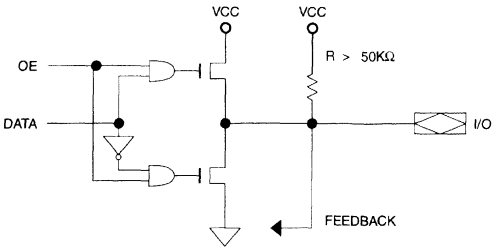
Input and I/O Pull-Ups

All ATF20V8B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF20V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF20V8B can be configured in one of three different modes. Each mode makes the ATF20V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF20V8B universal architecture can be programmed to emulate many 24-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF20V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF20V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8	P20V8
CUPL	G20V8MS	G20V8MA	G20V8	G20V8
LOG/iC	GAL20V8_R (1)	GAL20V8_C7 (1)	GAL20V8_C8 (1)	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8
PLDesigner	P20V8	P20V8	P20V8	P20V8
Tango-PLD	G20V8	G20V8	G20V8	G20V8

Note: 1. Only applicable for version 3.4 or lower.

ATF20V8B Registered Mode

PAL Device Emulation / PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

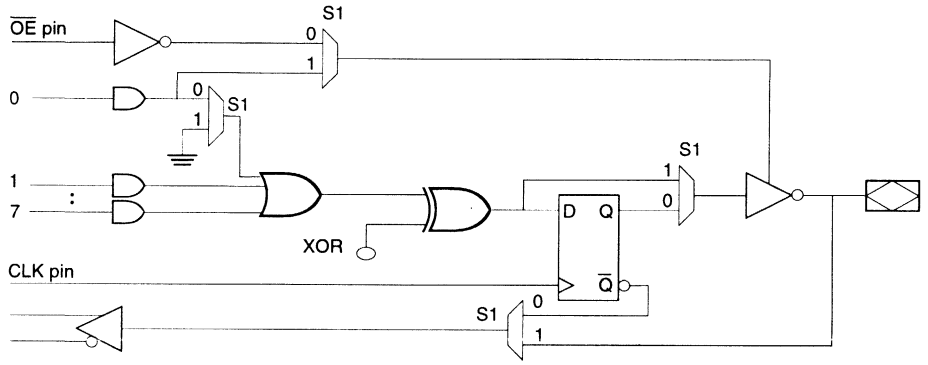
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

20R8 20RP8

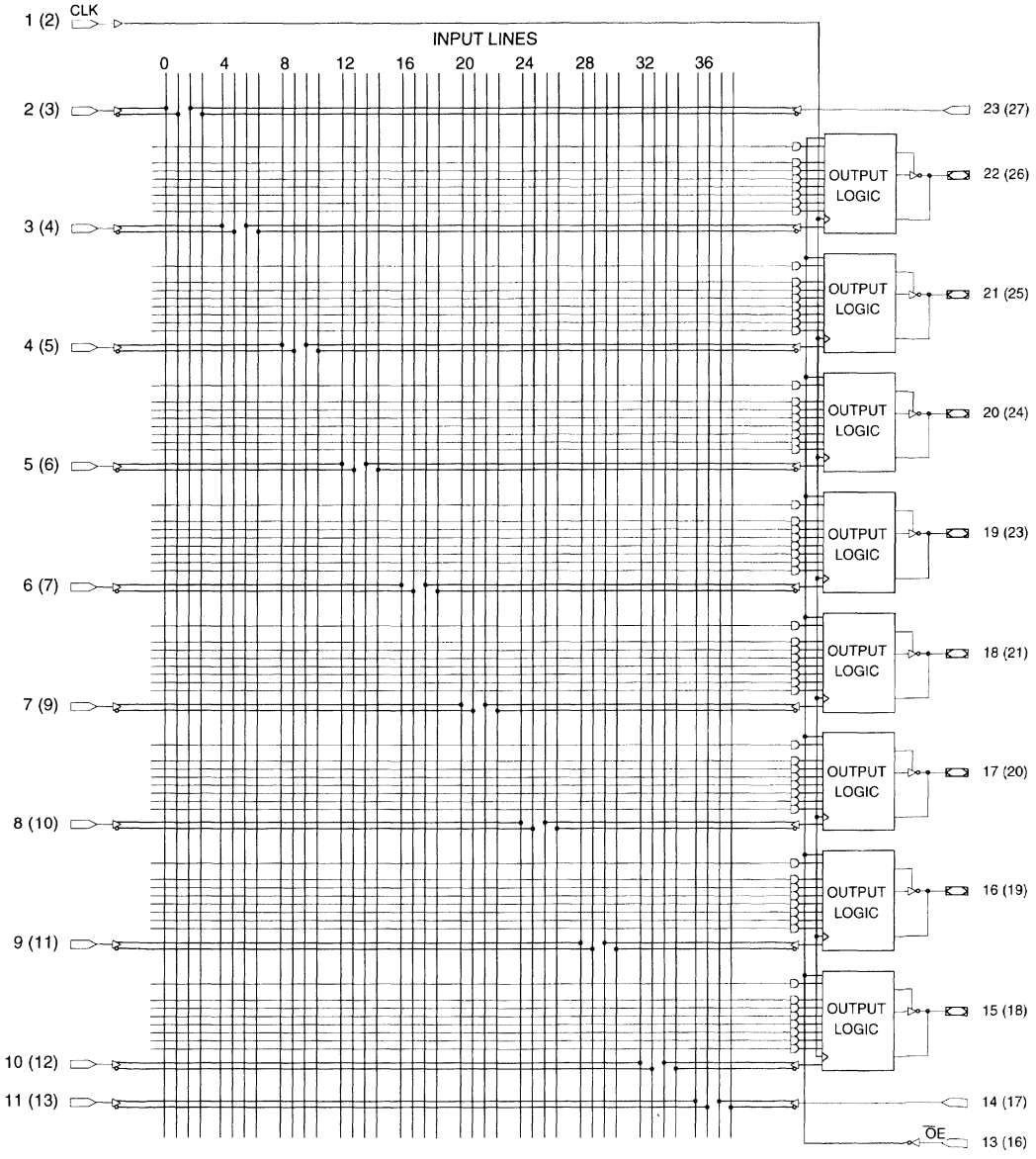
20R6 20RP6

20R4 20RP4

Registered Mode Option



Registered Mode Logic Diagram



ATF20V8B Complex Mode

PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

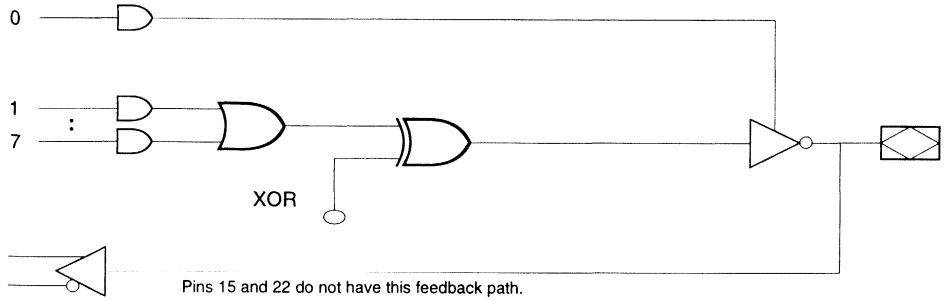
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

20L8

20H8

20P8

Complex Mode Option



ATF20V8B Simple Mode

PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

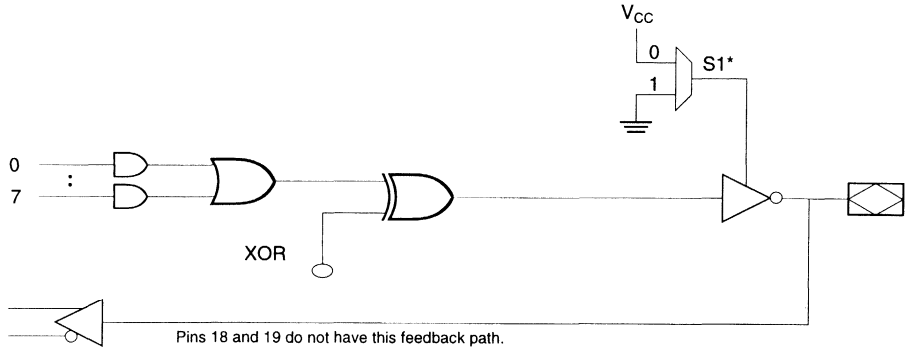
14L8 14H8 14P8

16L6 18H6 16P6

18L4 18H4 18P4

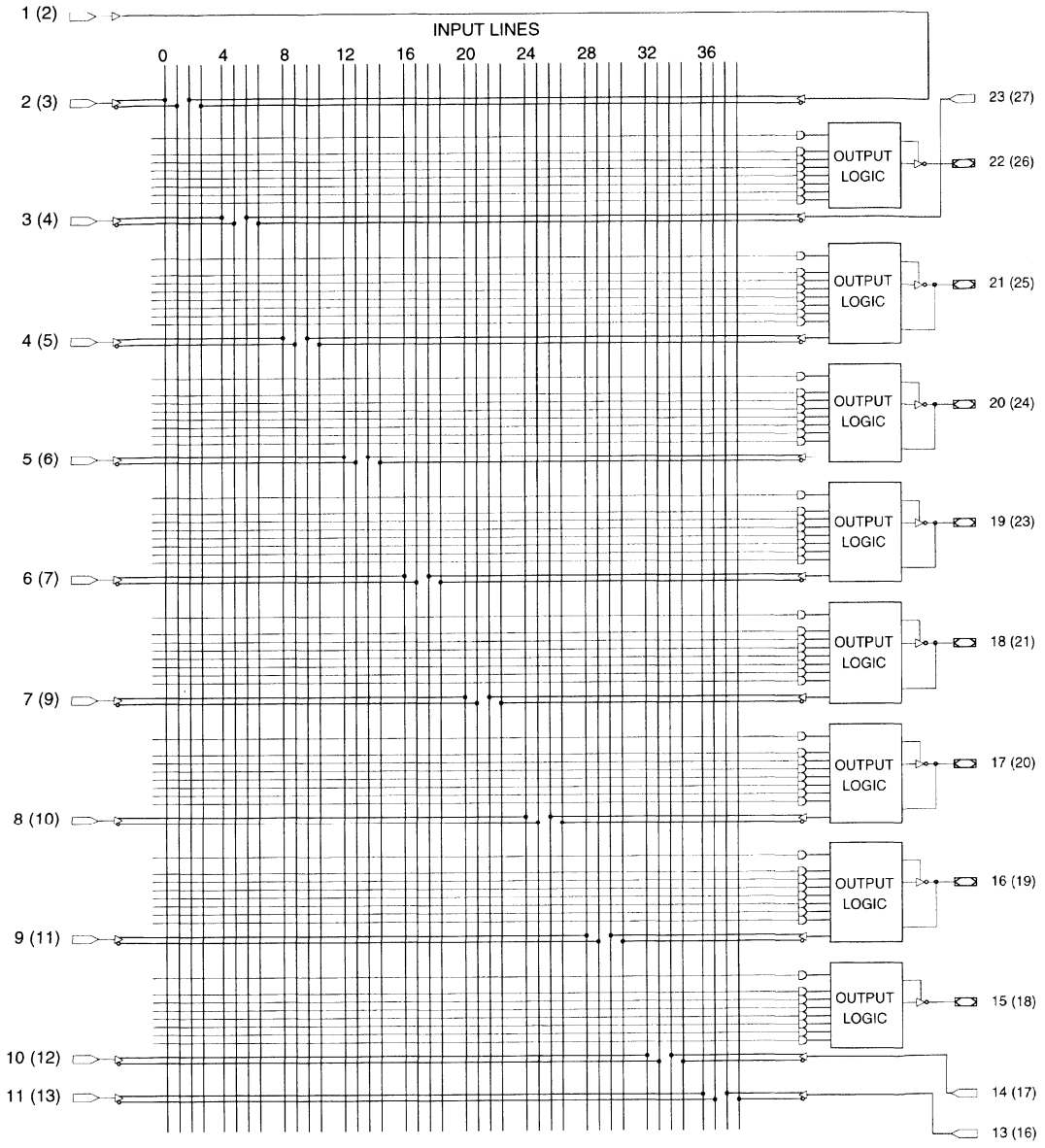
20L2 20H2 20P2

Simple Mode Option

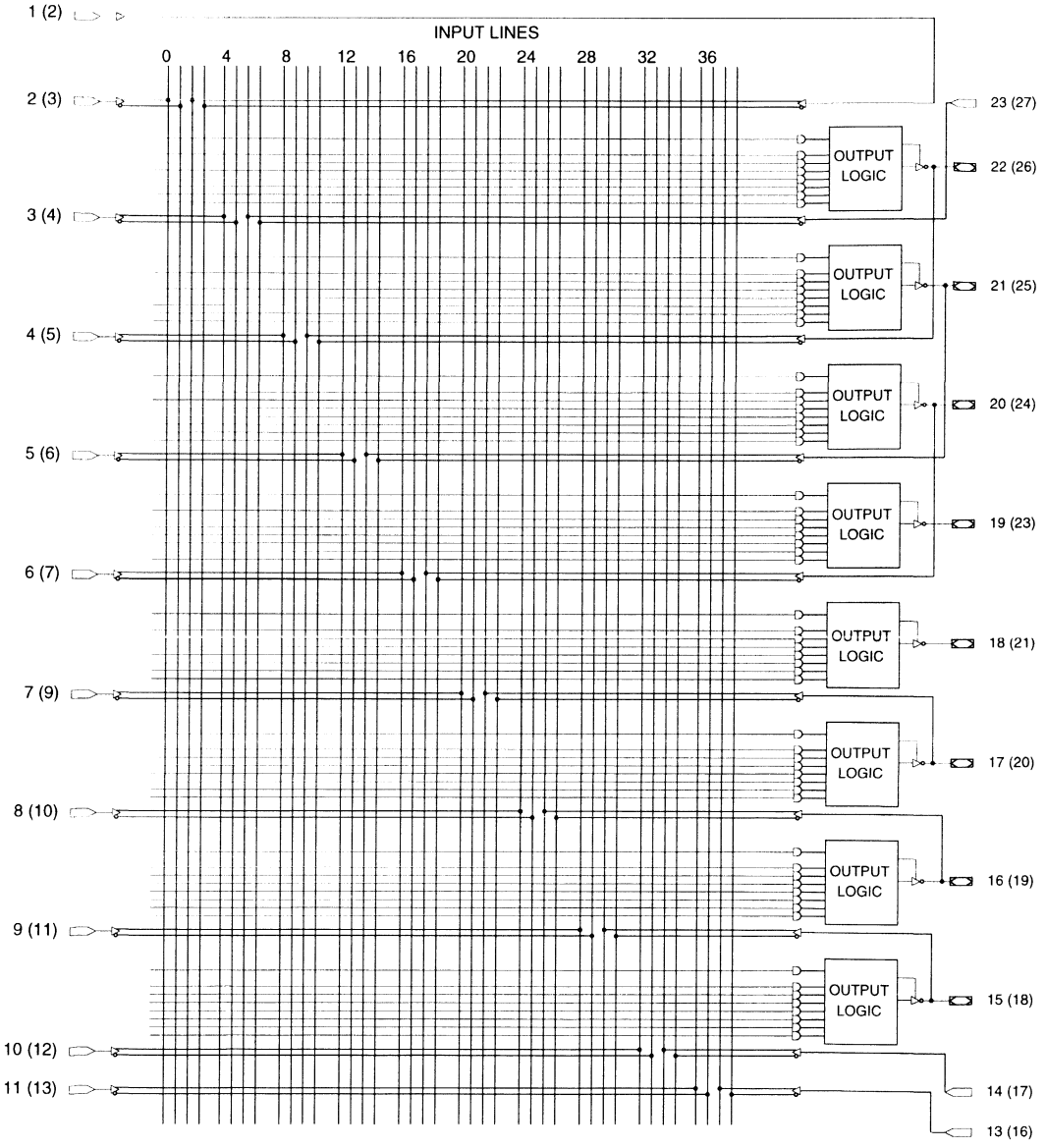


* - Pins 18 and 19 are always enabled.

Complex Mode Logic Diagram

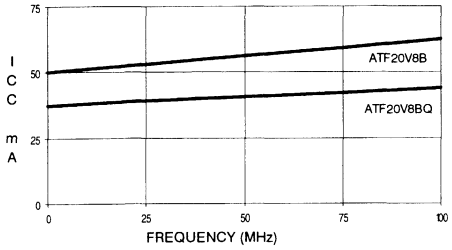


Simple Mode Logic Diagram



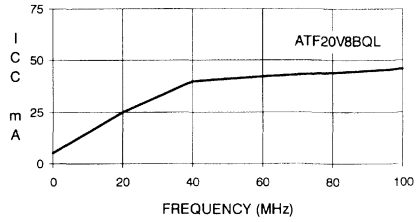
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF20V8B/BQ (VCC=5V, TA=25°C)



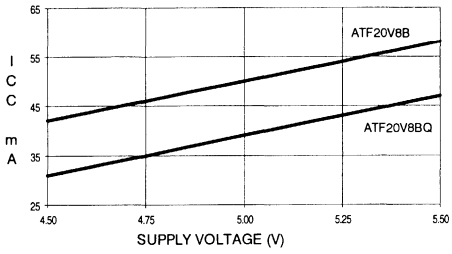
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF20V8BQL (VCC=5V, TA=25°C)



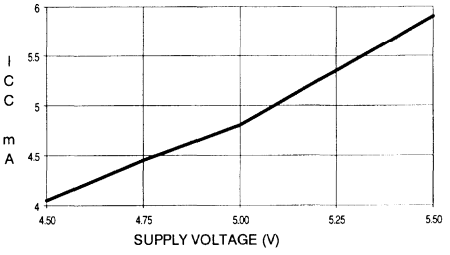
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF20V8B/BQ (VCC=5V, TA=25°C)



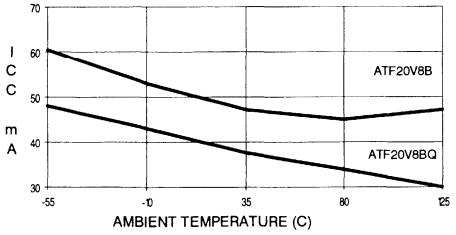
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF20V8BL/BQL (TA=25°C)



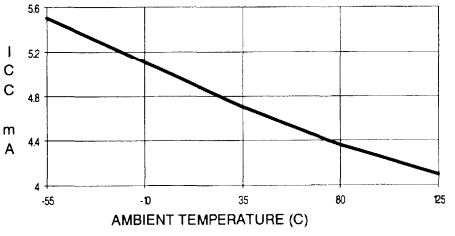
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF20V8B/BQ (VCC=5V)



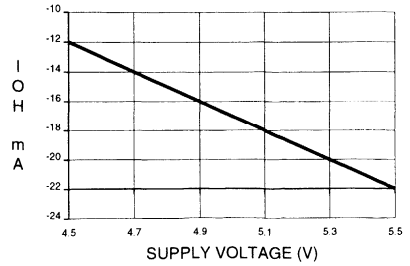
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF20V8BL/BQL (VCC=5V)



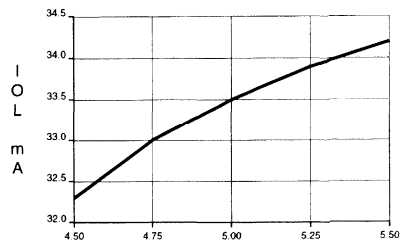
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



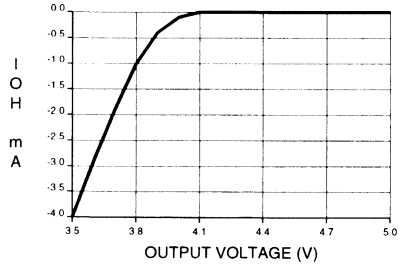
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



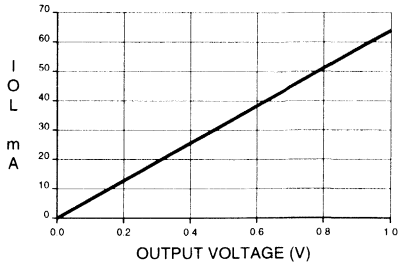
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



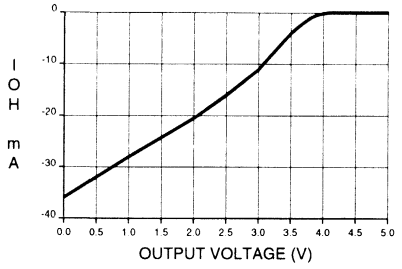
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



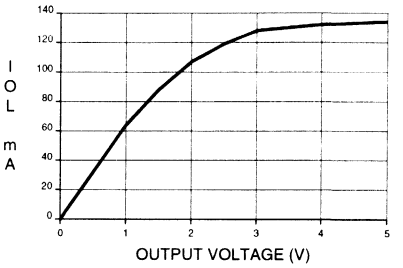
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



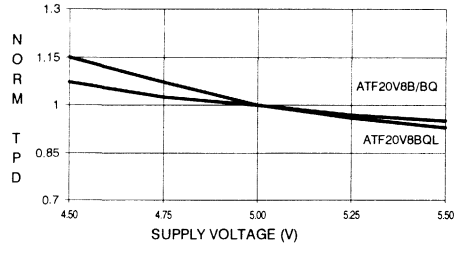
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



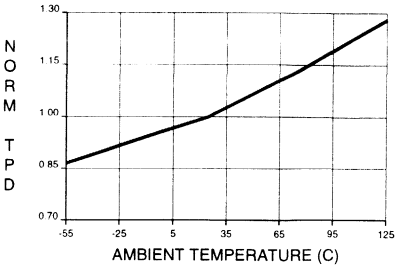
NORMALIZED TPD

vs. SUPPLY VOLTAGE (TA=25°C)



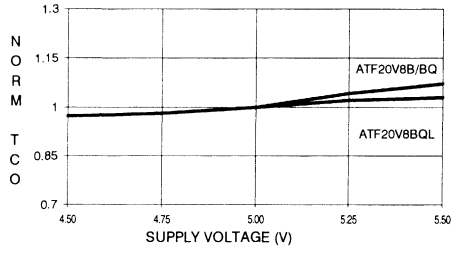
NORMALIZED TPD

vs. AMBIENT TEMPERATURE (VCC = 5V)



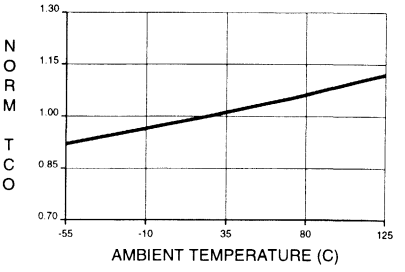
NORMALIZED TCO

vs. SUPPLY VOLTAGE (TA=25°C)

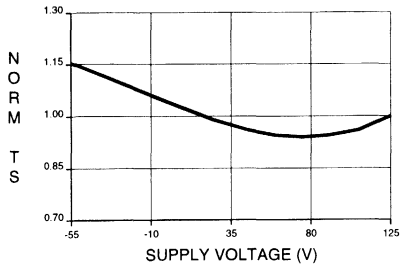


NORMALIZED TCO

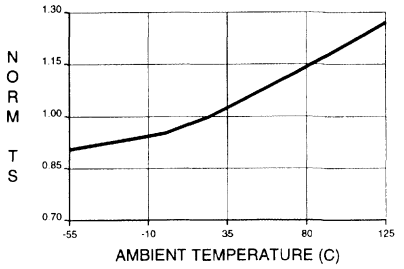
vs. AMBIENT TEMPERATURE (VCC = 5V)



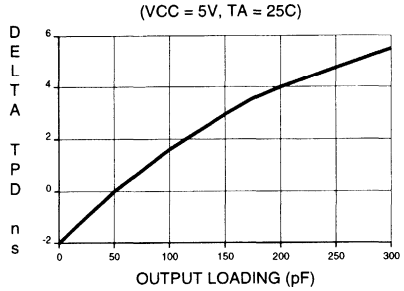
NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)



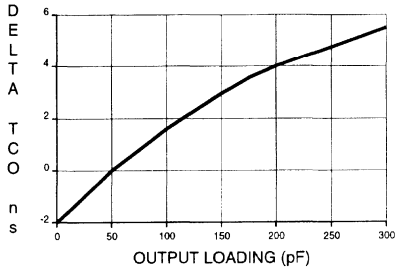
NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)



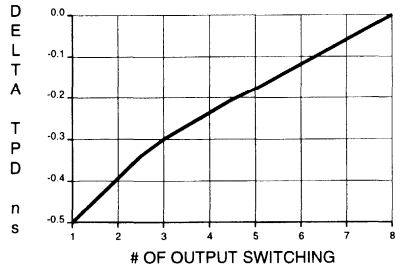
DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



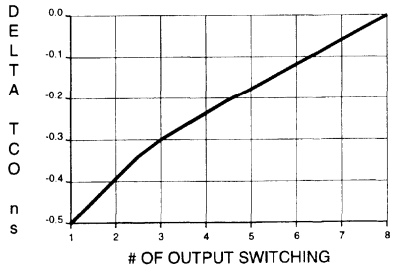
DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



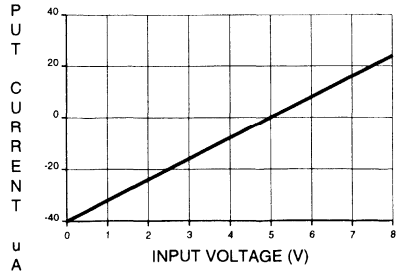
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



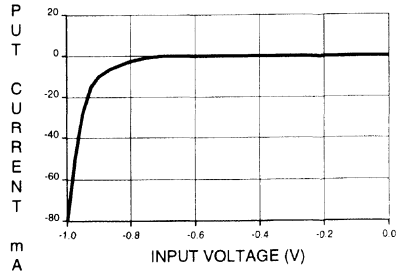
DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	5	5	ATF20V8B-7JC ATF20V8B-7PC ATF20V8B-7SC	20J 20P3 20S	Commercial (0°C to 70°C)
10	7.5	7	ATF20V8B-10JC ATF20V8B-10PC ATF20V8B-10SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF20V8B-10JI ATF20V8B-10PI ATF20V8B-10SI	20J 20P3 20S	Industrial (-40°C to 85°C)
15	12	10	ATF20V8B-15JC ATF20V8B-15PC ATF20V8B-15SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF20V8B-15JI ATF20V8B-15PI ATF20V8B-15SI	20J 20P3 20S	Industrial (-40°C to 85°C)
25	15	12	ATF20V8B-25JC ATF20V8B-25PC ATF20V8B-25SC	20J 20P3 20S	Commercial (0°C to 70°C)
			ATF20V8B-25JI ATF20V8B-25PI ATF20V8B-25SI	20J 20P3 20S	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	7.5	7	ATF20V8BQ-10JC ATF20V8BQ-10PC	28J 24P3	Commercial (0°C to 70°C)
15	12	10	ATF20V8BQL-15JC ATF20V8BQL-15PC ATF20V8BQL-15SC	28J 24P3 24S	Commercial (0°C to 70°C)
25	15	12	ATF20V8BQL-25JC ATF20V8BQL-25PC ATF20V8BQL-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATF20V8BQL-25JI ATF20V8BQL-25PI ATF20V8BQL-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)

Package Type	
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

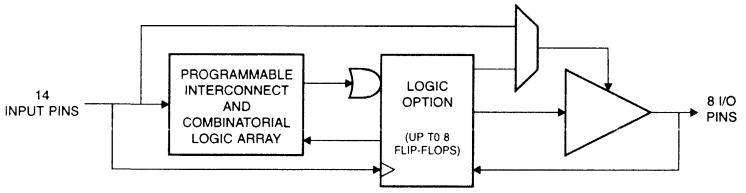
Features

- User-Controlled Power Down Pin
- High Speed Equivalent of ATF20V8B
- Pin-Controlled Zero Standby Power (10 µA Typical) Option
- Industry Standard Architecture
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

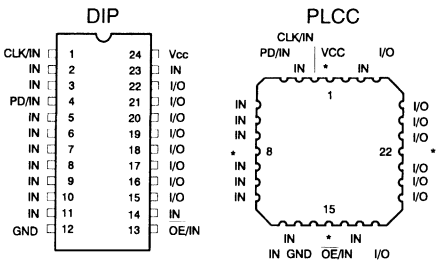
The ATF20V8C is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% for commercial ranges.

The ATF20V8C provides a high-speed CMOS PLD solution with maximum pin to pin delay of 5 ns. The ATF20V8C also has a user-controlled power down feature, offering "zero" standby power (10 µA typical). The user-controlled power down feature allows the user to

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
OE	Output Enable
*	No Internal Connection
VCC	+5 V Supply
PD	Power Down



0408A

Description (Continued)

manage total system power to meet specific application requirements, enhance reliability all without sacrificing speed. Pin "keeper" circuits on input and output pin reduce static power consumed by pull-up resistors.

The ATF20V8C incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

Functional Description

The ATF20V8C macrocell can be configured in one of three different modes. Each mode makes the ATF20V8C look like a different device. The ATF20V8C can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20V8C has a user controlled power down pin which, when active, allows the user to place the device into a "zero" standby power power down mode. The device can also operate at high speed. Maximum pin-to-pin delays of 5 ns are offered. Static power loss due to pull-up resistors is eliminated by using input and output pin "keeper" circuits which holds pins to their previous logic levels when idle.

The universal architecture of the ATF20V8C can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20V8C can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20V8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R [2]	GAL20V8_C7 [2]	GAL20V8_C8 [2]	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Not applicable when using pin-controlled PD (Power-down) feature.
2. Only applicable for version 3.4 or lower.

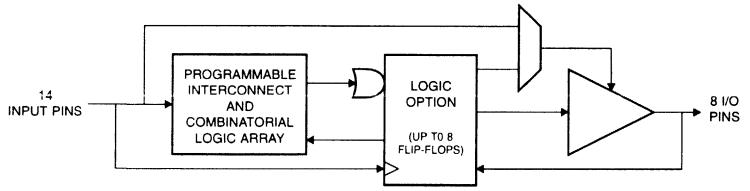
High Performance Flash PLD

Advance Information

Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF20V8B
- Operates down to 2.7 V
- Pin-Controlled Zero Standby Power (10 µA Typical)
- Ideal For Battery Powered Systems
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

Block Diagram



Description

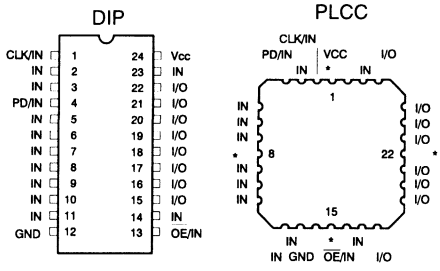
The ATF20LV8C is a low voltage compatible CMOS high performance Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with virtually zero standby power dissipation are offered. All pins offer low ± 10 µA leakage.

The ATF20LV8C provides a low voltage and user-controlled zero power CMOS PLD solution with operating voltages down to 2.7 V. The ATF20LV8C has a user-controlled power down

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply
PD	Power Down



0415A

Description (Continued)

feature, offering "zero" (10 µA typical) standby power. This feature allows the user to manage total system power to meet specific application requirements, enhance reliability, all without sacrificing speed. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors. (The ATF20LV8CZ provides edge-sensing "zero" standby power (10 µA typical), see the ATF20LV8CZ Data Sheet in this Data Book.)

The ATF20LV8C incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3 V ± 5%	3 V ± 10%

Functional Description

The ATF20LV8C macrocell can be configured in one of three different modes. Each mode makes the ATF20LV8C look like a different device. The ATF20LV8C can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20LV8C is capable of operating at supply voltages down to 2.7 V. A user-controlled power down pin is offered which, when active, allows the user to place the device into a "zero" standby power power-down mode thereby further decreasing overall system power consumption. When the power down pin is not used or active, the device operates in a full power low-voltage mode. Static power loss due to pull-up resistors is eliminated by including input and output pin "keeper" circuits which holds pins to their previous logic levels when idle.

The universal architecture of the ATF20LV8C can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20LV8C can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20LV8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R [2]	GAL20V8_C7 [2]	GAL20V8_C8 [2]	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Not applicable when using pin-controlled PD (Power-down) feature.
2. Only applicable for version 3.4 or lower.

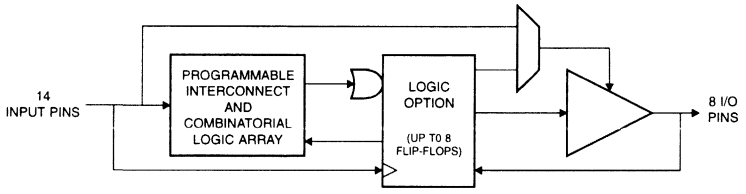
Features

- Edge-Controlled Power Down Pin
- Zero Power Equivalent of ATF20V8B
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Industry Standard Architecture
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 10 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

The ATF20V8CZ is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% range for commercial ranges.

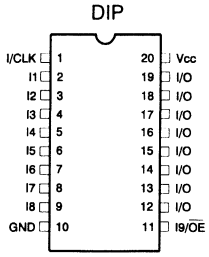
The ATF20V8CZ provides the zero power CMOS PLD solution, with "zero" standby power (10 µA typical). The ATF20V8CZ powers down automatically though Atmel's patented Input

(continued)

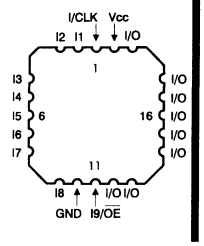
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply

DIP



PLCC



0454A

Description (Continued)

Transition Detection (ITD) circuitry to the "zero" standby power mode when all inputs are idle. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-ups.

The ATF20V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

Functional Description

The ATF20V8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF20V8CZ look like a different device. The ATF20V8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20V8CZ powers down automatically through the ITD circuitry down to a "zero" standby power (10 µA typical) when all inputs are idle. This feature allows the user flexibility to reduce total system power, enhance reliability all without sacrificing speed. Static power loss due to pull-up resistors is reduced through input and output pin "keeper" circuits which holds pins to their previous logic levels when idle.

The universal architecture of the ATF20V8CZ can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20V8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to further decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R (1)	GAL20V8_C7 (1)	GAL20V8_C8 (1)	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Only applicable for version 3.4 or lower.

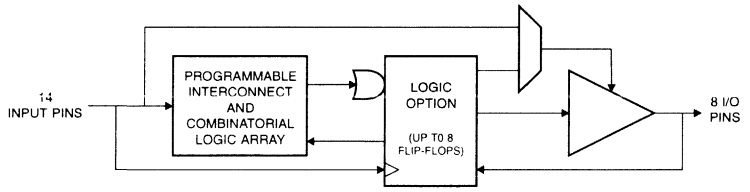
High Performance Flash PLD

Advance Information

Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF20V8B
- Operates down to 2.7 V
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Ideal For Battery Powered Systems
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 5 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

Block Diagram



Description

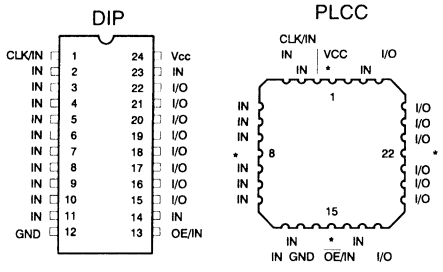
The ATF20LV8CZ is a low voltage compatible CMOS high performance Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with virtually zero standby power dissipation are offered. All pins offer low ± 10 µA leakage.

The ATF20LV8CZ provides a low voltage and user-controlled zero power CMOS PLD solution with operating voltages down to 2.7 V. The ATF20LV8CZ has an edge-sensing power

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply



0416A

Description (Continued)

down feature, offering "zero" (10 µA typical) standby power. This feature allows the user to manage total system power to meet specific application requirements, enhance reliability, all without sacrificing speed. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors. The ATF20LV8CZ provides edge-sensing "zero" standby power (10 µA typical).

The ATF20LV8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3 V ± 5%	3 V ± 10%

Functional Description

The ATF20LV8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF20LV8CZ look like a different device. The ATF20LV8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20LV8CZ is capable of operating at supply voltages down to 2.7 V. It powers down automatically through IDT cicuiting down to "zero" stand-by power (10µA) when all inputs are idle.

The universal architecture of the ATF20LV8CZ can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20LV8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20LV8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection[1]

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R [2]	GAL20V8_C7 [2]	GAL20V8_C8 [2]	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Not applicable when using pin-controlled PD (Power-down) feature.
2. Only applicable for version 3.4 or lower.

1

High Performance Flash PLD

Features

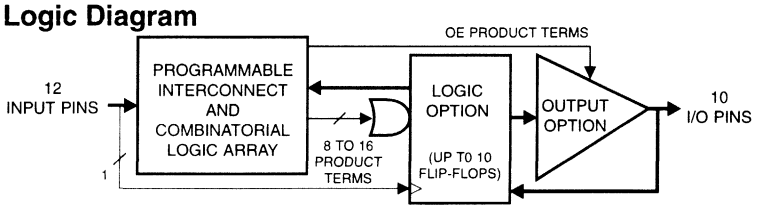
- **Industry Standard Architecture**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Several Power Saving Options**

Device	Icc, Stand-By	Icc, Active
ATF22V10B	85 mA	90 mA
ATF22V10BQ	35 mA	40 mA
ATF22V10BL	5 mA	60 mA
ATF22V10BQL	5 mA	20 mA

= Advance Information

- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

Logic Diagram



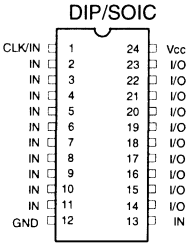
Description

The ATF22V10B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial temperature ranges.

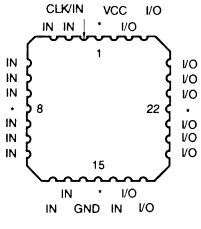
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



LCC/PLCC



0250C

Description (Continued)

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

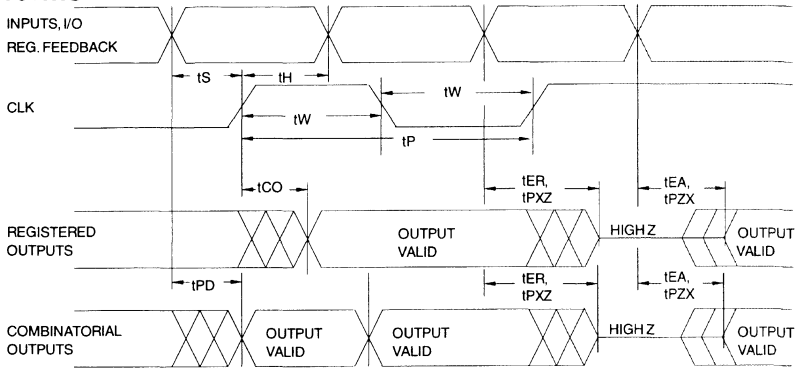
D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}(MAX)$				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		85	120	mA
				Ind., Mil.		85	140	mA
			B-15, -25	Com.		85	120	mA
				Ind., Mil.		85	140	mA
			BQ-15	Com.		35	55	mA
			BL-15, BQL-25	Com.		5	10	mA
				Ind., Mil.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BL-15, BQL-25	Com.		1		mA/MHz(2)
				Ind., Mil.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=15 MHz	B-7, -10	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			B-15, -25	Com.		90	120	mA
				Ind., Mil.		90	140	mA
			BQ-15	Com.		40	55	mA
			BL-15	Com.		60	90	mA
				Ind., Mil.		60	130	mA
			BQL-25	Com.		20	35	mA
				Ind., Mil.		20	40	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com., Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.

☐ = Advance Information

A.C. Waveforms [1]



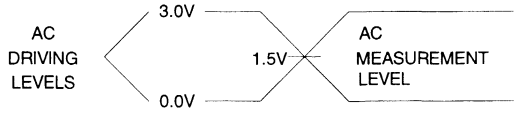
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics [1]

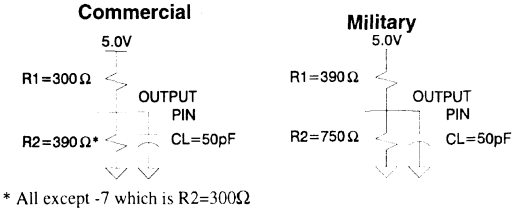
Symbol	Parameter		-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-25 Min	-25 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	7.5	3	10	3	15	3	25	ns
		1 output switching		7							ns
t_{CF}	Clock to Feedback			3		6		8		10	ns
t_{CO}	Clock to Output		2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Setup Time		5		7.5		12		15		ns
t_H	Hold Time		0		0		0		0		ns
t_P	Clock Period		8		12		16		24		ns
t_W	Clock Width		4		6		8		12		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			100		68		45		37	MHz
	Internal Feedback $1/(t_S + t_{CF})$			125		74		50		40	MHz
	No Feedback $1/(t_P)$			125		83		62		41	MHz
t_{EA}	Input to Output Enable — Product Term		3	9	3	10	3	15	3	20	ns
t_{ER}	Input to Output Disable — Product Term		2	9	2	10	2	15	2	20	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable		2	6	2	10	2	15	2	20	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable		1.5	6	1.5	10	1.5	15	1.5	20	ns

Note: 1. See ordering information for valid part numbers and speed grades.

Input Test Waveforms and Measurement Levels



Output Test Loads:



* All except -7 which is R2=300Ω

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

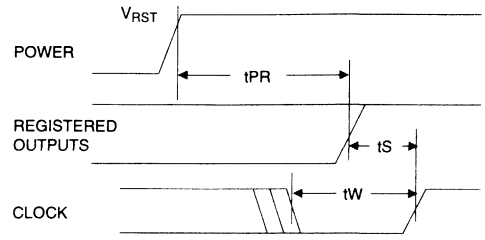
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF22V10Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF22V10B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Electronic Signature Word

There are 64-bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

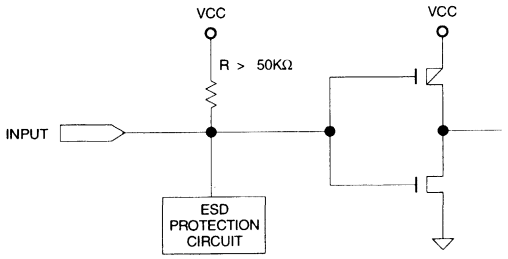
Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

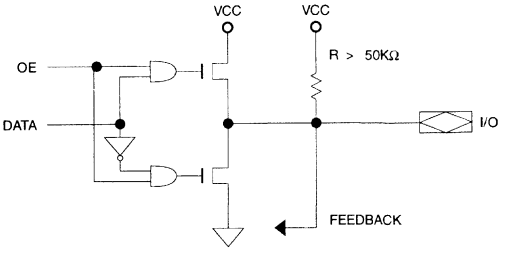
Input and I/O Pull-Ups

All ATF22V10B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

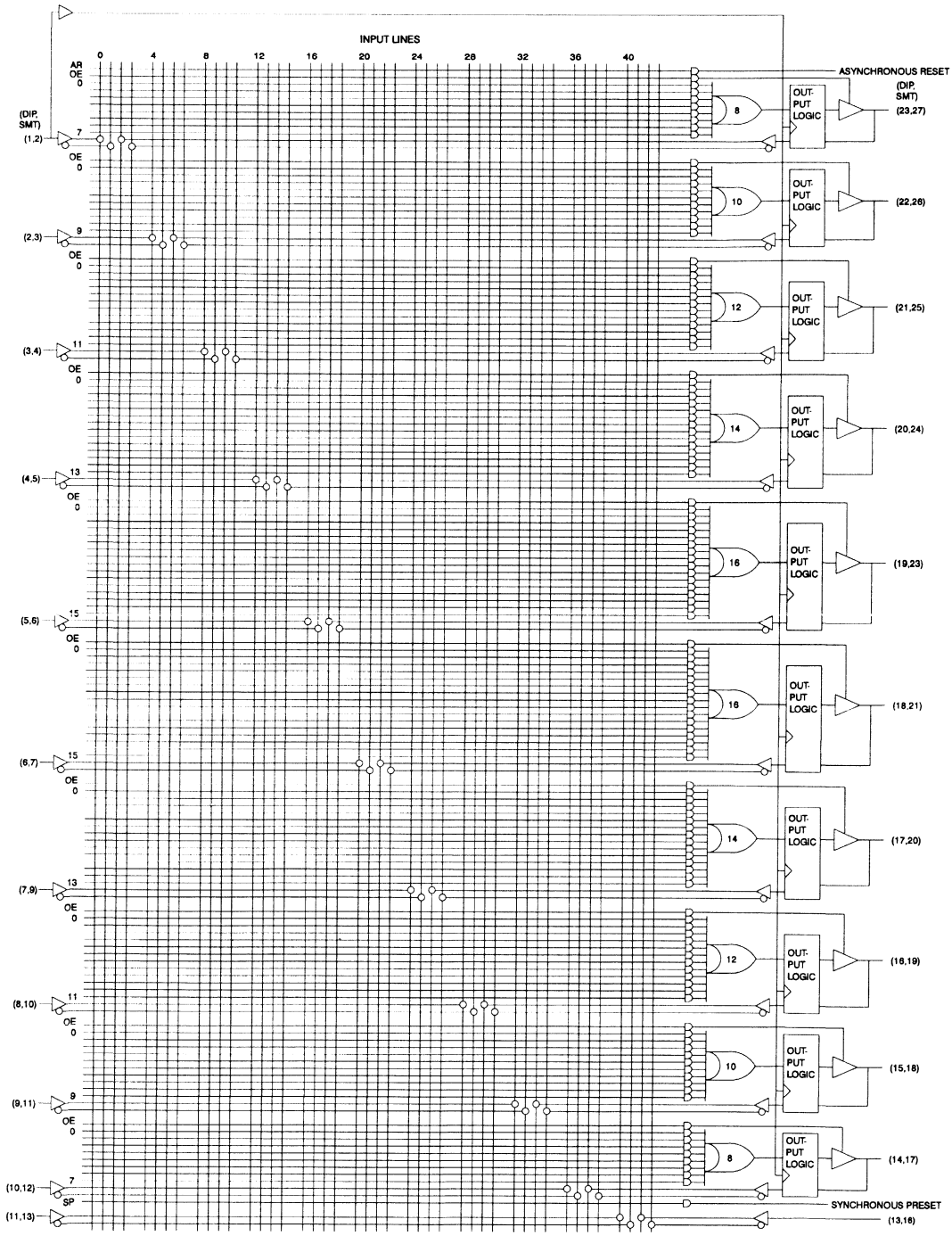
Input Diagram



I/O Diagram

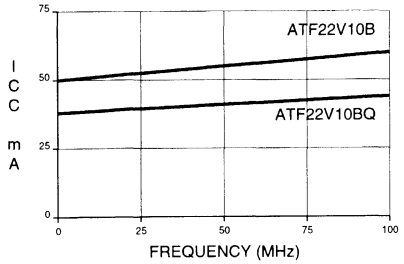


Functional Logic Diagram ATF22V10B/BL



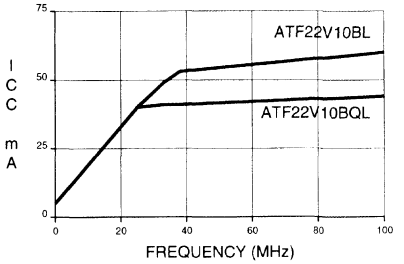
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF22V10B/BQ (VCC = 5V, TA = 25C)



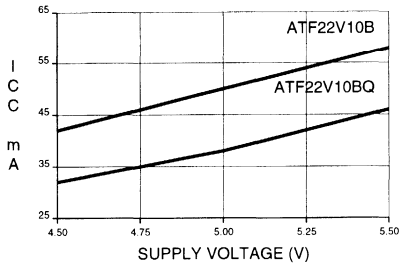
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF22V10BL/BQL (VCC = 5V, TA= 25C)



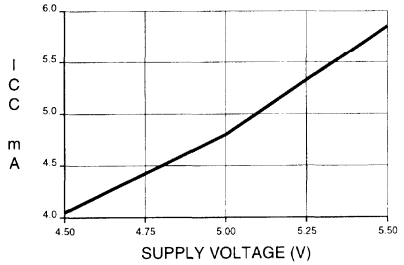
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF22V10B/BQ (TA = 25C)



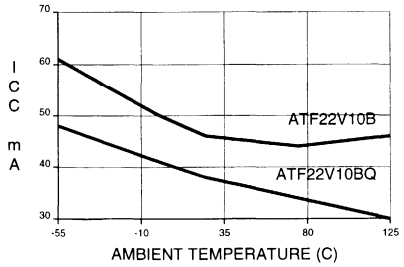
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8BL/BQL (TA = 25C)



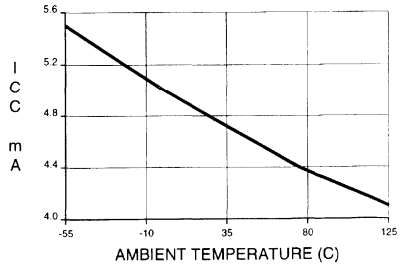
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF22V10B/BQ (VCC = 5V)



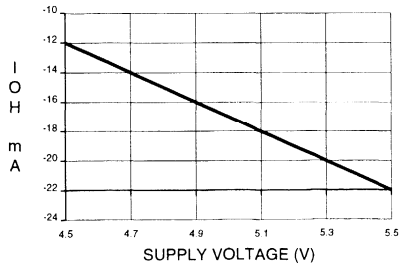
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8BL/BQL (VCC = 5V)



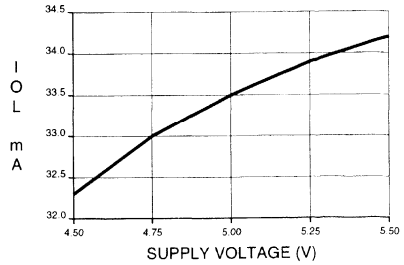
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



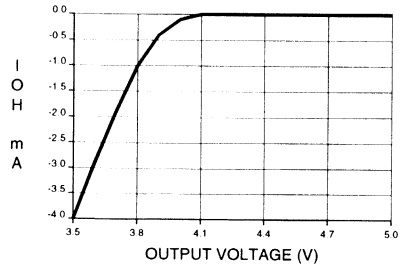
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



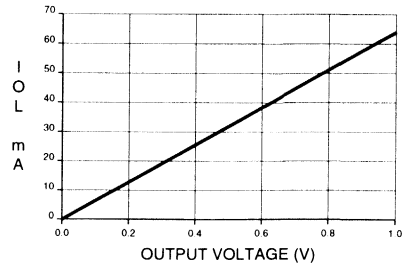
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



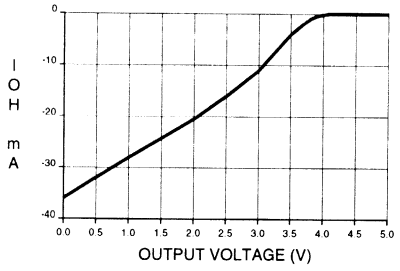
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



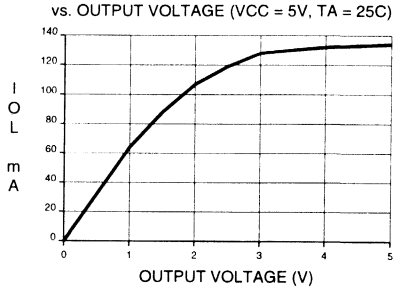
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



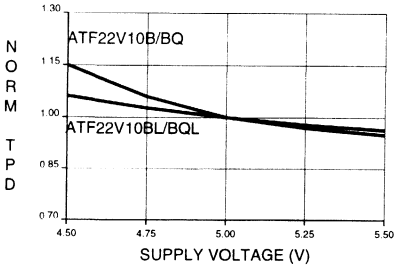
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



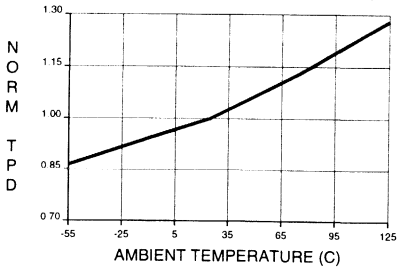
NORMALIZED TPD

vs. SUPPLY VOLTAGE (TA = 25C)



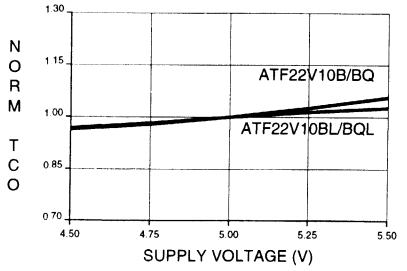
NORMALIZED TPD

vs. AMBIENT TEMPERATURE (VCC = 5V)



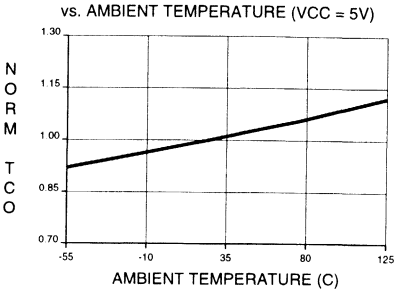
NORMALIZED TCO

vs. SUPPLY VOLTAGE (TA = 25C)

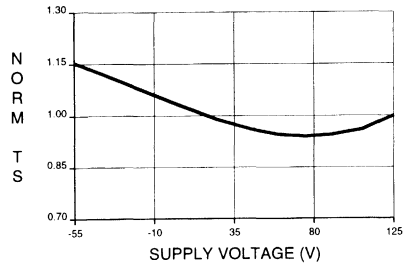


NORMALIZED TCO

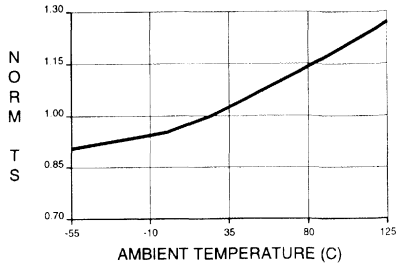
vs. AMBIENT TEMPERATURE (VCC = 5V)



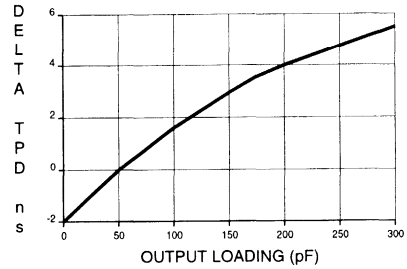
NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)



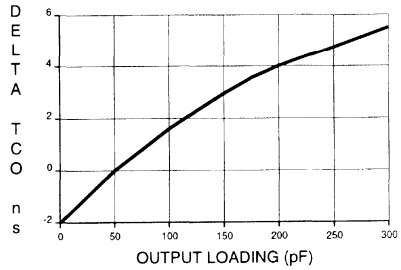
NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)



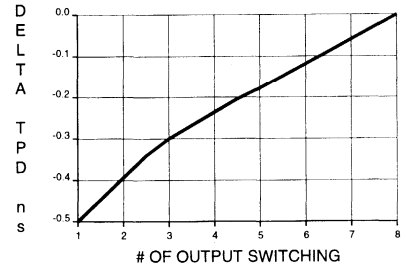
DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



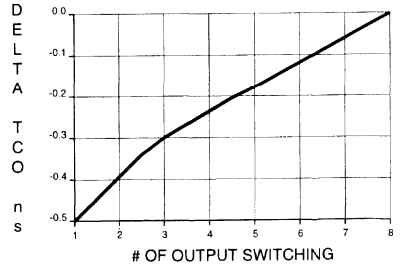
DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



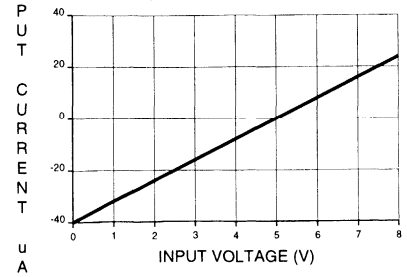
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



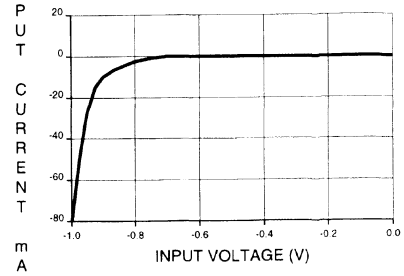
DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	6.5	5	ATF22V10B-7JC ATF22V10B-7PC	24D3 28J	Commercial (0°C to 70°C)
10	7	7	ATF22V10B-10JC ATF22V10B-10PC ATF22V10B-10SC	24D3 28J 24P3	Commercial (0°C to 70°C)
			ATF22V10B-10JI ATF22V10B-10PI ATF22V10B-10SI	24D3 28J 24P3	Industrial (-40°C to 85°C)
			ATF22V10B-10GM/883 ATF22V10B-10NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	8	ATF22V10B-15JC ATF22V10B-15PC ATF22V10B-15SC	24D3 28J 24P3	Commercial (0°C to 70°C)
			ATF22V10B-15JI ATF22V10B-15PI ATF22V10B-15SI	24D3 28J 24P3	Industrial (-40°C to 85°C)
			ATF22V10B-15GM/883 ATF22V10B-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	ATF22V10B-25JC ATF22V10B-25PC ATF22V10B-25SC	24D3 28J 24P3	Commercial (0°C to 70°C)
			ATF22V10B-25JI ATF22V10B-25PI ATF22V10B-25SI	24D3 28J 24P3	Industrial (-40°C to 85°C)
10	7	7	5962-89841 06LA 5962-89841 063X	24D3 28L	Military (-55°C to 125°C Class B, Fully Compliant
15	12	8	5962-89841 03LA 5962-89841 033X	24D3 28L	Military (-55°C to 125°C Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	12	12	5962-89841 05LA 5962-89841 053X	24D3 28L	Military (-55°C to 125°C Class B, Fully Compliant
25	18	20	5962-89841 04LA 5962-89841 043X	24D3 28L	Military (-55°C to 125°C Class B, Fully Compliant
15	10	8	ATF22V10BL-15JC ATF22V10BL-15PC ATF22V10BL-15SC	24D3 28J 24P3	Commercial (0°C to 70°C)
			ATF22V10BL-15JI ATF22V10BL-15PI ATF22V10BL-15SI	24D3 28J 24P3	Industrial (-40°C to 85°C)
			ATF22V10BL-15GM/883 ATF22V10BL-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	12	10	ATF22V10BQ-15JC ATF22V10BQ-15PC	28J 24P3	Commercial (0°C to 70°C)
25	15	12	ATF22V10BQL-25JC ATF22V10BQL-25PC ATF22V10BQL-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATF22V10BQL-25JI ATF22V10BQL-25PI ATF22V10BQL-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF22V10BQL-25GM/883 ATF22V10BQL-25NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

= Advance Information

Package Type	
24D3	24 Lead, 0.300" Wide, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28L	28 Pad, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

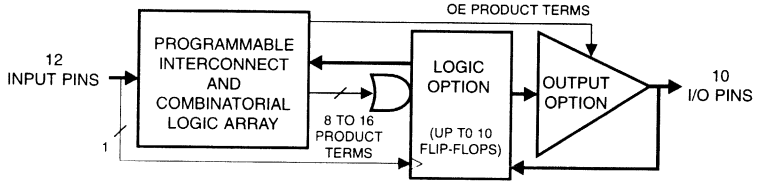
Features

- User-Programmable Power Down Pin
- High Speed Equivalent of ATF22V10B
- Pin-Controlled Zero Standby Power (10 µA Typical)
- Ideal for Battery Powered Systems
  - Low-Cost, Easy-To-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Device
  - 5 ns Max Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Technology
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Full Military, Commercial and Industrial Temperature Ranges
- Dual-In-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Logic Diagram



Description

The ATF22V10C is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) that utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and "zero" standby power dissipation are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial ranges.

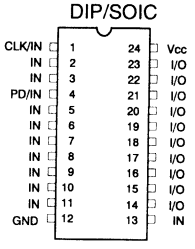
The ATF22V10C provides a high-speed CMOS PLD solution with maximum pin to pin delays of 5 ns. The ATF22V10C has a user-controlled power down feature, offering "zero" standby power. (10 µA typical) The user-controlled power down feature allow the user to manage total system power to meet specific application requirements, enhance reliability, all without sacrificing speed.

(continued)

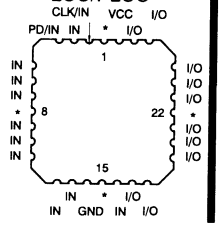
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply
PD	Power Down

DIP/SOIC



LCC/PLCC



0417A

Description (Continued)

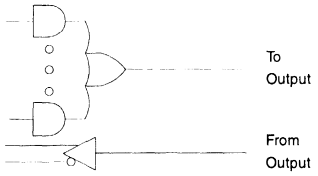
A power down pin allows the user to place the device into a "zero" standby power power-down mode whenever active. When the power down pin is not used or active, the device operates in a full power high-speed mode. Pin "keeper" circuits holds input and output pins to the previous output levels when idle. This can reduce static power consumed by pull-up resistors.

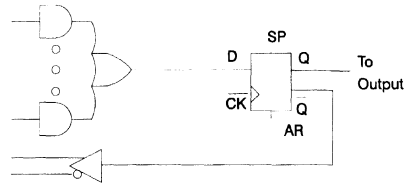
The ATF22V10C macrocell incorporates a variable product term architecture. each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All register are automatically cleared upon power up.

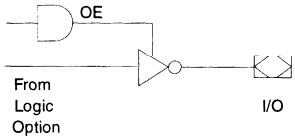
Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

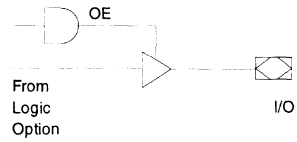
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

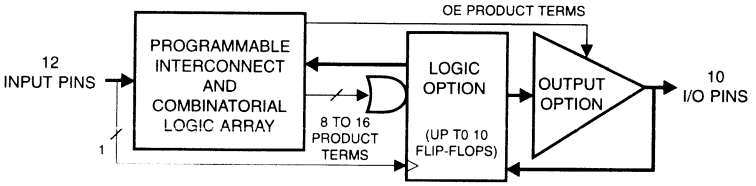
Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF22V10B
- Wide Supply Range 2.7 V to 5.5 V
- Pin-Controlled Zero Standby Power (10 µA Typical)
- Ideal for Battery Powered Systems
  - Low-Cost, Easy-To-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Device
  - 5 ns Max Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Technology
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Full Military, Commercial and Industrial Temperature Ranges
- Dual-In-Line and Surface Mount Packages in Standard Pinouts
- Virtually Zero Standby Power

High Performance Flash PLD

Advance Information

Logic Diagram



Description

The ATF22LV10C is a low voltage compatible CMOS high performance Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with "zero" standby power dissipation are offered. All speed ranges are specified oven the 2.7 V to 5.5 V range. All pins offer low ± 10 µA leakage.

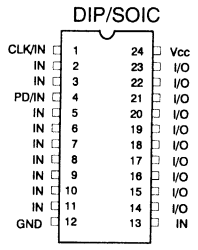
The ATF22LV10C provides the low voltage and user-controlled zero power CMOS PLD solution. A user-controlled power down feature, offers "zero" (10 µA typical) standby power. This feature allows the user to manage total system power to meet specific application requirements, enhance reliability, without sacrificing speed. (The ATF22LV10CZ provides

(continued)

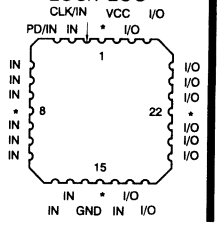
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply
PD	Power Down

DIP/SOIC



LCC/PLCC



0418A

Description (Continued)

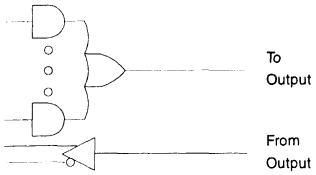
edge-sensing "zero" standby power (10 µA typical), see the ATF22LV10CZ Data Sheet in this Data Book.)

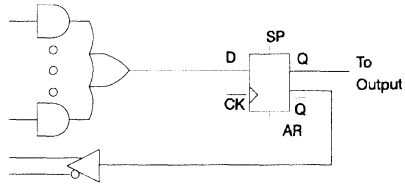
The ATF22LV10C is capable of operating at supply voltages down to 2.7 V. When the power down pin is active the device is placed into a zero standby power power-down mode. When the power down pin is not used or active, the device operates in a full power low voltage mode. Pin "keeper" circuits on the input and output pins hold pin to their previous logic level when idle. This can reduce static power consumed by pull-up resistors.

The ATF22LV10C macrocell incorporates a variable product term architecture. each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

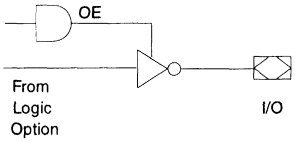
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

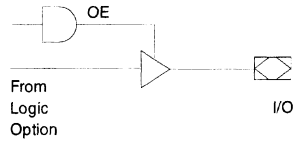
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	3 V ± 10%	3 V ± 10%	3 V ± 10%

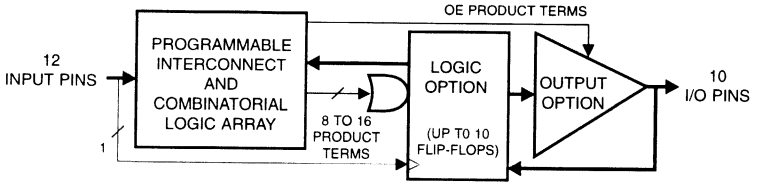
Features

- Edge-Controlled Power Down Pin
- Zero Power Equivalent of ATF22V10B
- Edge-Sensing Zero Standby power (10 µA Typical)
- Industry Standard Architecture
  - Low-Cost, Easy-To-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Device
  - 5 ns Max Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Technology
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Full Military, Commercial and Industrial Temperature Ranges
- Dual-In-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Logic Diagram



Description

The ATF22V10CZ is a high performance CMOS (electrically erasable) Programmable Logic Device (PLD) that utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and "zero" standby power dissipation are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial ranges.

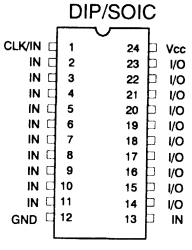
The ATF22V10CZ provides the zero power CMOS PLD solution, with "zero" standby power (10 µA typical). The ATF22V10CZ powers down automatically to the zero power mode though Atmel's patented Input Transition Detection (ITD) circuitry when the device is idle.

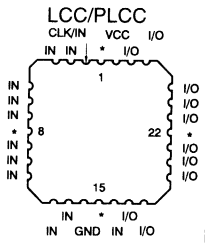
The ITD circuitry feature allows the user flexibility to reduce total system power, and enhance reliability all without sacrificing speed. Pin "keeper" circuits on input and output pins hold

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply





0420A

Description (Continued)

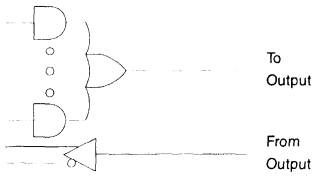
pins to their previous logic levels when idle. This can reduce static power consumed by pull-up resistors.

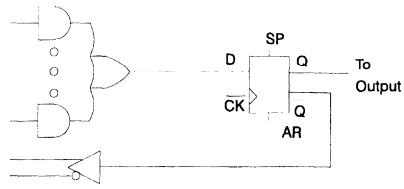
The ATF22V10CZ macrocell incorporates a variable product term architecture each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

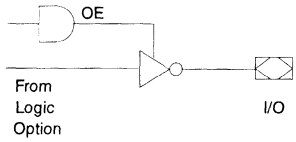
Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

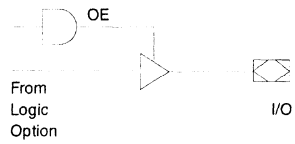
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

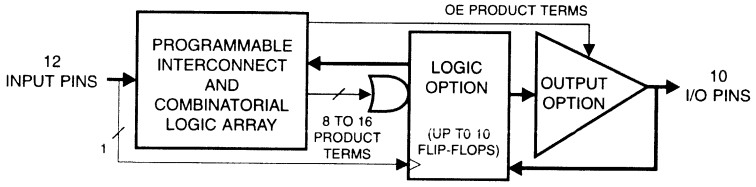
Features

- User-Controlled Power Down Pin
- Low Voltage Equivalent of ATF22V10B
- Wide Supply Range 2.7 V to 5.5 V
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Ideal for Battery Powered Systems
  - Low-Cost, Easy-To-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Device
  - 5 ns Max Propagation Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Technology
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Full Military, Commercial and Industrial Temperature Ranges
- Dual-In-Line and Surface Mount Packages in Standard Pinouts
- Virtually Zero Standby Power

High Performance Flash PLD

Advance Information

Logic Diagram



Description

The ATF22LV10CZ is a low voltage compatible CMOS high performance Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns with "zero" standby power dissipation are offered. All speed ranges are specified oven the 2.7 V to 5.5 V range. All pins offer low ± 10 µA leakage.

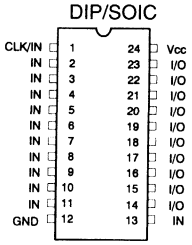
The ATF22LV10CZ provides the low voltage and edge-sensing zero power CMOS PLD solution with 10 µA typical stand-by power.

(continued)

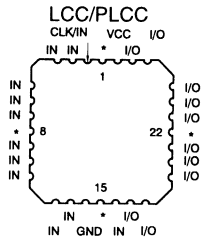
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



LCC/PLCC



0419A

Description (Continued)

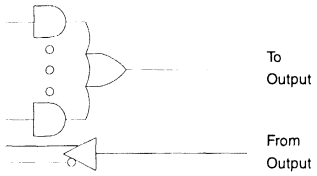
The ATF22LV10CZ is capable of operating at supply voltages down to 2.7 V. It powers-down automatically through IDT circuiting down to "zero" stand-by power (10µA) when all inputs are idle. The device operates in a full power low voltage mode. Pin "keeper" circuits on the input and output pins hold pin to their previous logic level when idle. This can reduce static power consumed by pull-up resistors.

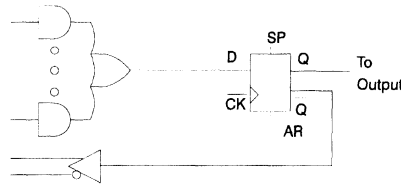
The ATF22LV10CZ macrocell incorporates a variable product term architecture. each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

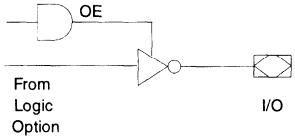
Register Preload simplifies testing. A Security Fuse prevents unauthorized copying of programmed fuse patterns.

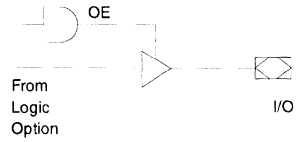
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	3 V ± 10%	3 V ± 10%	3 V ± 10%

Features

- **High Density, High Performance Electrically Erasable Complex Programmable Logic Device**
  - **44-pin, 32 I/O CPLD**
  - **7.5 ns Maximum Pin-to-Pin Delay**
  - **Registered Operation Up To 125 MHz**
  - **Fully Connected Input and Feedback Logic Array**
- **Flexible Logic Macrocell**
  - **D/T / Latch Configurable Flip Flops**
  - **Global and Individual Register Control Signals**
  - **Global and Individual Output Enable**
  - **Programmable Output Slew Rate**
- **Advanced Power Management Features**
  - **Automatic 2 mA Stand-By (ATF1500L)**
  - **Pin-Controlled 10 µA Stand-By Mode**
  - **Bus-friendly Pin-Keeper Inputs and I/Os**
- **Available in Commercial and Industrial Temperature Ranges**
- **Available in 44-pin PLCCs and TQFPs**
- **Advanced Flash Technology**
  - **100% Tested**
  - **Completely Reprogrammable**
  - **100 Program/Erase Cycles**
  - **20 Year Data Retention**
  - **2000 V ESD Protection**
  - **200 mA Latch-Up Immunity**
- **Supported By Popular 3rd Party Tools**

High Performance Flash PLD

Preliminary

Description

The ATF1500 is a high performance, high density Complex PLD. Built on an advanced Flash technology, it has maximum pin to pin delays of 7.5 ns and supports sequential logic operation at speeds up to 125 MHz. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLD's. The ATF1500's global input and feedback architecture simplifies logic placement and eliminates pinout changes due to design changes.

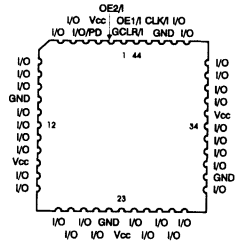
The ATF1500 has 32 bi-directional I/O pins and 4 dedicated input pins. Each dedicated input pin can also serve as a global control signal: register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

(continued)

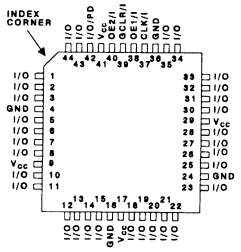
Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
GCLR	Register Reset
OE	Output Enable (active low)
VCC	+5 V Supply
PD	Power Down (active high)

PLCC

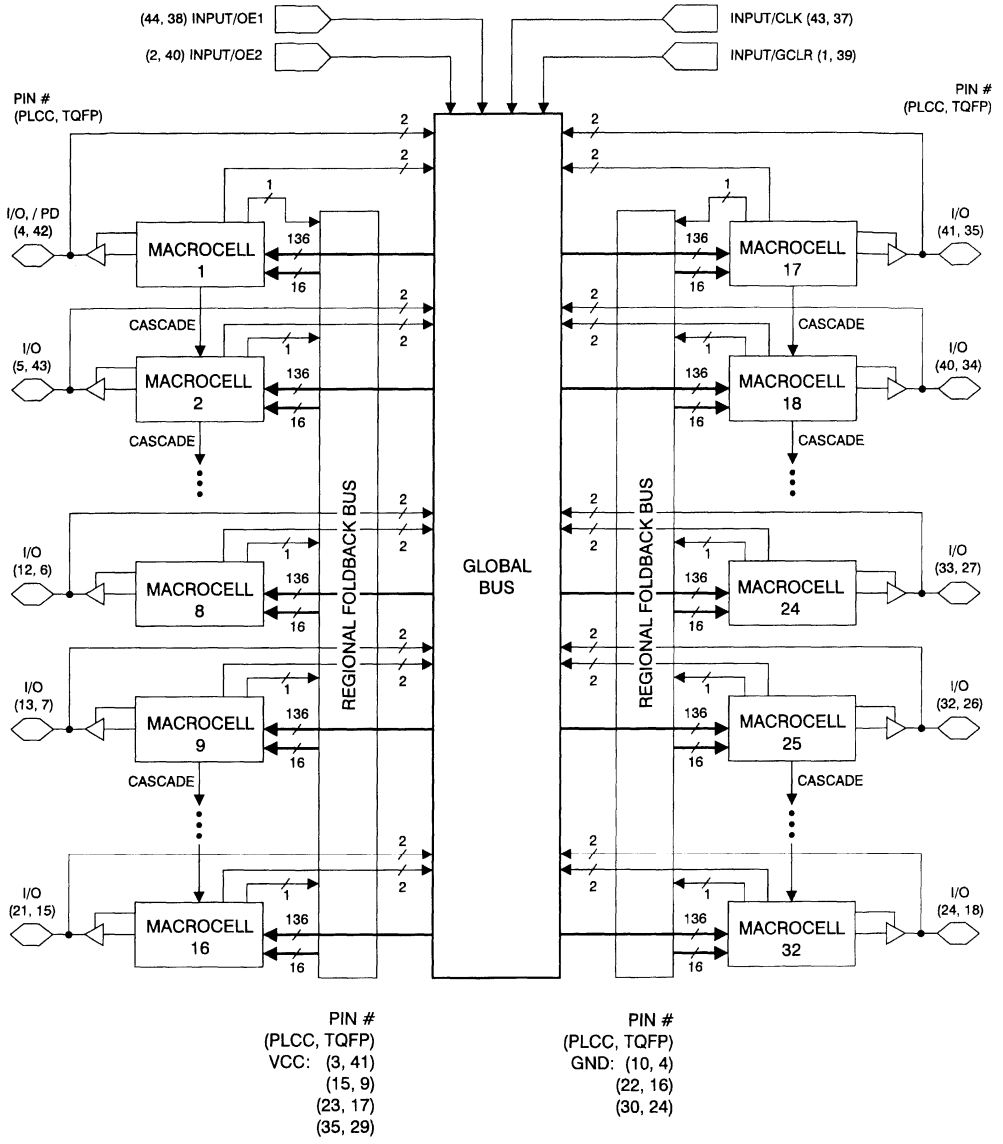


TQFP



0421A

Functional Logic Diagram[1]



Note: 1. Arrows connecting macrocells indicate direction and groupings of CASIN/CASOUT data flow.

Description (Continued)

Each of the 32 logic macrocells generates a buried feedback, which goes to the global bus. Each input and I/O pin also feeds into the global bus. Because of this global bussing, each of these signals is always available to all 32 macrocells in the device.

Each macrocell also generates a foldback logic term, which goes to a regional bus. All signals within a regional bus are connected to all 16 macrocells within the region.

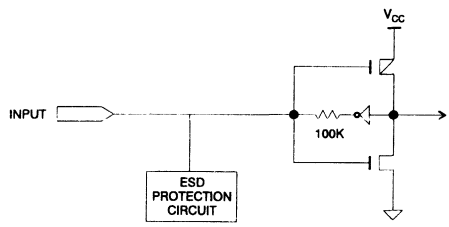
Cascade logic between macrocells in the ATF1500 allows fast, efficient generation of complex logic functions. The ATF1500 contains 4 such logic chains, each capable of creating sum term logic with a fan in of up to 40 product terms.

Bus Friendly Pin-Keeper Input and I/O's

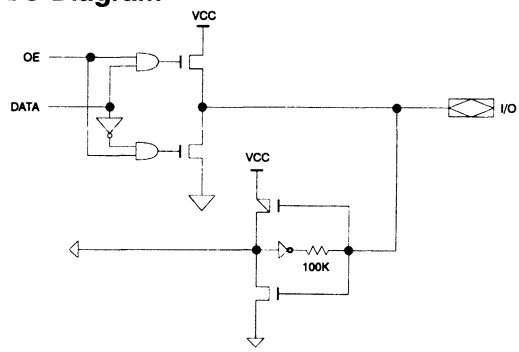
All Input and I/O pins on the ATF1500 have bus friendly "data keeper" circuits. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

This circuitry prevents unused Input and I/O lines from floating to intermediate voltage levels, which cause unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF1500 has several built-in speed and power management features. The ATF1500L contains circuitry that automatically puts the device into a low power stand-by mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides a proportional power savings for most applications running at system speeds below 50 MHz.

All ATF1500s also have an optional pin-controlled power down mode. In this mode, current drops to below 10 µA. When the power down option is selected, the PD pin is used to power down the part. The power down option is selected in the design source file. When enabled, the device goes into power down when the PD pin is high. In the power down mode, all internal logic signals are latched and held, as are any enabled outputs.

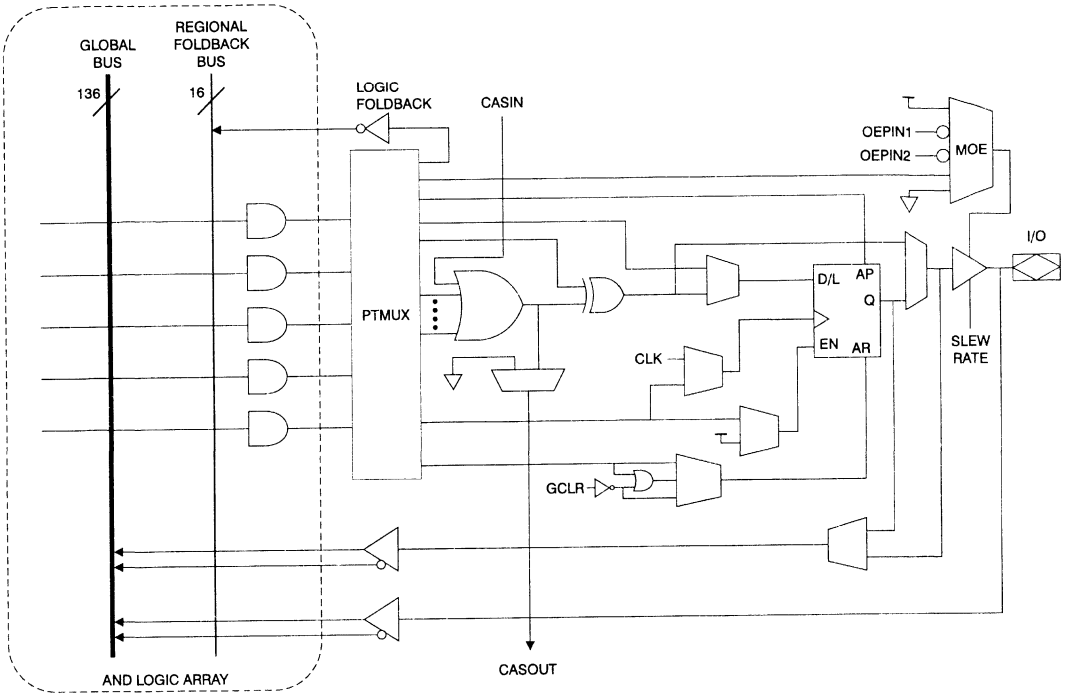
All pin transitions are ignored until the PD is brought low. When the power down feature is enabled, the PD cannot be used as a logic input or output. However, the PD pin's macrocell may still be used to generate buried foldback and cascade logic signals.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design file.

Design Software Support

ATF1500 designs are supported by several 3rd party tools. Automated fitters allow logic synthesis using a variety of high level description languages and formats.

ATF1500 Macrocell



ATF1500 Macrocell

The ATF1500 macrocell is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of 5 sections: product terms and product term select multiplexer; OR/XOR/CASCADE logic; a flip flop; output select and enable; and logic array inputs.

Product Terms and Select Mux

Each ATF1500 macrocell has 5 product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the 5 product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE Logic

The ATF1500 macrocell's OR/XOR/CASCADE logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5 input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with a very small additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high or low level. For combinatorial outputs, the fixed level input allows output polarity selection. For registered functions, the fixed levels allow De Morgan minimization of the product terms. The XOR gate is also used to emulate T- and JK type flip flops.

Flip Flop

The ATF1500's flip flop has very flexible data and control functions. The data input can come from either the XOR gate or from a separate product term. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell.

In addition to D, T, JK and SR operation, the flip flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can be either the global CLK pin or an individual product term. The flip flop changes state on the clock's rising edge. When the CLK pin is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored.

The flip flop's asynchronous reset signal (AR) can be either the pin global clear (GCLR), a product term, or always off. AR can also be a logic OR of GCLR with a product term. The asynchronous preset (AP) can be a product term or always off.

Output Select and Enable

The ATF1500 macrocell output can be selected as registered or combinatorial. When the output is registered, the same registered signal is fed back internally to the global bus. When the output is combinatorial, the buried feedback can be either the same combinatorial signal or it can be the register output if the separate product term is chosen as the flip flop input.

The output enable multiplexer (MOE) controls the output enable signals. Any buffer can be permanently enabled for simple output operation. Buffers can also be permanently disabled to allow use of the pin as an input. In this configuration all the macrocell resources are still available, including the buried feedback, expander and CASCADE logic.

The output enable for each macrocell can also be selected as either of the two OE pins or as an individual product term.

Global/Regional Busses

The global bus contains all Input and I/O pin signals as well as the buried feedback signal from all 32 macrocells. Together with the complement of each signal, this provides a 136 bit bus as input to every product term. Having the entire global bus available to each macrocell eliminates any potential routing problems. With this architecture designs can be modified without requiring pinout changes.

Each macrocell also generates a foldback product term. This signal goes to the regional bus, and is available to 16 macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The 16 foldback terms in each region allow generation of high fan-in sum terms (up to 21 product terms) with a small additional delay.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is Vcc + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

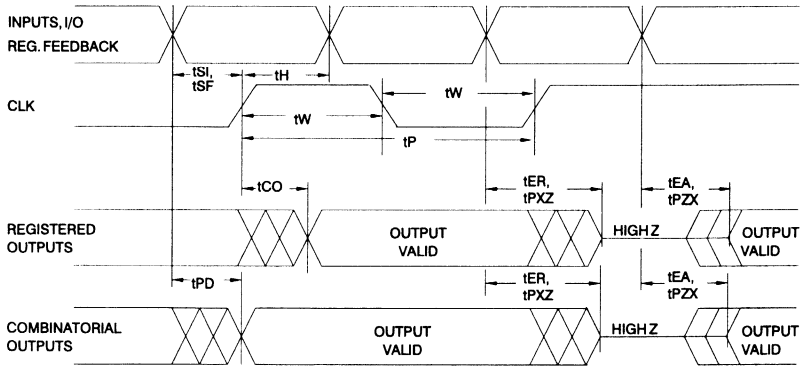
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(max)					-10	µA
I_{IH}	Input or I/O High Leakage Current	V_{IH},min < $V_{IN} \le V_{CC}$					10	µA
I_{CC1}(1)	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = 0, V_{CC}	ATF1500	Com.		70		mA
				Ind.		100		mA
			ATF1500L	Com.			3	mA
				Ind.			5	mA
I_{CC2}(1)	Power Supply Current, Power Down Mode	V_{CC} = MAX, V_{IN} = 0, V_{CC}		Com.			10	µA
				Ind..			15	µA
I_{CC3}(1)	Clocked Power Supply Current	V_{CC} = MAX, V_{IN} = 0, V_{CC}	ATF1500L	Com.		1		mA/MHz
				Ind.		1		mA/MHz
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage	V_{CC}, min < V_{CC} < V_{CC}, max			-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	V_{CC} = MIN	I_{OL} = 8 mA				0.45	V
V_{OH}	Output High Voltage	V_{CC}= MIN	I_{OH} = -4 mA		2.4			V

Note: 1. All I_{CC} parameters measured with outputs open, and a 16-bit loadable, up/down counter programmed into each region.

A.C. Waveforms



Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COS}[1]	Clock to Output		4.5	2	5	2	6	2	8	2	12	ns
t_{CFS}	Clock to Feedback		2		2		2		2		2	ns
t_{SIS}	I, I/O Setup Time		6		8		10		11		13	ns
t_{SFS}	Feedback Setup Time		6		8		10		11		13	ns
t_{HS}	Input, I/O, Feedback Hold Time	0		0		0		0		0		ns
t_{PS}	Clock Period	6		8		9		10		12		ns
t_{WS}	Clock Width	3		4		4.5		5		6		ns
F_{MAXS}	External Feedback $1/(t_{SIS}+t_{COS})$		95		76.9		62.5		52.6		40	MHz
	Internal Feedback $1/(t_{SFS}+t_{CFS})$		125		100		90.9		76.9		66	MHz
	No Feedback $1/(t_{PS})$		166.7		125		125		100		83	MHz
t_{RPRS}	Reset Pin Recovery Time	2		3		3		4		5		ns
t_{RTRS}	Reset Term Recovery Time	6		9		10		12		14		ns

Notes: 1. For slow slew outputs, add t_{SSO}.

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COA}[1]	Clock to Output		7.5		10		12		15		25	ns
t_{CFA}	Clock to Feedback		5		7		7		9		11	ns
t_{SIA}	I, I/O Setup Time	3		3		4		4		5		ns
t_{SFA}	Feedback Setup Time	3		3		4		4		5		ns
t_{HA}	Input, I/O, Feedback Hold Time	2		3		4		4		5		ns
t_{PA}	Clock Period	6		8		10		12		16		ns
t_{WA}	Clock Width	3		4		5		6		8		ns
F_{MAXA}	External Feedback $1/(t_{SIA}+t_{COA})$		95.2		76.9		62.5		52.6		33.3	MHz
	Internal Feedback $1/(t_{SFA}+ t_{CFA})$		125		100		90.9		76.9		62.5	MHz
	No Feedback $1/(t_{PA})$		166.7		125		100		83.3		62.5	MHz
t_{RPRA}	Reset Pin Recovery Time	0		0		0		0		0		ns
t_{RTRA}	Reset Term Recovery Time	4		5		6		6		8		ns

A.C. Characteristics

Symbol	Parameter	-7		-10		-12		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}[1]	I, I/O or FB to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	25	ns
t_{PD2}	I, I/O to Feedback		5		7		8		9		14	ns
t_{PD3}[1]	Feedback to Non-Registered Output	2	7.5	3	10	3	12	3	15	3	25	ns
t_{PD4}	Feedback to Feedback		5		7		8		9		14	ns
t_{EA}[1]	OE Term to Output Enable	2	7.5	3	10	3	12	3	15	3	25	ns
t_{ER}	OE Term to Output Disable	2	7.5	2	10	2	12	2	15	2	25	ns
t_{PZX}[1]	OE Pin to Output Enable	2	5.5	2	7	2	8	2	9	2	11	ns
t_{PXZ}	OE Pin to Output Disable	1.5	5.5	1.5	7	1.5	8	1.5	9	1.5	11	ns
t_{PW}	Preset Width		3		4		4		5		6	ns
t_{PF}	Preset To Feedback		6		9		9		12		20	ns
t_{PO}[1]	Preset to Registered Output		8.5		12		14		20		25	ns
t_{RPW}	Reset Pin Width		3		4		4		5		6	ns
t_{RPF}	Reset Pin to Feedback		3		4		3		5		6	ns
t_{RPO}[1]	Reset Pin to Registered Output		5.5		7		8		11		15	ns
t_{RTW}	Reset Term Width		3		4		4		5		6	ns
t_{RTF}	Reset Term to Feedback		6		9		9		12		20	ns
t_{RTO}[1]	Reset Term to Registered Output		8.5		12		14		20		25	ns
t_{CAS}	Cascade Logic Delay		0.8		0.8		1		1		1.5	ns
t_{SSO}	Slow Slew Output Adder		3		3		3		4		4	ns
t_{FLD}	Foldback Term Delay		4		5		7		8		12	ns

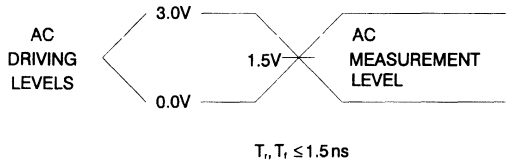
Notes: 1. For slow slew outputs, add t_{SSO}.

Power Down A.C. Characteristics

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-12 Min	-12 Max	-15 Min	-15 Max	-25 Min	-25 Max	Units
t_{IVDH}	Valid I, I/O Before PD High	7		10		12		15		25		ns
t_{GVDH}	Valid OE(2) Before PD High	7		10		12		15		25		ns
t_{CVDH}	Valid Clock(2) Before PD High	7		10		12		15		25		ns
t_{DHIX}	I, I/O Hold After PD High		15		20		22		25		35	ns
t_{DHGX}	OE(2) Hold After PD High		15		20		22		25		35	ns
t_{DHCX}	Clock(2) Hold After PD High		15		20		22		25		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1		1	µs

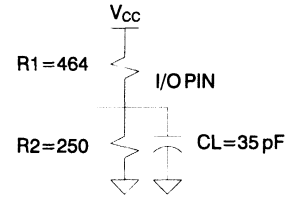
Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or Product Term.

Input Test Waveforms and Measurement Levels:



$T_r, T_f \leq 1.5$ ns

Output Test Load:



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

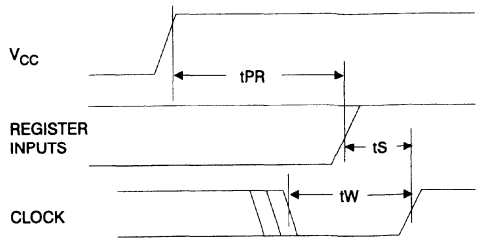
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The ATF1500's registers are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be low on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock signal high, and
3) Signals from which clocks are derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	2	10	µs
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Power Down Mode

The ATF1500 includes an optional pin controlled power down feature. When this mode is enabled, the PD pin acts as the power down pin. When the PD pin is high, the device supply current is reduced to less than 10 µA. During power down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs which were in a HI-Z state at the onset of power down will remain at HI-Z. During power down, all input signals except the power down pin are blocked. Input and I/O hold latches remain active to insure that pins do not float to indeterminate levels, further reducing system power. The power down pin feature is enabled in the logic design file. Designs using the power down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Register Preload

The ATF1500's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with preload vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically when vectors are run by any approved programmers. The preload mode is enabled by raising an input pin to a high voltage level. Contact Atmel PLD Applications for PRELOAD pin assignments, timing and voltage requirements.

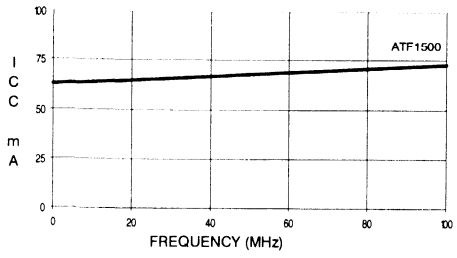
Security Fuse

A single fuse is provided to prevent unauthorized copying of the ATF1500 fuse patterns. Once programmed, fuse verify and preload are inhibited.

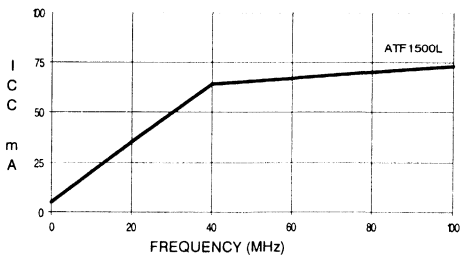
Output Slew Rate Control

Each ATF1500 macrocell contains a configuration bit for each I/O to control its output slew rate. This allows selected data paths to operate at maximum throughput while reducing system noise from outputs that are not speed-critical. Outputs default to slow edges, and may be individually set to fast in the design file. Output transition times for outputs configured as slow have a Tsso delay adder.

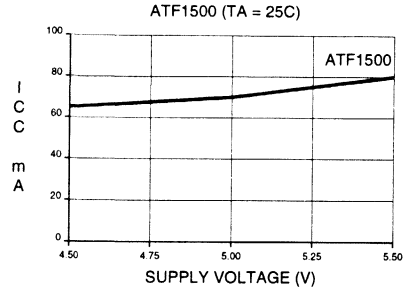
SUPPLY CURRENT vs. INPUT FREQUENCY
ATF1500 (VCC=5V, TA=25°C)



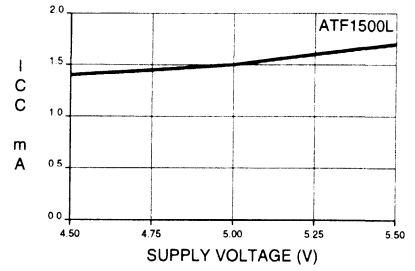
SUPPLY CURRENT vs. INPUT FREQUENCY
ATF1500L (VCC=5V, TA=25°C)



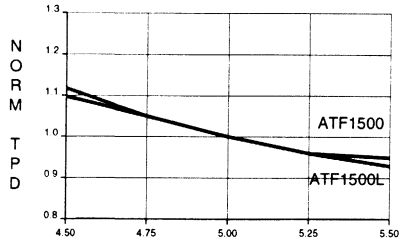
SUPPLY CURRENT vs. SUPPLY VOLTAGE
ATF1500 (TA = 25C)



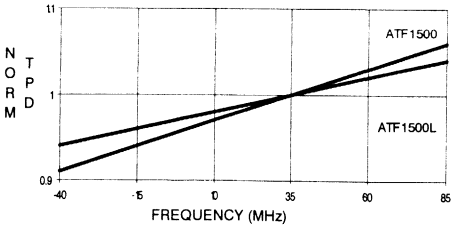
SUPPLY CURRENT vs. SUPPLY VOLTAGE
ATF1500L (TA = 25C)



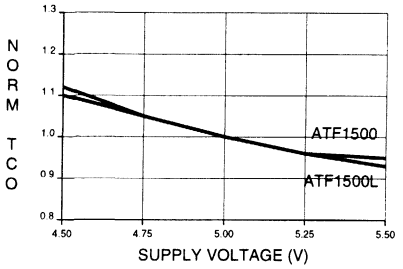
NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA = 25C)



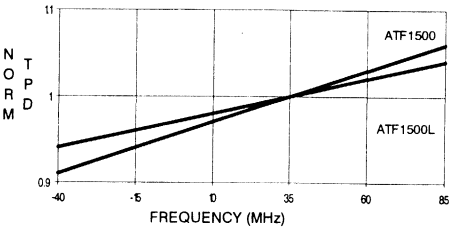
NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC=5V)



NORMALIZED TCO
vs. SUPPLY VOLTAGE (TA = 25C)



NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC=5V)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	F_{MAXS} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	95	ATF1500-7AC ATF1500-7JC	44A 44J	Commercial (0°C to 70°C)
10	5	76.9	ATF1500-10AC ATF1500-10JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500-10JI	44J	Industrial (-40°C to 85°C)
12	6	62.5	ATF1500-12AC ATF1500-12JC	44A 44J	Commercial (0°C to 70°C)
15	8	52.6	ATF1500-15AC ATF1500-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500-15JI	44J	Industrial (-40°C to 85°C)
15	8	52.6	ATF1500L-15AC ATF1500L-15JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500L-15JI	44J	Industrial (-40°C to 85°C)
25	12	40	ATF1500L-25AC ATF1500L-25JC	44A 44J	Commercial (0°C to 70°C)
			ATF1500L-25JI	44J	Industrial (-40°C to 85°C)

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)

High Speed UV Erasable Programmable Logic Device

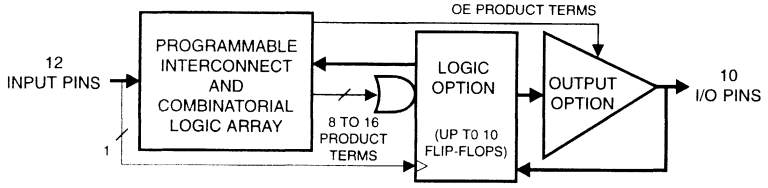
Features

- **High Speed Programmable Logic Device**
  - **15 ns Max Propagation Delay**
  - **5 V ±10% Operation**
- **Low Power CMOS Operation**

Speed	"L"	-15,-20	All
Temp	Com./Mil.	Com./Mil.	Others
Icc(mA)	12/15	90/100	55

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages**

Logic Diagram



Description

The AT22V10 and AT22V10L are CMOS high performance EPROM-based Programmable Logic Devices (PLDs). Speeds down to 15 ns and power dissipation as low as 12 mA are offered. All speed ranges are specified over the full 5 V ±10% range. All pins offer a low ±10 µA leakage.

The AT22V10L provides the optimum low power CMOS PLD solution, with low DC power (8 mA typical) and full CMOS output levels. The AT22V10L significantly reduces total system power and enhances system reliability.

Full CMOS output levels help reduce power in many other system components.

The AT22V10 and AT22V10L incorporate a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

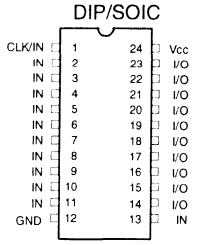
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all 10 registers. All registers are automatically cleared upon power up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

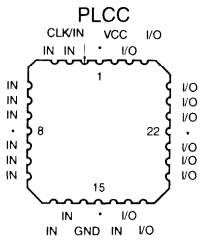
Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



PLCC



0023C

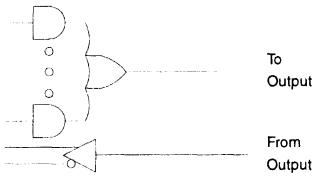
Absolute Maximum Ratings*

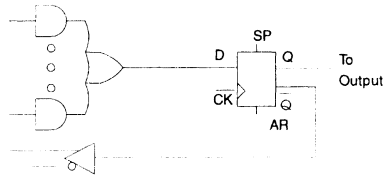
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

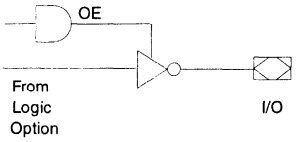
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options





Output Options



D.C. and A.C. Operating Conditions

	Commercial AT22V10/L -15, -20, -25	Industrial AT22V10/L -15, -20, -25	Military AT22V10/L -15, -20, -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND, Outputs Open	AT22V10-15,-20	Com.			90	mA
				Ind., Mil.			100	mA
			AT22V10-25,-35[2]				55	mA
			AT22V10L[2]	Com.		1.7	12	mA
				Ind., Mil.		2.0	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	AT22V10L[2]	Com.		2.0		mA/MHz
				Ind., Mil.		2.0		mA/MHz
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

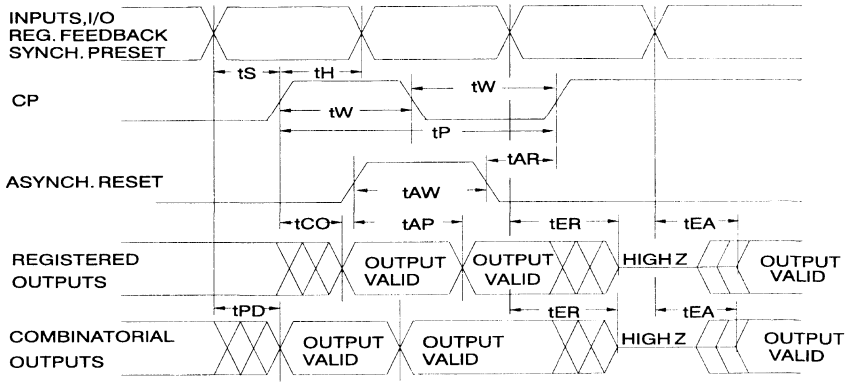
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics, Commercial and Industrial

Symbol	Parameter	AT22V10-15			AT22V10/L-20			AT22V10/L-25			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25	ns
t_{EA}	Input to Output Enable		10	15			20		15	25	ns
t_{ER}	Input to Output Disable		10	15			20		15	25	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	ns
t_{CO}	Clock to Output	0	7	10	0	8	12	0	10	15	ns
t_S	Input or Feedback Setup Time	10	8		12	8		15	12		ns
t_H	Hold Time	0			0			0			ns
t_P	Clock Period	12			20			24			ns
t_W	Clock Width	6			10			12			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			41.6			33.3	MHz
	Internal Feedback $1/(t_S + t_{CF})$			80.0			50.0			40.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	15	8		20	12		25	15		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25	ns

A.C. Waveforms [1]

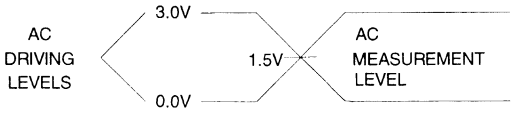


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics, Military

Symbol	Parameter	AT22V10-15			AT22V10/L-20			AT22V10/L-25			AT22V10/L-30			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		10	15		12	20		15	25		20	30	ns
t_{EA}	Input to Output Enable		10	15			20		15	25		20	30	ns
t_{ER}	Input to Output Disable		10	15			20		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	1	2.5	0	4	8	0	5	10	0	10	15	ns
t_{CO}	Clock to Output	0	7	10	0	8	15	0	10	15	0	12	20	ns
t_{SF}	Feedback Setup Time	10	8		12	10		15	12		18	15		ns
t_S	Input Setup Time	10	8		17	14		18	15		20	15		ns
t_H	Hold Time	0			0			0			0			ns
t_P	Clock Period	12			20			24			30			ns
t_W	Clock Width	6			10			12			15			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			50.0			31.2			30.3			25.0	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$			80.0			50.0			40.0			30.0	MHz
	No Feedback $1/(t_P)$			83.3			50.0			41.6			33.3	MHz
t_{AW}	Asynchronous Reset Width	15	8		20	9		25	10		30	15		ns
t_{AR}	Asynchronous Reset Recovery Time	15	8		20	12		25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		12	20		15	22		18	25		20	30	ns

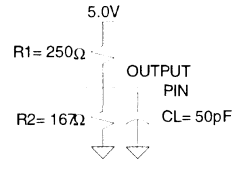
Input Test Waveforms and Measurement Levels



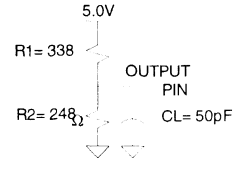
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

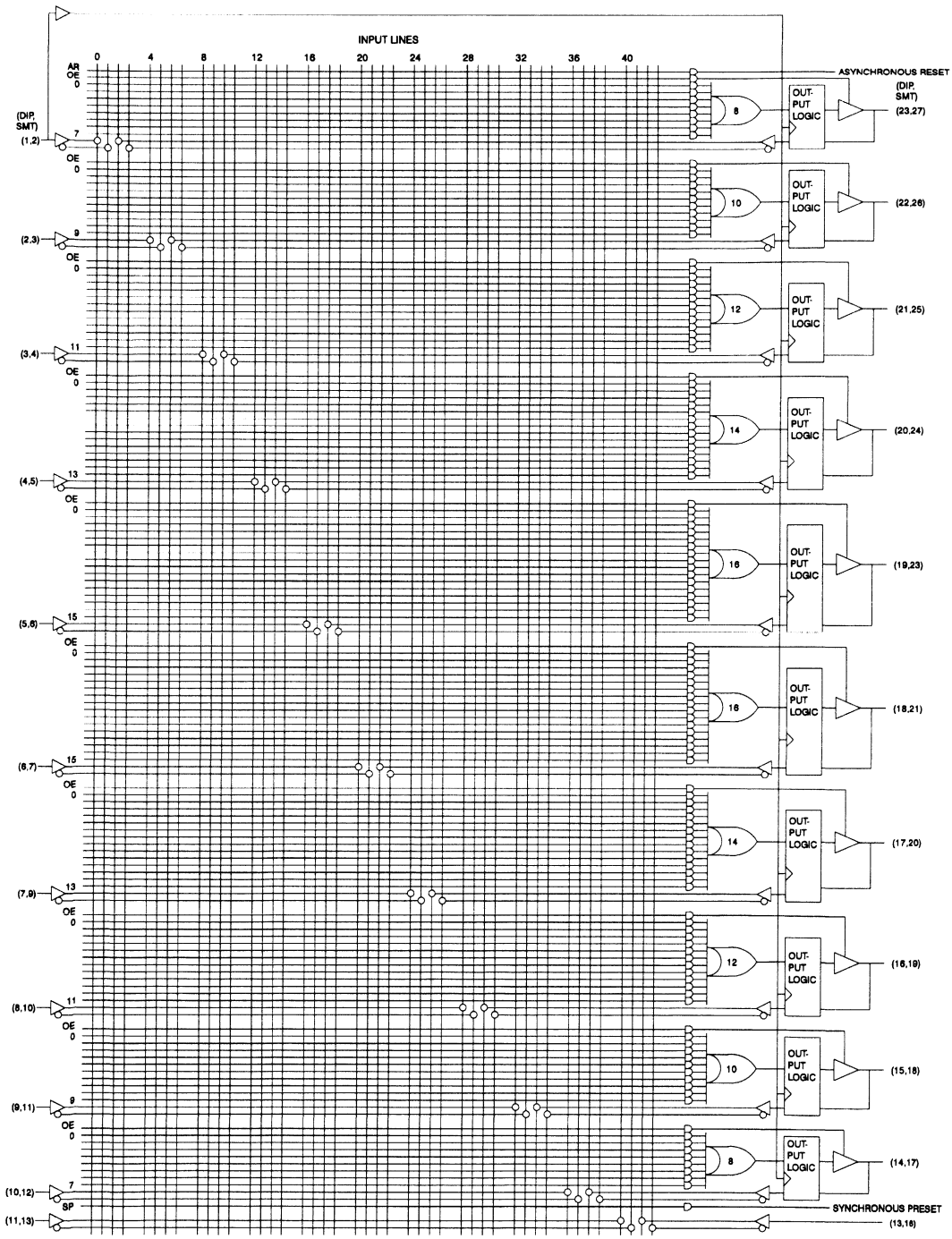
Commercial



Military



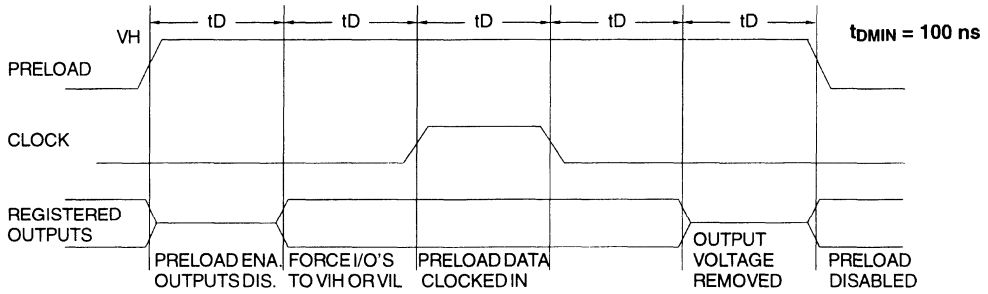
Functional Logic Diagram AT22V10/L



Preload of Registered Outputs

The registers in the AT22V10 and AT22V10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5-V to 13-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during preload cycle	Register state after cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

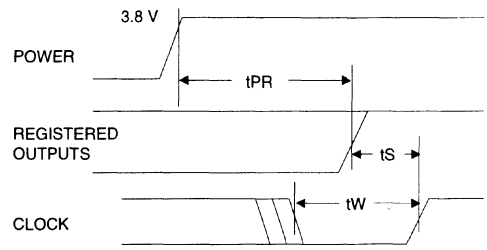
The registers in the AT22V10 and AT22V10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

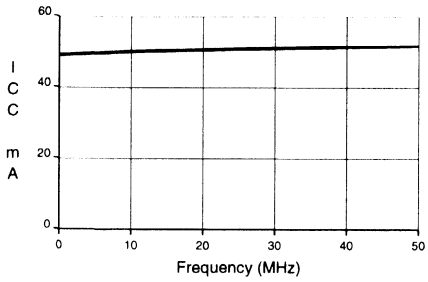
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10 or AT22V10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

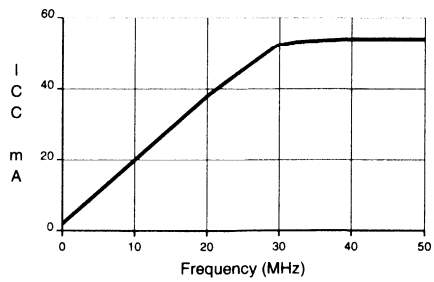
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10 (TA = 25C, VCC = 5V)

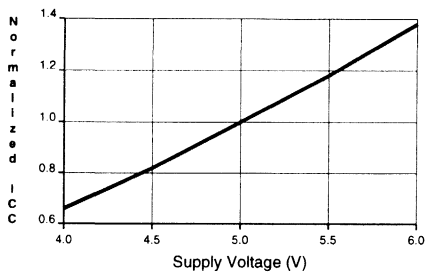


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10L (TA = 25C, VCC = 5V)

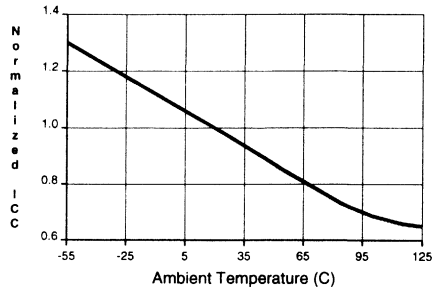


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



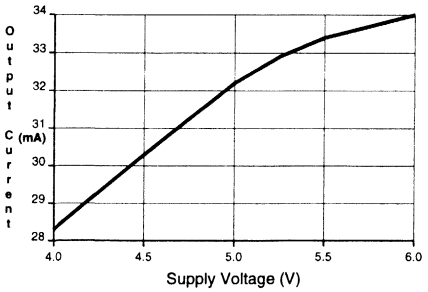
NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz



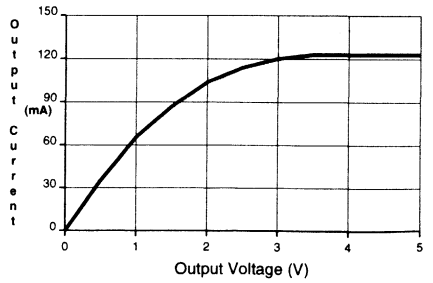
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



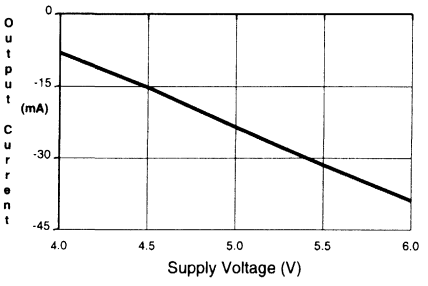
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



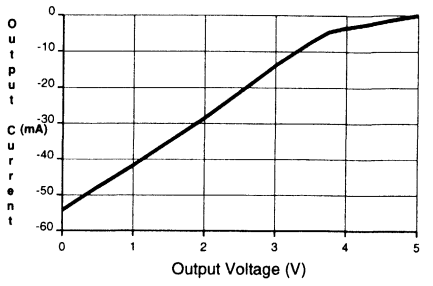
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

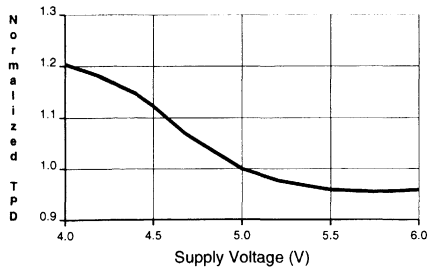


OUTPUT SOURCE CURRENT

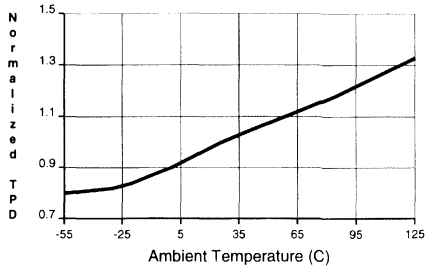
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



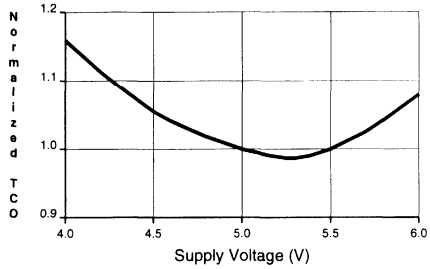
NORMALIZED TPD
vs. SUPPLY VOLTAGE



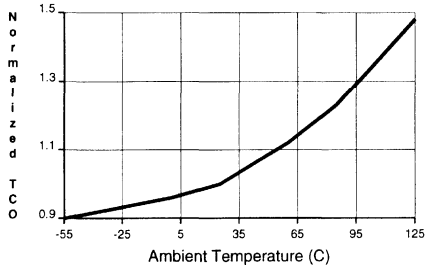
NORMALIZED TPD
vs. TEMPERATURE



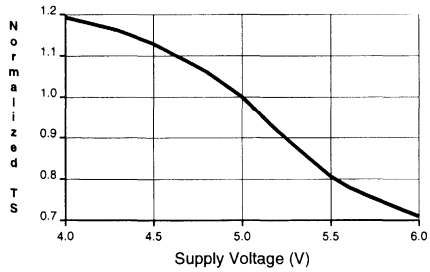
NORMALIZED TCO
vs. SUPPLY VOLTAGE



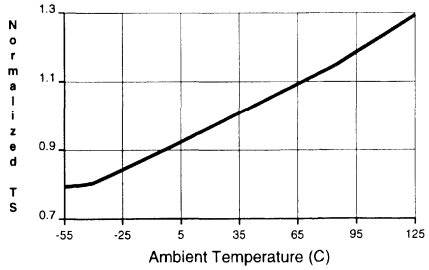
NORMALIZED TCO
vs. TEMPERATURE



NORMALIZED TS
vs. SUPPLY VOLTAGE

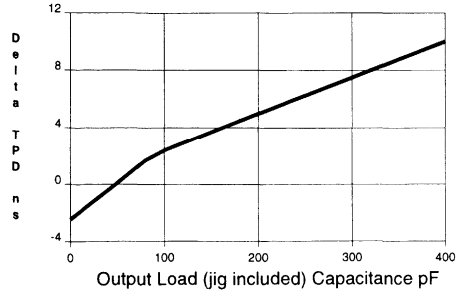


NORMALIZED TS
vs. TEMPERATURE



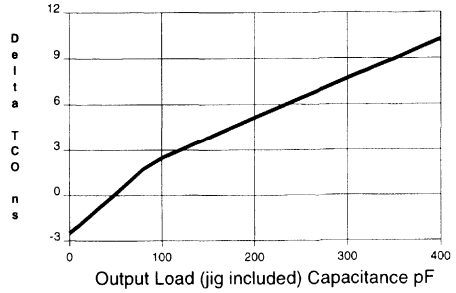
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	10	10	AT22V10-15DC AT22V10-15GC AT22V10-15JC AT22V10-15PC AT22V10-15SC	24DW3 24D3 28J 24P3 24S	Military/883C Commercial (0°C to 70°C)
			AT22V10-15DI AT22V10-15GI AT22V10-15JI AT22V10-15PI AT22V10-15SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22V10-15DM AT22V10-15GM AT22V10-15LM AT22V10-15NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10-15DM/883 AT22V10-15GM/883 AT22V10-15LM/883 AT22V10-15NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10-25DC AT22V10-25GC AT22V10-25JC AT22V10-25PC AT22V10-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10-25DI AT22V10-25GI AT22V10-25JI AT22V10-25PI AT22V10-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	18	15	AT22V10-25DM AT22V10-25GM AT22V10-25LM AT22V10-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10-25DM/883 AT22V10-25GM/883 AT22V10-25LM/883 AT22V10-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-87539 01 LA 5962-87539 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	10	5962-87539 05 LA 5962-87539 05 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	10	5962-88670 05 LA 5962-88670 05 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88670 01 LA 5962-88670 01 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	12	15	AT22V10L-20DC AT22V10L-20GC AT22V10L-20JC AT22V10L-20PC AT22V10L-20SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10L-20DI AT22V10L-20GI AT22V10L-20JI AT22V10L-20PI AT22V10L-20SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
20	17	15	AT22V10L-20DM AT22V10L-20GM AT22V10L-20LM AT22V10L-20NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10L-20DM/883 AT22V10L-20GM/883 AT22V10L-20LM/883 AT22V10L-20NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	15	AT22V10L-25DC AT22V10L-25GC AT22V10L-25JC AT22V10L-25PC AT22V10L-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10L-25DI AT22V10L-25GI AT22V10L-25JI AT22V10L-25PI AT22V10L-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	18	15	AT22V10L-25DM AT22V10L-25GM AT22V10L-25LM AT22V10L-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10L-25DM/883 AT22V10L-25GM/883 AT22V10L-25LM/883 AT22V10L-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-88724 04 LA 5962-88724 04 3X	24DW3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-88724 01 LA 5962-88724 01 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	17	15	5962-89755 04 LA 5962-89755 04 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	18	15	5962-89755 01 LA 5962-89755 01 3X	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

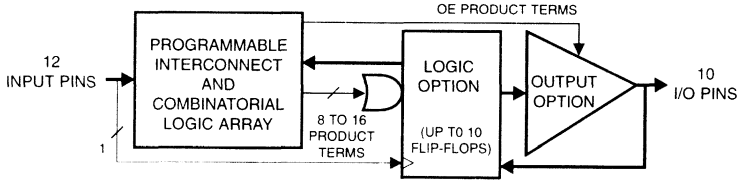
Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

High Speed UV Erasable Programmable Logic Device

Features

- **High Performance Programmable Logic Device**
  - **7.5 ns Max Propagation Delay**
  - **Up to 166 MHz Operation**
  - **5 V ± 10% Operation**
- **Fully Compatible with Standard 22V10**
  - **Identical Functionality/Fuse-Map**
- **TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability**
  - **Proven UV Erasable CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latch-Up Protection**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages with Standard Pinouts**

Logic Diagram



Description

The AT22V10B is an ultra-high performance CMOS Programmable Logic Device (PLD). Speeds down to 7.5 ns and operation up to 166 MHz are offered. All pins offer a low ± 10 µA leakage.

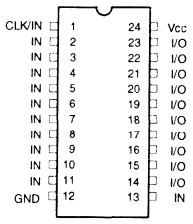
The AT22V10B logic functionality is fully compatible with the standard 22V10. The 12 dedicated inputs and ten configurable I/O pins allow implementation of logic requiring up to 22 input signals. The AT22V10B also provides individual output enable product terms for each of the ten I/Os.

(continued)

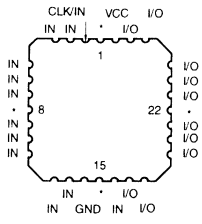
Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



PLCC



Description (Continued)

The AT22V10B incorporates a variable product term architecture. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

The AT22V10B includes two additional product terms to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

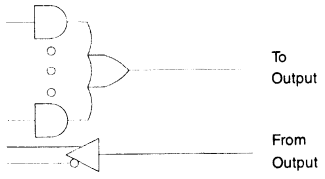
Absolute Maximum Ratings*

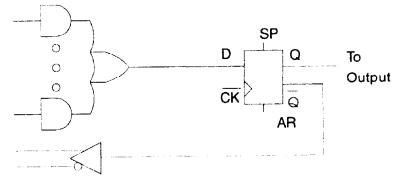
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

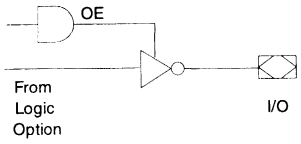
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

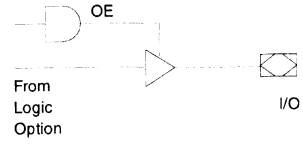
Logic Options





Output Options





D.C. and A.C. Operating Conditions

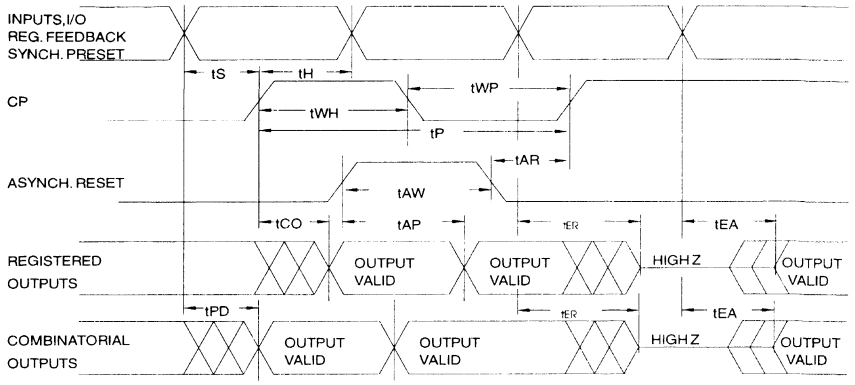
	Commercial AT22V10B -7	Commercial AT22V10B -10	Industrial AT22V10B -10	Military AT22V10B -10
Operating Temperature (Case)	0°C - 70°C	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current	f = 0 MHz to F_{MAX}, V_{CC} = MAX, V_{IN} = GND, Outputs Open		Com.		140	mA
				Ind., Mil.		160	mA
I_{OS} [1]	Output Short Circuit Current	V_{OUT} = 0.5 V			-30	-120	mA
V_{IL}	Input Low Voltage				-0.6	0.8	V
V_{IH}	Input High Voltage				2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.		0.5	V
			I_{OL} = 12 mA	Mil.		0.5	V
			I_{OL} = 24 mA	Com.		0.8	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -4.0 mA		2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

A.C. Waveforms [1]



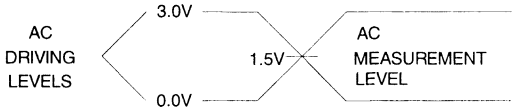
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

		AT22V10B-7			AT22V10B-10			
Symbol	**Parameter**	Min	Typ	Max	Min	Typ	Max	**Units**
t_{PD}	Input or Feedback to Non-Registered Output		5	7.5		6	10	ns
t_{EA}	Input to Output Enable		5	7.5		6	10	ns
t_{ER}	Input to Output Disable		5	7.5		6	10	ns
t_{CF} [1]	Clock to Feedback	0	1	2	0	1	2	ns
t_{CO}	Clock to Output	0	3.5	5.5	0	4	7	ns
t_S	Input or Feedback Setup Time	3.5	2		5	3		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	6			7			ns
t_{WL} [1]	Clock Width Low	3			3.5			ns
t_{WH}	Clock Width High	3			3.5			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			111			83	MHz
	Internal Feedback $1/(t_S + t_{CF})$			166			142	MHz
	No Feedback $1/(t_P)$			166			142	MHz
t_{AW}	Asynchronous Reset Width	6	3		7	4		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	7	4		8	5		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		6	10		8	14	ns

Note: 1. This parameter is only sampled and is not 100% tested.

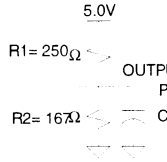
Input Test Waveforms and Measurement Levels



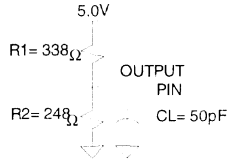
tR, tF < 2 ns (10% to 90%)

Output Test Loads:

Commercial

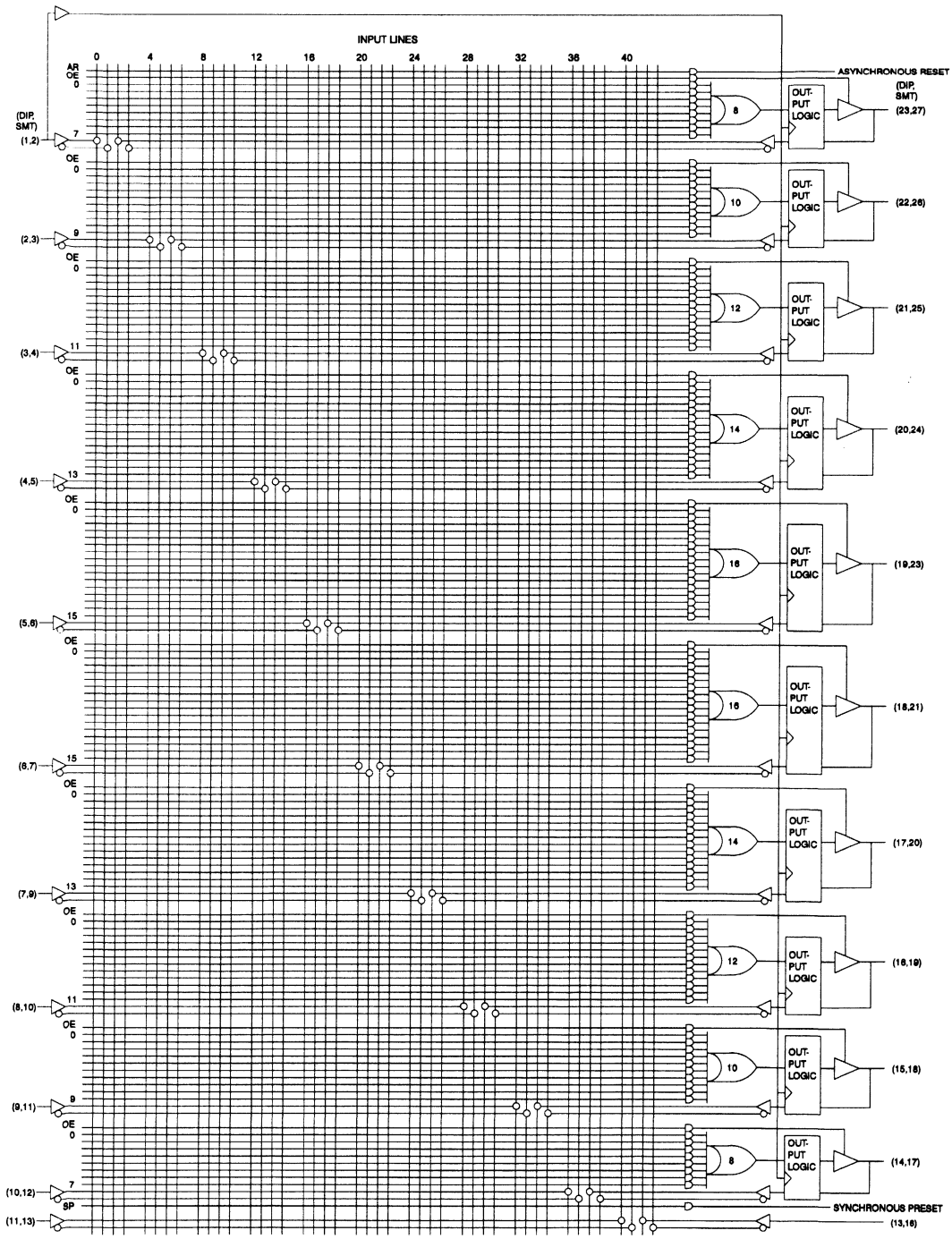


Military



Note: 1. CL = 30 pF for AT22V10B-7

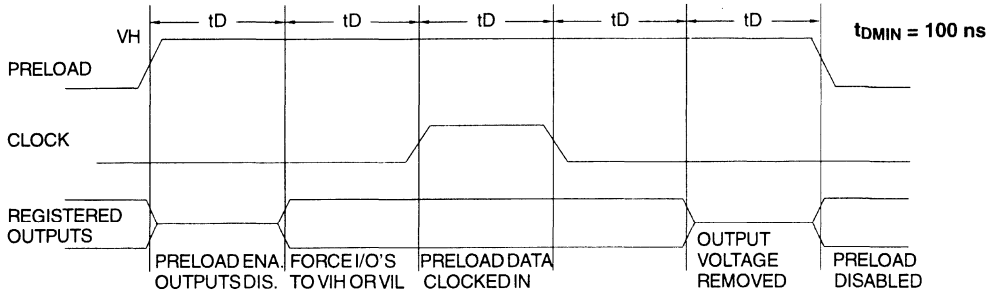
Functional Logic Diagram AT22V10B



Preload of Registered Outputs

The registers in the AT22V10B are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 10.5-V to 12-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during preload cycle	Register state after cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

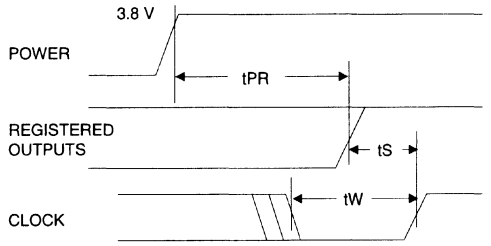
The registers in the AT22V10B are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

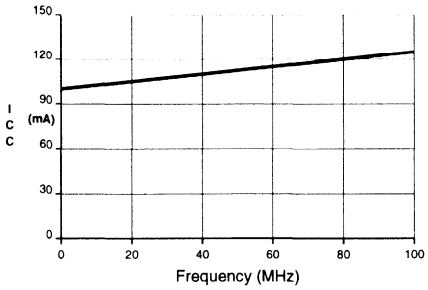
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22V10B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

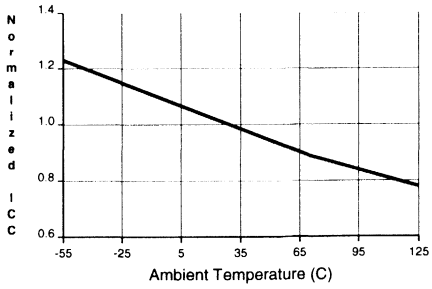
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22V10B (TA = 25C, VCC = 5V)

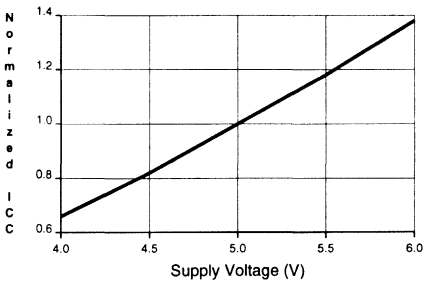


NORMALIZED ICC vs. AMBIENT TEMP.

f = 50 MHz

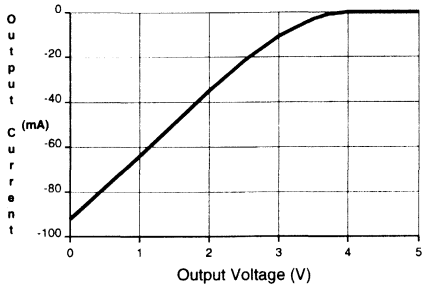


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



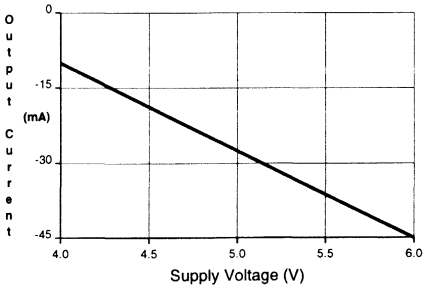
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



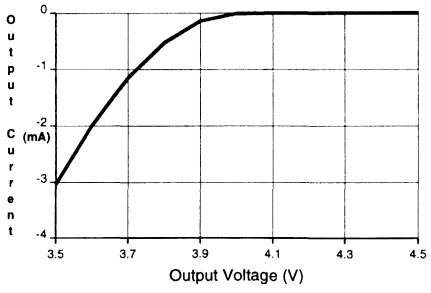
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)



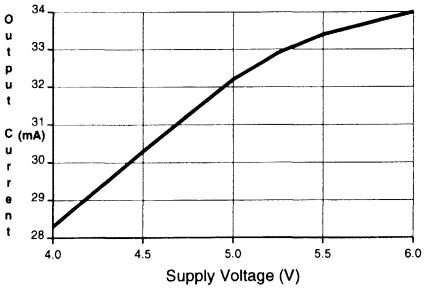
OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



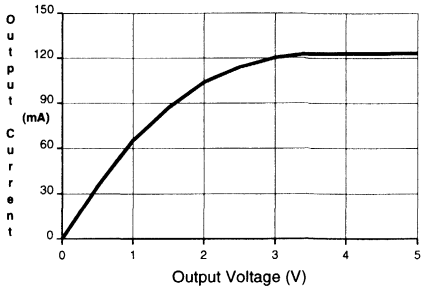
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)

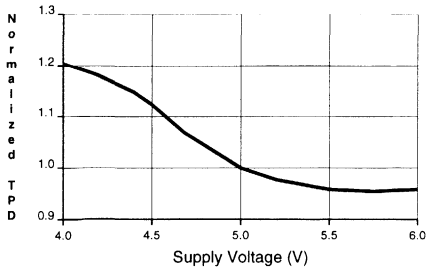


OUTPUT SINK CURRENT

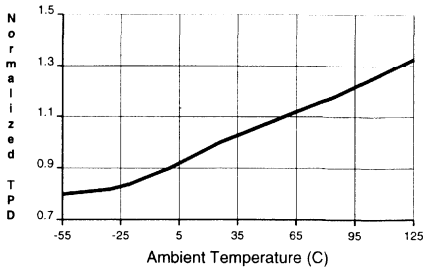
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



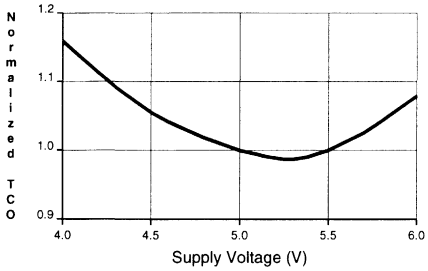
NORMALIZED TPD
vs. SUPPLY VOLTAGE



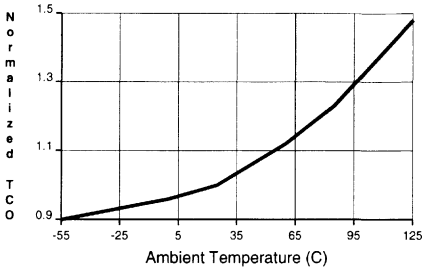
NORMALIZED TPD
vs. TEMPERATURE



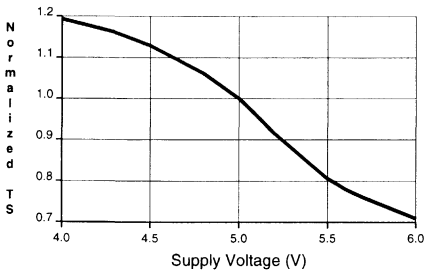
NORMALIZED TCO
vs. SUPPLY VOLTAGE



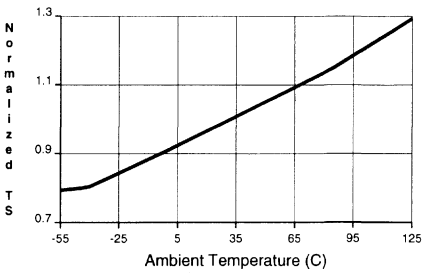
NORMALIZED TCO
vs. TEMPERATURE



NORMALIZED TS
vs. SUPPLY VOLTAGE

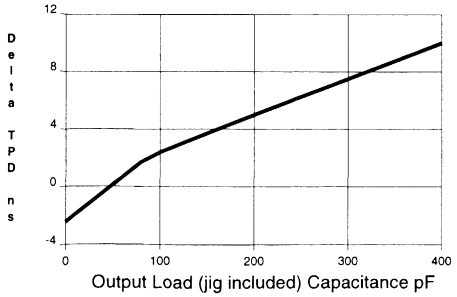


NORMALIZED TS
vs. TEMPERATURE



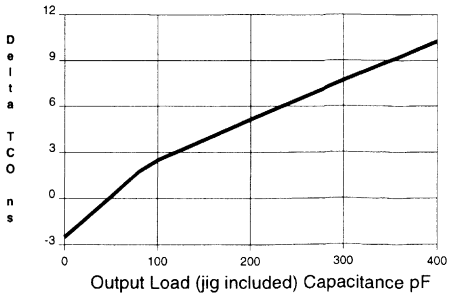
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	3.5	5.5	AT22V10B-7DC AT22V10B-7JC AT22V10B-7PC	24DW3 28J 24P3	Commercial (0°C to 70°C)
10	5	7	AT22V10B-10DC AT22V10B-10GC AT22V10B-10JC AT22V10B-10PC AT22V10B-10SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22V10B-10DI AT22V10B-10GI AT22V10B-10JI AT22V10B-10PI AT22V10B-10SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22V10B-10DM AT22V10B-10GM AT22V10B-10LM AT22V10B-10NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22V10B-10DM/883 AT22V10B-10GM/883 AT22V10B-10LM/883 AT22V10B-10NM/883 AT22V10B-12LM/883 AT22V10B-12NM/883	24DW3 24D3 28LW 28L 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
10	5	7	5962-87539 06 LA 5962-87539 06 3X	24DW3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

1

Low Voltage UV Erasable Programmable Logic Device

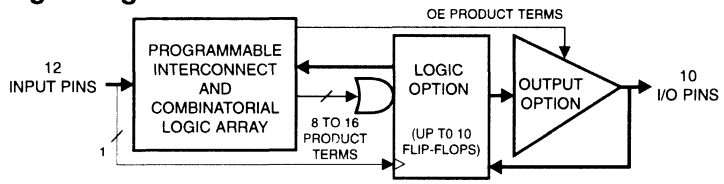
Features

- **Low Voltage Programmable Logic Device**
  - **Wide Power Supply Range - 3.0 V to 5.5 V**
  - **Ideal for Battery Powered Systems**
- **High Speed Operation**
  - **20 ns max Propagation Delay at V_{CC} = 3.0 V**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Familiar 22V10 Logic Architecture**
- **Low Power 3-Volt CMOS Operation**

	AT22LV10L	AT22LV10	
Temp	Com./Mil.	Com./Mil.	
Icc (mA)	4 / 5	35 / 45	V_{CC} = 3.6 V

- **CMOS and TTL Compatible Inputs and Outputs**
  - **10 µA Leakage Maximum**
- **Reprogrammable - Tested 100% for Programmability**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Dual-In-Line and Surface Mount Packages**

Logic Diagram



Description

The AT22LV10 and AT22LV10L are low voltage compatible CMOS high performance Programmable Logic Devices (PLDs). Speeds down to 20 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0 V to 5.5 V range. All pins offer a low ±10 µA leakage.

The AT22LV10L provides the optimum low power CMOS PLD solution, with low DC power (1 mA typical at V_{CC} = 3.3 V) and full CMOS output levels. The AT22LV10L significantly reduces total system power, allowing battery powered operation.

Full CMOS output levels help reduce power in many other system components.

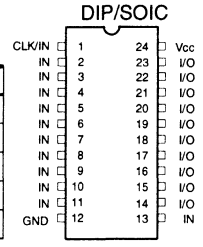
The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

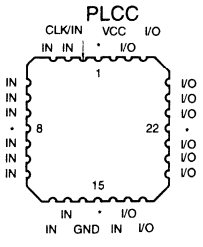
Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

Pin Configurations

Pin Name	Function
CLK/IN	Clock and Logic Input
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	3.0 V to 5.5 V Supply





0190B

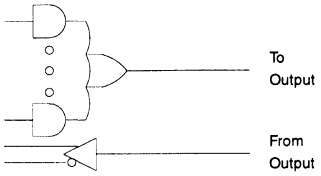
Absolute Maximum Ratings*

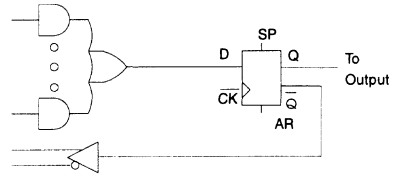
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

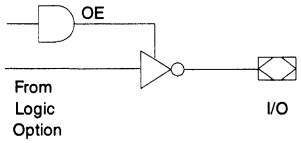
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum pin voltage is V_{CC}+0.75 V dc which may overshoot to V_{CC} +2.0 V for pulses of less than 20 ns.

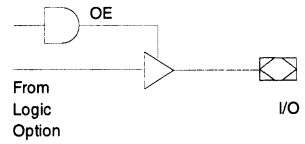
Logic Options





Output Options





D.C. and A.C. Operating Conditions

	Commercial AT22LV10/L -20, -25, -30	Industrial AT22LV10/L -20, -25, -30	Military AT22LV10/L -25, -30
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	3.0 V to 5.5 V	3.0 V to 5.5 V	3.0 V to 5.5 V

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = 3.6 V / 5.5 V, V_{IN} = GND, Outputs Open	AT22LV10	Com.		20/50	35/90	mA
				Ind., Mil.		20/50	45/100	mA
			AT22LV10L(2)	Com.		1/2	4/12	mA
				Ind., Mil.		1/2	5/15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = Max, Outputs Open	AT22LV10L(2)	Com.		1.0		mA/MHz
				Ind., Mil.		1.0		mA/MHz
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V			-0.6		0.8	V
V_{IL2}	Input Low Voltage	3.0 V ≤ V_{CC} < 4.5 V			-0.6		0.6	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage V_{IN} = V_{IH} or V_{IL}	V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 8 mA / 6 mA			0.5	V
		V_{CC} = 4.5 V	Com.,Ind./Mil.	I_{OL} = 16 mA / 12 mA			0.5	V
		V_{CC} = 3.0 V	Com.,Ind./Mil.	I_{OL} = 6 mA / 4 mA			0.35	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 3.0 V / 4.5 V	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -0.4 mA / -4.0 mA		2.4			V

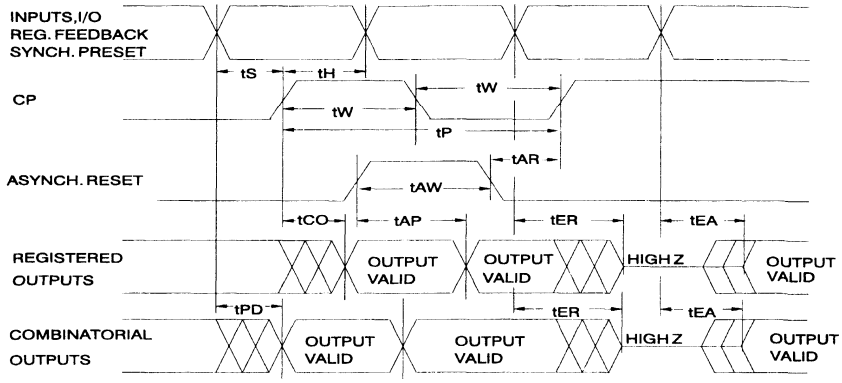
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See I_{CC} vs. Frequency curves in the back of this data sheet.

A.C. Characteristics for the AT22LV10

Symbol	Parameter	AT22LV10-20			AT22LV10-25			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		12	20		15	25	ns
t_{EA}	Input to Output Enable			20		15	25	ns
t_{ER}	Input to Output Disable			20		15	25	ns
t_{CF}	Clock to Feedback	0	4	9	0	5	9	ns
t_{CO}	Clock to Output	0	8	14	0	10	17	ns
t_S	Input or Feedback Setup Time	10	6		12	7		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	10			12			ns
t_W	Clock Width	5			6			ns
F_{MAX}	External Feedback 1/(t_S+t_{CO})			41.6			34.5	MHz
	Internal Feedback 1/(t_S + t_{CF})			52.6			47.6	MHz
	No Feedback 1/(t_P)			100.0			83.3	MHz
t_{AW}	Asynchronous Reset Width	20	12		25	15		ns
t_{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	20	12		25	15		ns

A.C. Waveforms [1]

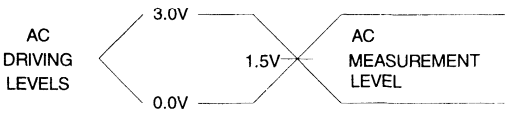


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics for the AT22LV10L

Symbol	Parameter	AT22LV10L-25			AT22LV10L-30			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Non-Registered Output		15	25		20	30	ns
t_{EA}	Input to Output Enable		15	25		20	30	ns
t_{ER}	Input to Output Disable		15	25		20	30	ns
t_{CF}	Clock to Feedback	0	5	9	0	6	10	ns
t_{CO}	Clock to Output	0	10	14	0	12	17	ns
t_{SF}	Feedback Setup Time	12	7		15	10		ns
t_S	Input Setup Time	17	15		20	15		ns
t_H	Hold Time	0			0			ns
t_P	Clock Period	12			14			ns
t_W	Clock Width	6			7			ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$			32.2			27.0	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$			47.6			40.0	MHz
	No Feedback $1/(t_P)$			83.3			71.4	MHz
t_{AW}	Asynchronous Reset Width	25	15		30	18		ns
t_{AR}	Asynchronous Reset Recovery Time	25	15		30	18		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		18	28		20	30	ns

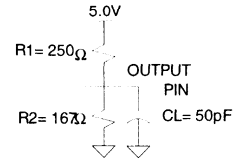
Input Test Waveforms and Measurement Levels



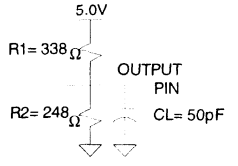
tR, tF < 5 ns (10% to 90%)

Output Test Loads:

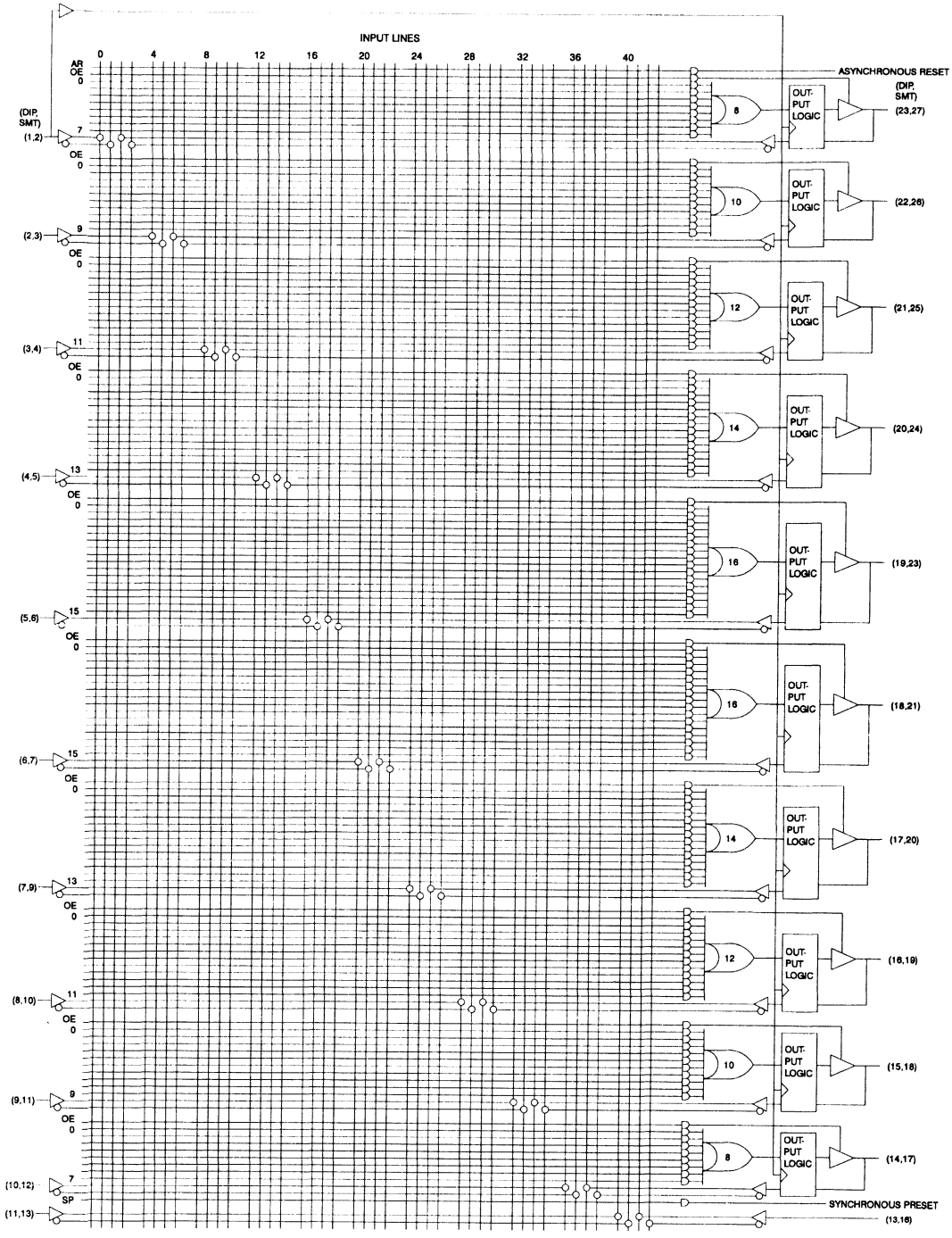
Commercial



Military



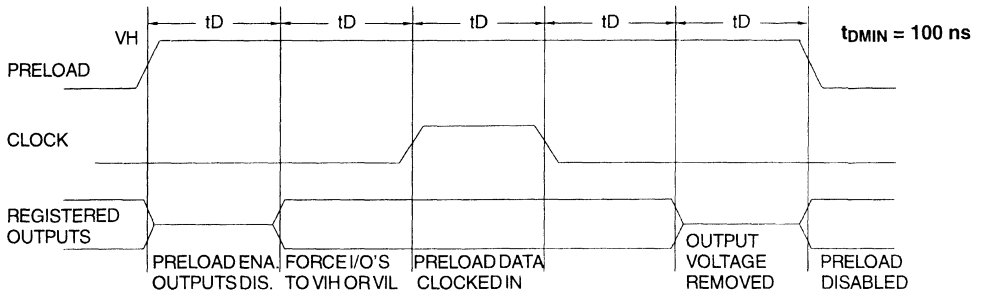
Functional Logic Diagram AT22LV10/L



Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5-V to 13-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level forced on registered output pin during preload cycle	Register state after cycle
V_{IH}	High
V_{IL}	Low



Power Up Reset

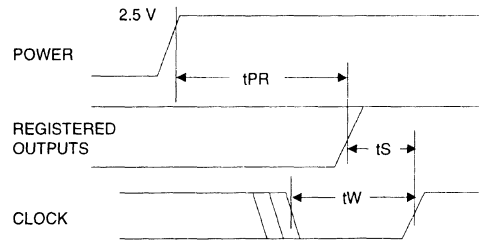
The registers in the AT22LV10 and AT22LV10L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 2.5 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

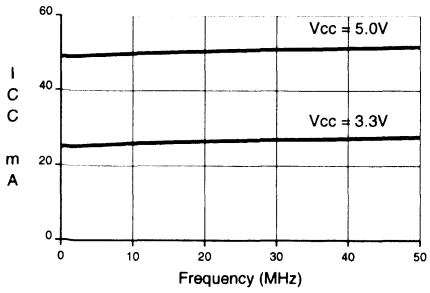
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

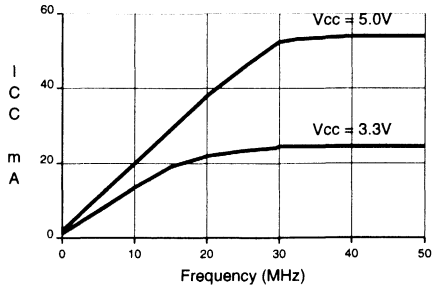
SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10 (TA = 25C)

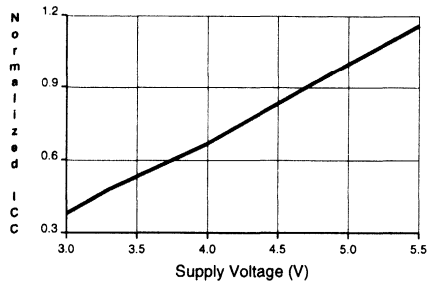


SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10L (TA = 25C)

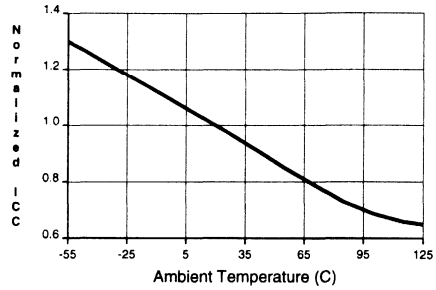


NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



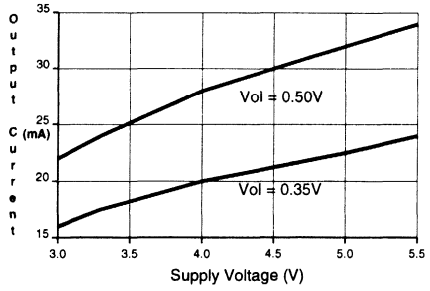
NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz



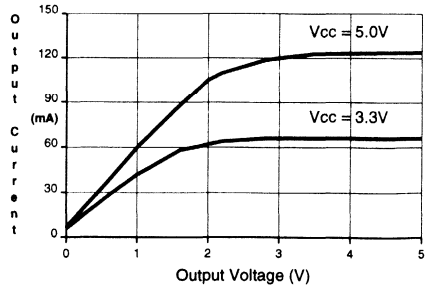
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



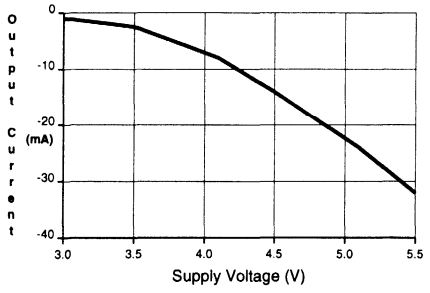
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C)



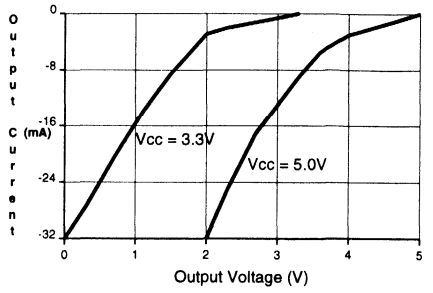
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V TA = 25C)

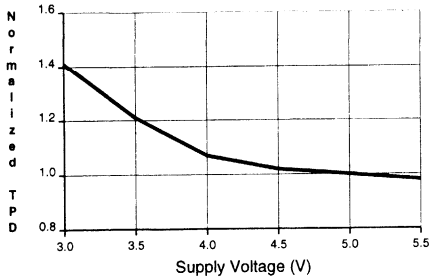


OUTPUT SOURCE CURRENT

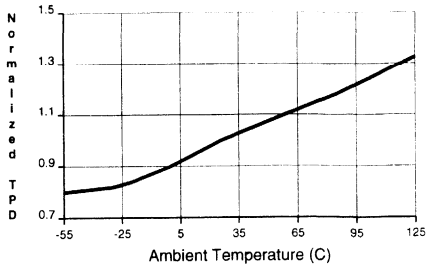
vs. OUTPUT VOLTAGE (TA = 25C)



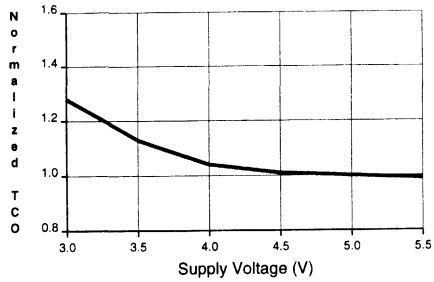
NORMALIZED TPD vs. SUPPLY VOLTAGE



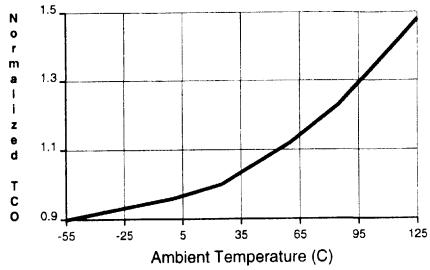
NORMALIZED TPD vs. TEMPERATURE



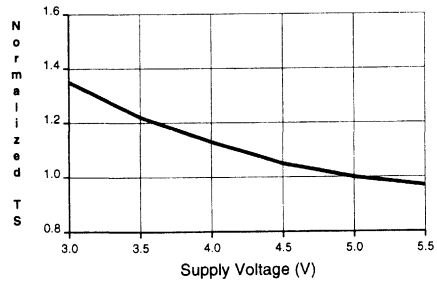
NORMALIZED TCO vs. SUPPLY VOLTAGE



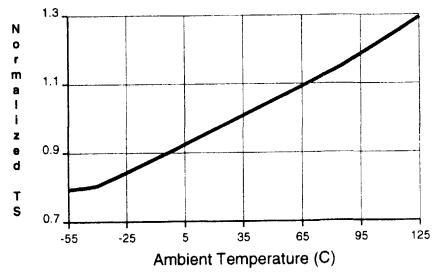
NORMALIZED TCO vs. TEMPERATURE



NORMALIZED TS vs. SUPPLY VOLTAGE

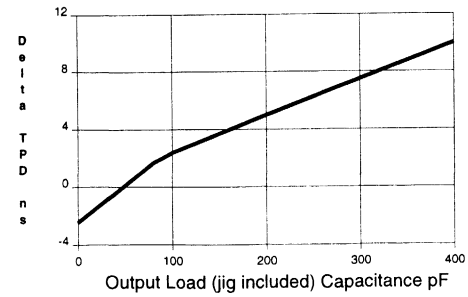


NORMALIZED TS vs. TEMPERATURE



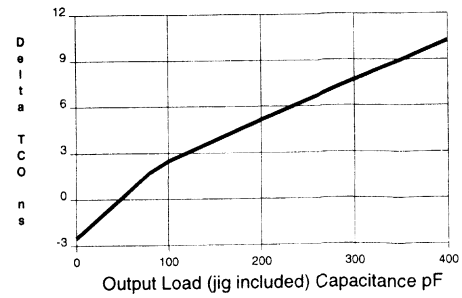
DELTA TPD vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING

(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
20	10	14	AT22LV10-20DC AT22LV10-20GC AT22LV10-20JC AT22LV10-20PC AT22LV10-20SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-20DI AT22LV10-20GI AT22LV10-20JI AT22LV10-20PI AT22LV10-20SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
25	12	17	AT22LV10-25DC AT22LV10-25GC AT22LV10-25JC AT22LV10-25PC AT22LV10-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-25DI AT22LV10-25GI AT22LV10-25JI AT22LV10-25PI AT22LV10-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22LV10-25DM AT22LV10-25GM AT22LV10-25LM AT22LV10-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22LV10-25DM/883 AT22LV10-25GM/883 AT22LV10-25LM/883 AT22LV10-25NM/883	24DW3 24D3 28LW 28L	Military/883D (-55°C to 125°C) Class B, Fully Compliant
25	12	17	5962-93245 01M LA 5962-93245 01M 3X	24DW3 28LW	Military/883D (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	17	14	AT22LV10L-25DC AT22LV10L-25GC AT22LV10L-25JC AT22LV10L-25PC AT22LV10L-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-25DI AT22LV10L-25GI AT22LV10L-25JI AT22LV10L-25PI AT22LV10L-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
30	20	17	AT22LV10L-30DC AT22LV10L-30GC AT22LV10L-30JC AT22LV10L-30PC AT22LV10L-30SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-30DI AT22LV10L-30GI AT22LV10L-30JI AT22LV10L-30PI AT22LV10L-30SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			AT22LV10L-30DM AT22LV10L-30GM AT22LV10L-30LM AT22LV10L-30NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			AT22LV10L-30DM/883 AT22LV10L-30GM/883 AT22LV10L-30LM/883 AT22LV10L-30NM/883	24DW3 24D3 28LW 28L	Military/883D (-55°C to 125°C) Class B, Fully Compliant
30	20	17	5962-93245 03M LA 5962-93245 03M LX	24DW3 28LW	Military/883D (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

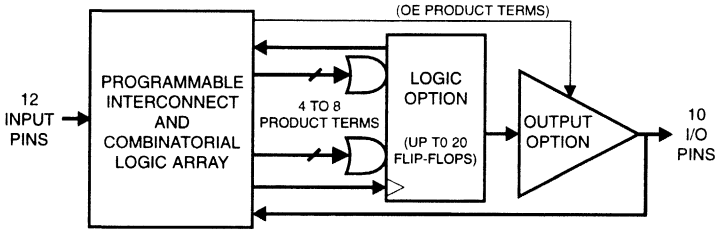
Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP), Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

High Density UV Erasable Programmable Logic Device

Features

- **Third Generation Programmable Logic Structure**
  - **High Density Replacement for Discrete Logic**
- **High Speed - Plus a New Low Power Version**
- **Increased Logic Flexibility**
  - **42 Inputs and 20 Sum terms**
- **Flexible Output Logic**
  - **20 Flip-Flops - 10 Extra**
  - **All Can Be Individually Buried or 10 Output Directly**
  - **Each has Individual Asynchronous Reset and Clock Terms**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **24-pin, 300-mil Dual-In-line and 28-Lead Surface Mount Packages**

Logic Diagram



Description

The ATV750/L is 100% more powerful than most other programmable logic devices in 24-pin packages. Increased product terms, sum terms, and flip-flops translate into more usable gates.

Each of the ATV750's 22 logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All 20 flip-flops can be fed back into the array independently. This flexibility allows burying all of the sum terms and flip-flops.

There are 171 product terms available. A variable format is used to assign between four and eight product terms per sum term. There are two sum terms per output, providing added flexibility.

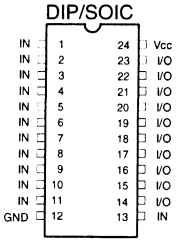
The ATV750/L has more flip-flops available than other PLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing asynchronous resets, flip-flop clocks, and output enables. One reset and one clock term are provided per flip-flop, with one enable term per output. One product term provides a global synchronous preset. Register preload simplifies testing. The device has an internal power up clear function.

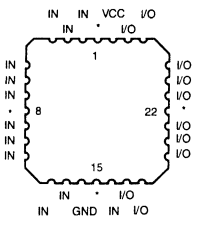
Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
Vcc	+5V Supply

DIP/SOIC



PLCC/LCC



0024C

Absolute Maximum Ratings*

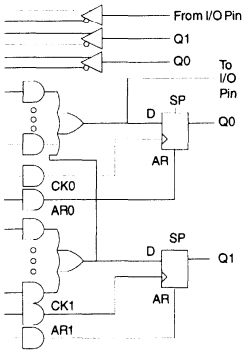
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

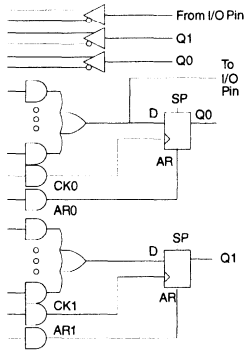
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options

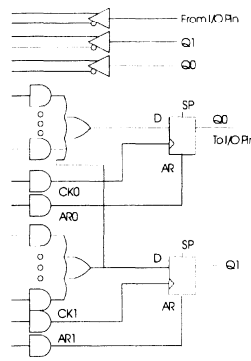
Combined Terms



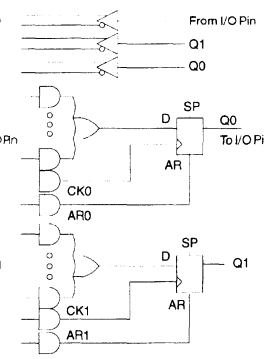
Separate Terms



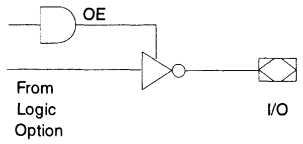
Combined Terms

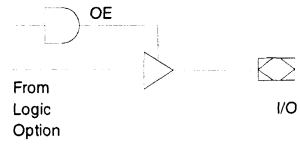


Separate Terms



Output Options





D.C. and A.C. Operating Conditions

		ATV750-20	ATV750/L-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%

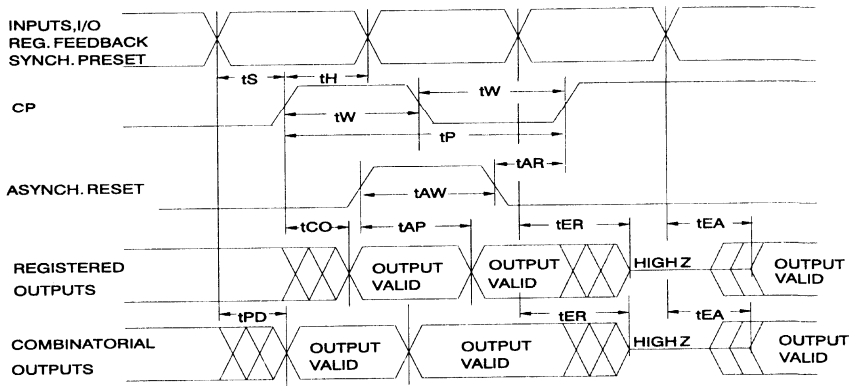
D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	VCC = MAX, V_{IN} = GND, Outputs Open	ATV750	Com.			120	mA
				Ind.,Mil.			140	mA
			ATV750L	Com.		1.0	12	mA
				Ind.,Mil.		1.0	15	mA
I_{CC2} (2)	Clocked Power Supply Current	VCC = MAX, Outputs Open	ATV750L(2)	Com.		3.0		mA/MHz
				Ind.,Mil.		3.0		mA/MHz
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 12 mA Com.,Ind.				0.5	V
			I_{OL} = 8 mA Mil.				0.5	V
			I_{OL} = 24 mA, Com.				1.0	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

2. See ICC vs frequency curves at end of datasheet.

A.C. Waveforms [1]

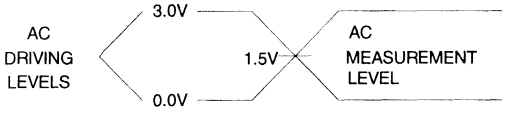


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

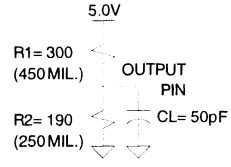
Symbol	Parameter	ATV750-20 Min	ATV750-20 Max	ATV750/L-25 Min	ATV750/L-25 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		20		25	ns
t_{EA}	Input to Output Enable		20		25	ns
t_{ER}	Input to Output Disable		20		25	ns
t_{CO}	Clock to Output		20		22	ns
t_{CF}	Clock to Feedback	5	10	5	10	ns
t_S	Input Setup Time	10		12		ns
t_{SF}	Feedback Setup Time	5		7		ns
t_H	Hold Time	5		5		ns
t_P	Clock Period	18		22		ns
t_W	Clock Width	8		10		ns
F_{MAX}	Maximum Frequency		55		45	MHz
t_{AW}	Asynchronous Reset Width	15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		20		25	ns
t_{SP}	Setup Time, Synchronous Preset	12		15		ns

Input Test Waveforms and Measurement Levels

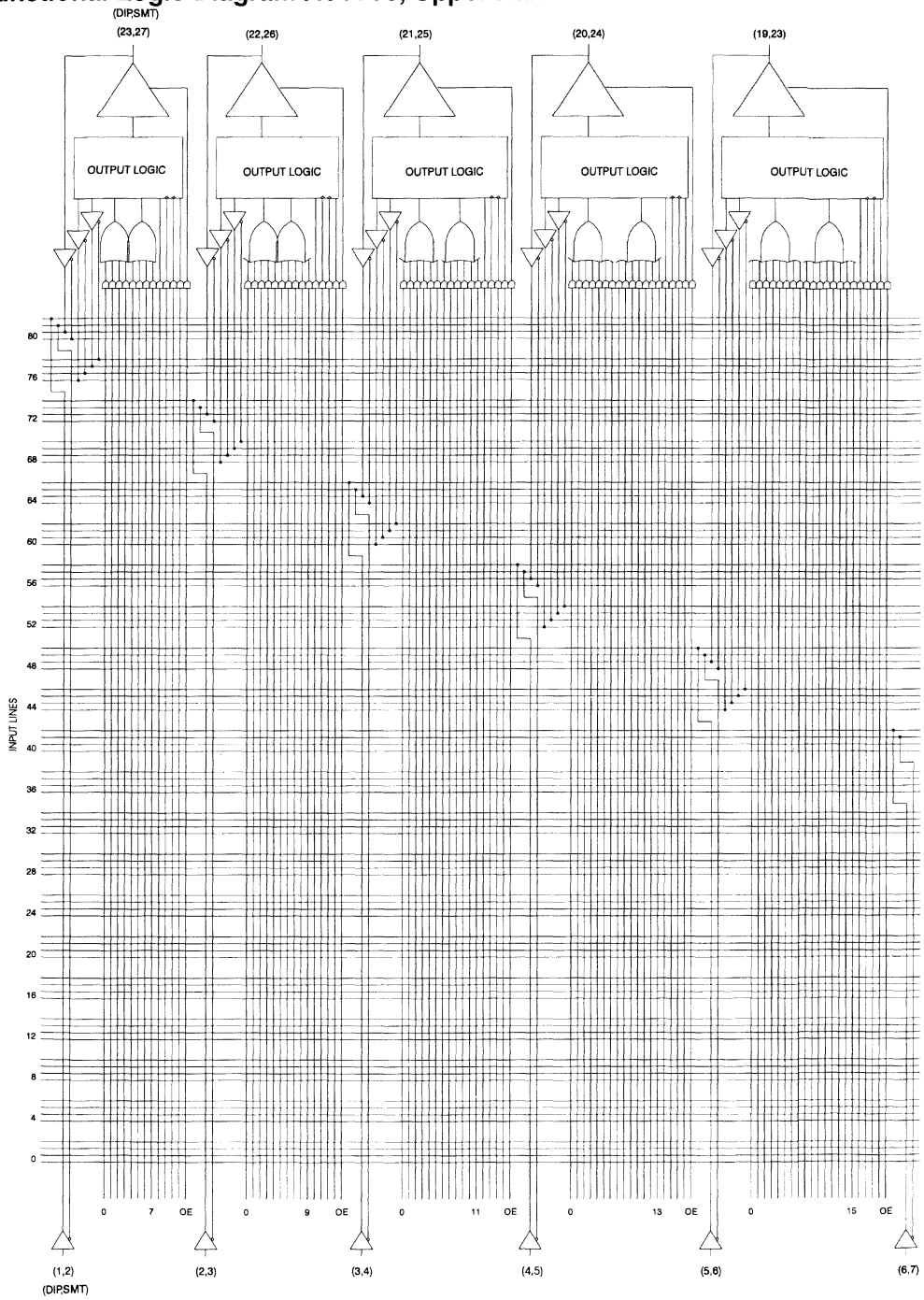


tR, tF < 5 ns (10% to 90%)

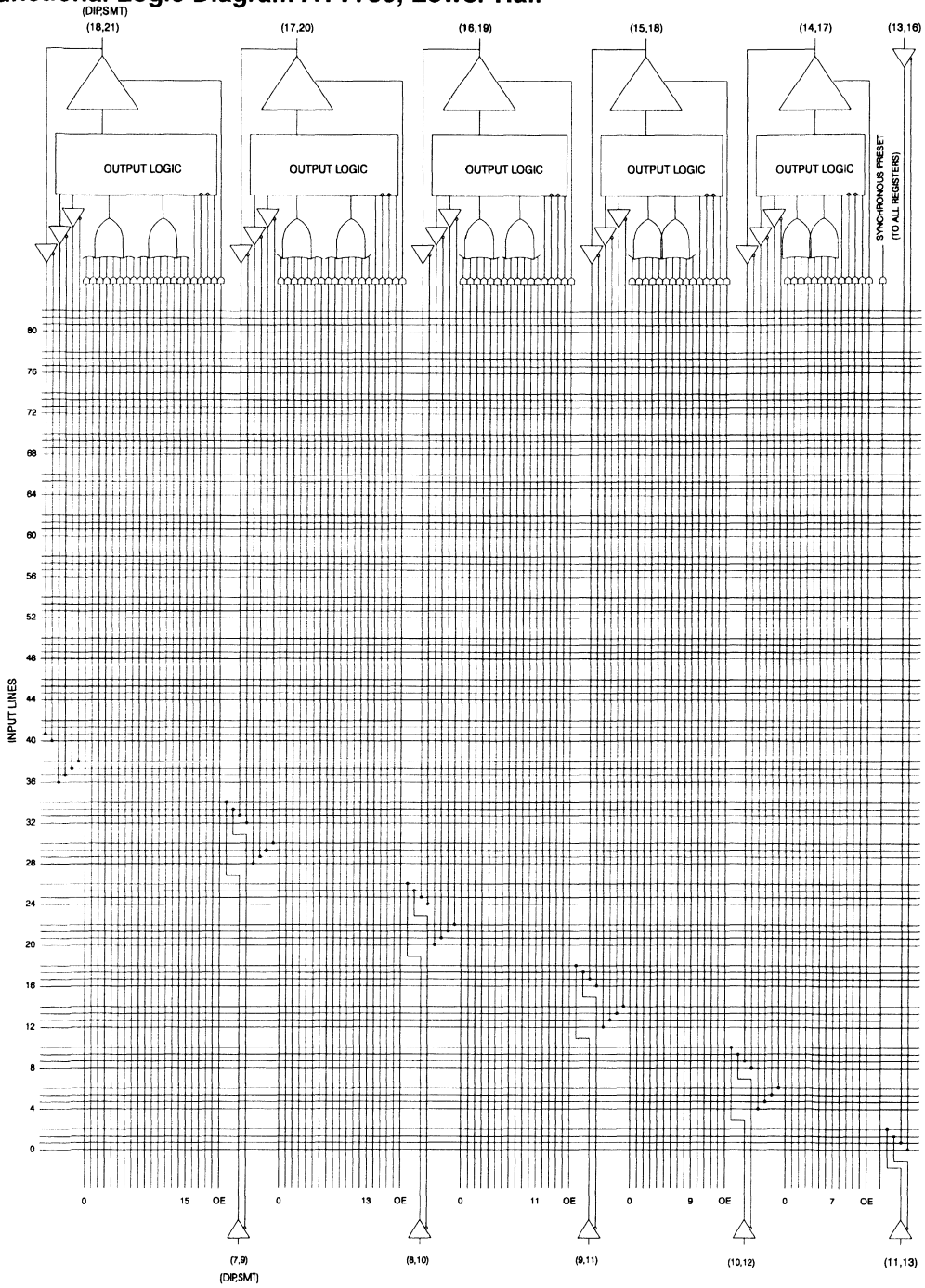
Output Test Load



Functional Logic Diagram ATV750, Upper Half

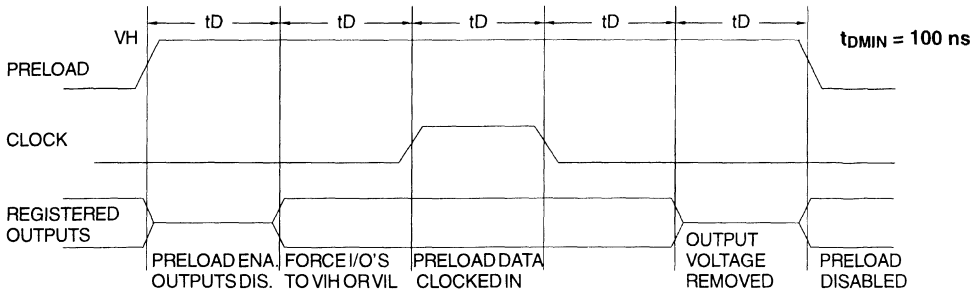


Functional Logic Diagram ATV750, Lower Half



Preload of Registered Outputs

The ATV750's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the output polarity. The preload state is entered by placing an 10.5-V to 11.5-V signal on pin 8 on DIPs, and pin 10 on SMPs. When the clock term is pulsed high, the data on the I/O pin is placed into the register chosen by the Select Pin.



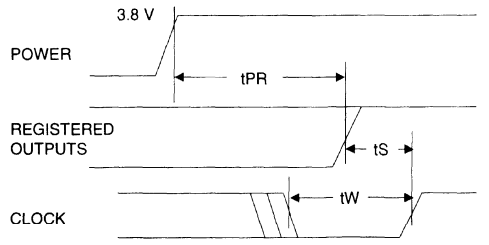
Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #1 state after cycle	Register #2 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

The registers in the ATV750/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using the ATV750's Many Advanced Features

The ATV750's flexibility puts more usable gates in 24 pins than other PLDs. The ATV750/L starts with an architecture similar to the popular AT22V10, and adds several features:

- Asynchronous Clocks -
  Each of the flip-flops in the ATV750/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV750/L clock period matches that of similar synchronous devices.
- A Full Bank of 10 More Registers -
  The ATV750/L provides two flip-flops for each output macrocell - a total of 20. Each register has its own clock and reset product terms, as well as its own SUM term.
- Independent I/O Pin and Feedback Paths -
  Each I/O pin on the ATV750/L has a dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's output enable, facilitates designs using bi-directional I/O buses.
- Combinable Sum Terms -
  Each output macrocell's two SUM terms can be combined in an OR gate before the output or the register. This provides up to 16 product terms per output or flip-flop. This architecture increases the number of usable gates available.

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV750/L is available from several PLD software vendors. Please refer to the Software Support Information table in the *Programmable Logic Development Tools* section for more information.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750/L. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received combine so as to force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750/L fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

The entire memory array of an ATV750/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

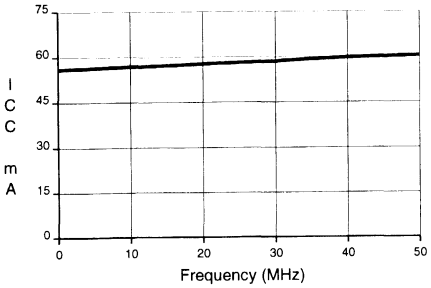
Atmel CMOS PLDs

Atmel's Programmable Logic Devices utilize an advanced 1.5-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

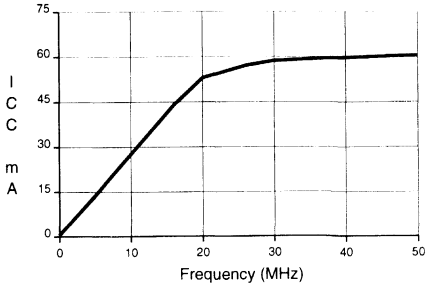
V750 ICC vs FREQUENCY

TA = 25C, VCC = 5V



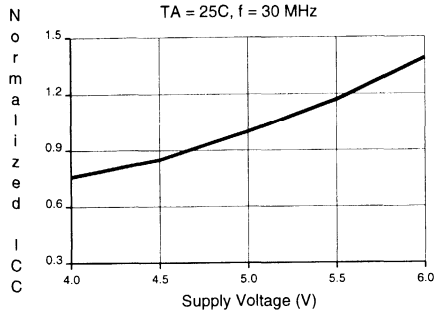
V750L ICC vs FREQUENCY

TA = 25C, VCC = 5V



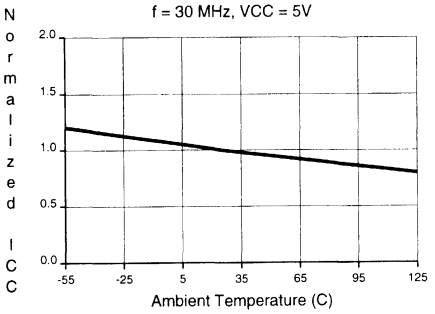
NORMALIZED ICC vs. VCC

TA = 25C, f = 30 MHz



NORMALIZED ICC vs. AMBIENT TEMP.

f = 30 MHz, VCC = 5V



Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
20	20	55	ATV750-20DC ATV750-20GC ATV750-20JC ATV750-20PC ATV750-20SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750-20DI ATV750-20GI ATV750-20JI ATV750-20PI ATV750-20SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750-20DM ATV750-20GM ATV750-20LM ATV750-20NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750-20DM/883 ATV750-20GM/883 ATV750-20LM/883 ATV750-20NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C)
25	22	45	ATV750-25DC ATV750-25GC ATV750-25JC ATV750-25PC ATV750-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750-25DI ATV750-25GI ATV750-25JI ATV750-25PI ATV750-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750-25DM ATV750-25GM ATV750-25LM ATV750-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750-25DM/883 ATV750-25GM/883 ATV750-25LM/883 ATV750-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	20	55	5962-88726 04 LA 5962-88726 04 3X 5962-94524 03 MLA 5962-94524 03 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 03 LA 5962-88726 03 3X 5962-94524 02 MLA 5962-94524 02 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	22	45	ATV750L-25DC ATV750L-25GC ATV750L-25JC ATV750L-25PC ATV750L-25SC	24DW3 24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750L-25DI ATV750L-25GI ATV750L-25JI ATV750L-25PI ATV750L-25SI	24DW3 24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750L-25DM ATV750L-25GM ATV750L-25LM ATV750L-25NM	24DW3 24D3 28LW 28L	Military (-55°C to 125°C)
			ATV750L-25DM/883 ATV750L-25GM/883 ATV750L-25LM/883 ATV750L-25NM/883	24DW3 24D3 28LW 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	22	45	5962-88726 07 LX 5962-88726 07 3X 5962-94524 05 MLA 5962-94524 05 M3X	24DW3 28LW 24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
24D3	24 Lead, 0.300" Wide, Non-Windowed (OTP) Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28L	28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier OTP (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

1

High Speed UV Erasable Programmable Logic Device

Features

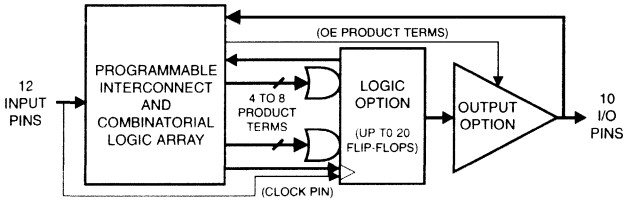
- **Advanced, High Speed Programmable Logic Device-Superset of 22V10**
  - **Improved Performance - 7.5 ns tPD, 95 MHz External Operation**
  - **Enhanced Logic Flexibility**
  - **Backward Compatible with ATV750/L Software and Hardware**
- **New Flip-Flop Features**
  - **D- or T-Type**
  - **Product Term or Direct Input Pin Clocking**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Several Power Saving Options**

Device	Icc, Stand-By
ATV750B	125 mA
ATV750BQ	60 mA
ATV750BL	15 mA
ATV750BQL	15 mA

[ ] = Advance Information

- **Highest Density Programmable Logic Available in a 24-Pin Package**
- **Increased Logic Flexibility**
  - **42 Array Inputs, 20 Sum Terms and 20 Flip-Flops**
- **Enhanced Output Logic Flexibility**
  - **All 20 Flip-Flops Feed Back Internally**
  - **10 Flip-Flops are Also Available as Outputs**
- **Full Military, Commercial and Industrial Temperature Ranges**

Logic Diagram



Description

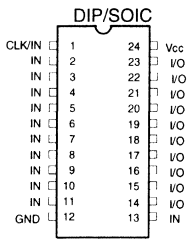
The ATV750Bs are twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High speed logic and uniform, predictable delays guarantee fast in-system performance.

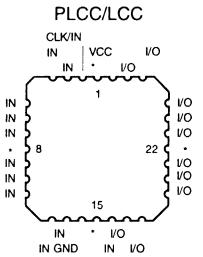
Each of the ATV750B's 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
Vcc	+5 V Supply





0301B

Description (Continued)

D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. A variable format is used to assign between four to eight product terms per sum term. There are two sum terms per output, providing added flexibility. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATV750BL is a low power device with speeds as fast as 15 ns. The ATV750BL provides the optimum low power PLD solution, with full CMOS output levels. This device significantly reduces total system power, thereby allowing battery-powered operation.

Absolute Maximum Ratings*

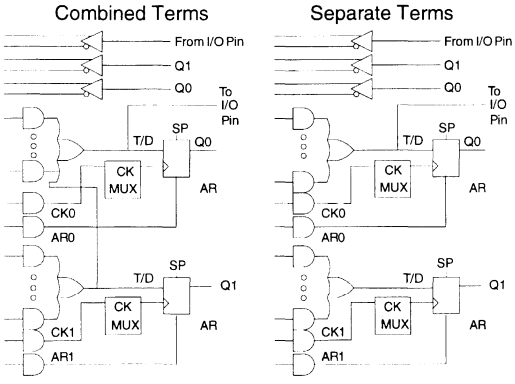
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

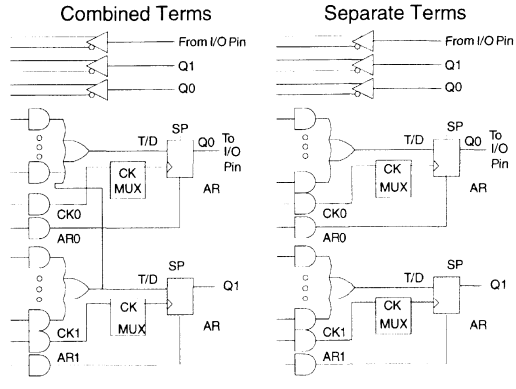
Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Logic Options

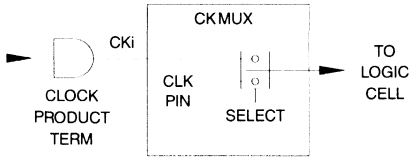
Combinatorial Output



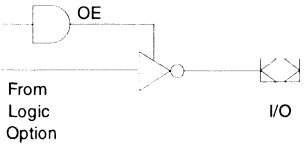
Registered Output

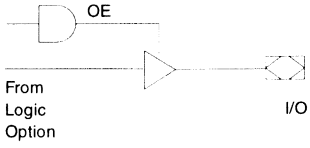


Clock MUX



Output Options





D.C. and A.C. Operating Conditions [1]

	Commercial -7, -10, -15	Commercial -25	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Note: 1. See ordering information for valid speed and temperature combination.

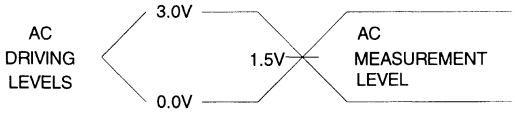
D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current, Standby	VCC = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		125	180	mA
				Ind.,Mil.		125	190	mA
			B-15, -25	Com.		125	180	mA
				Ind.,Mil.		125	190	mA
			BQ-10	Com.		60	90	mA
			BL-15, BQL-15, -25	Com.		15	30	mA
				Ind.,Mil.		15	30	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	BL-15, BQL-15, -25	Com.		10		mA/MHz (2)
				Ind.,Mil.		10		mA/MHz (2)
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage	4.5 ≤ V_{CC} ≤ 5.5 V			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	VIN = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA Com.,Ind.				0.5	V
			I_{OL} = 12 mA Mil.				0.5	V
			I_{OL} = 24 mA Com.				0.8	V
V_{OH}	Output High Voltage	VIN = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. See I_{CC} versus frequency characterization curves.

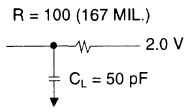
= Advance Information

Input Test Waveforms and Measurement Levels

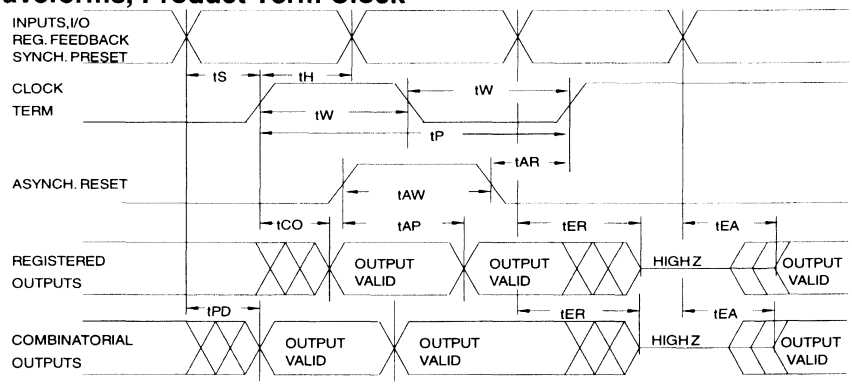


tR, tF < 3 ns (10% to 90%)

Output Test Load



A.C. Waveforms, Product Term Clock [1]



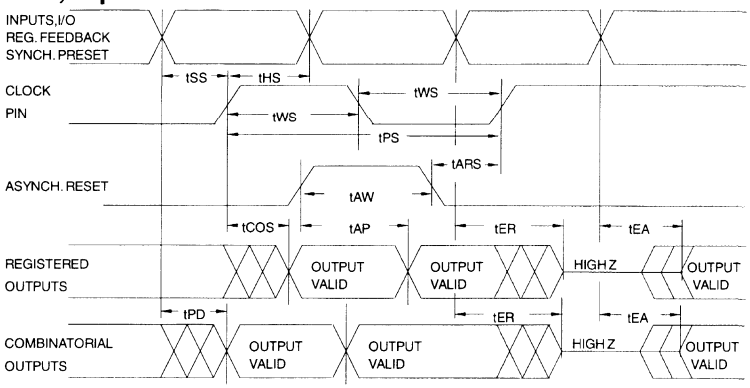
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics, Product Term Clock [1]

		-7		B/BQ -10		B/BL/BQL -15		B/BL/BQL -25		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	Min	Max	**Units**
t_{PD}	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
t_{EA}	Input to Output Enable		7.5		10		15		25	ns
t_{ER}	Input to Output Disable		7.5		10		15		25	ns
t_{CO}	Clock to Output	3	7.5	4	10	5	14	6	22	ns
t_{CF}	Clock to Feedback	1	5	4	7.5	5	9	5	10	ns
t_S	Input Setup Time	3		4		8/10		12		ns
t_{SF}	Feedback Setup Time	3		4		7		7		ns
t_H	Hold Time	1		2		5/7		5/7		ns
t_P	Clock Period	7		11		14		17		ns
t_W	Clock Width	3.5		5.5		7		8.5		ns
F_{MAX}	External Feedback $1/(t_S+t_{CO})$		95		71		45/41		29	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$		125		86		62		58	MHz
	No Feedback $1/(t_P)$		142		90		71		58	MHz
t_{AW}	Asynchronous Reset Width	5		10		15		20		ns
t_{AR}	Asynchronous Reset Recovery Time	3		10		15		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		8		12		15		25	ns
t_{SP}	Setup Time, Synchronous Preset	4		7		8		15		ns

Note: 1. See ordering information for valid part numbers.

A.C. Waveforms, Input Pin Clock[1]

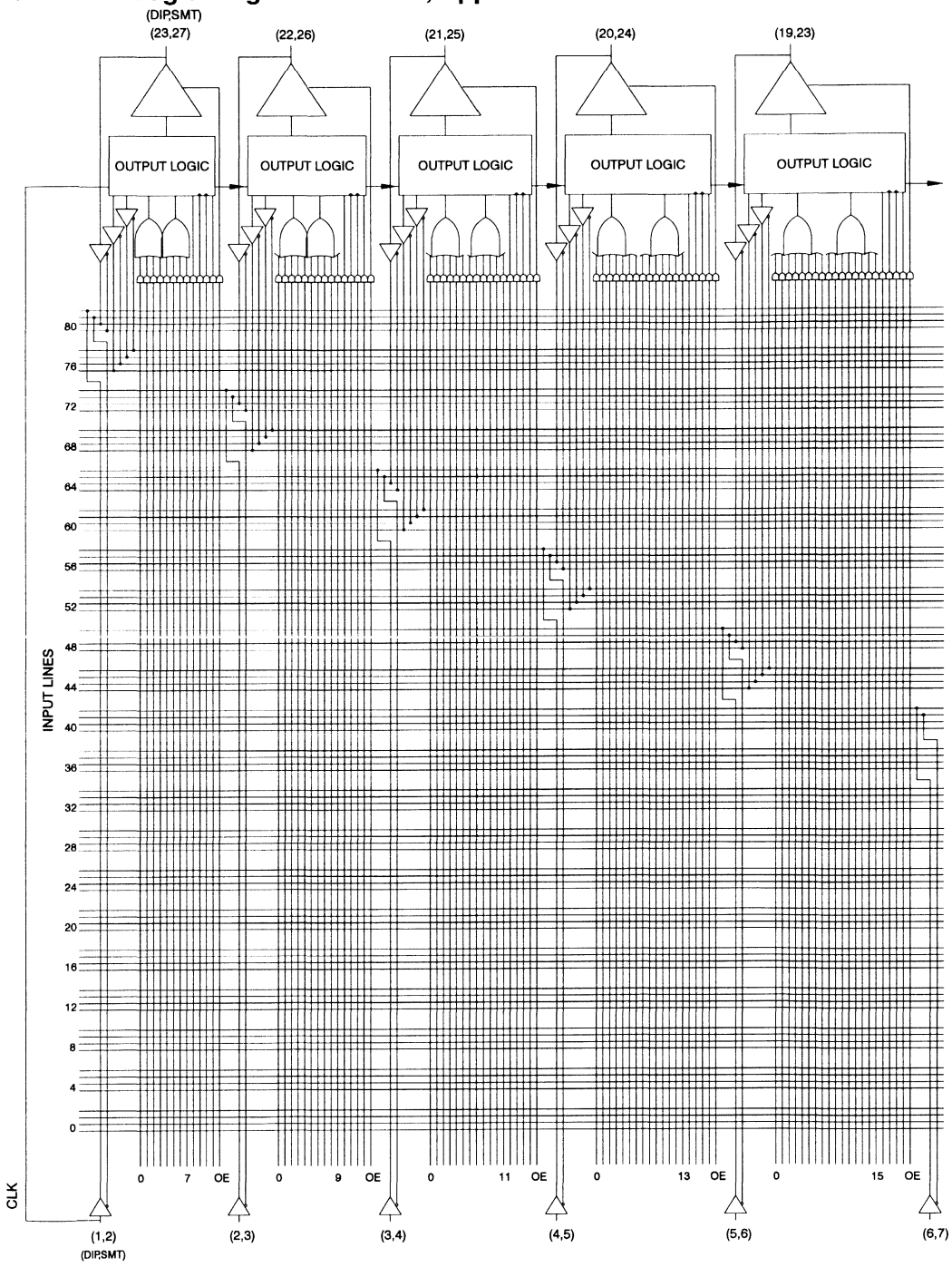


Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

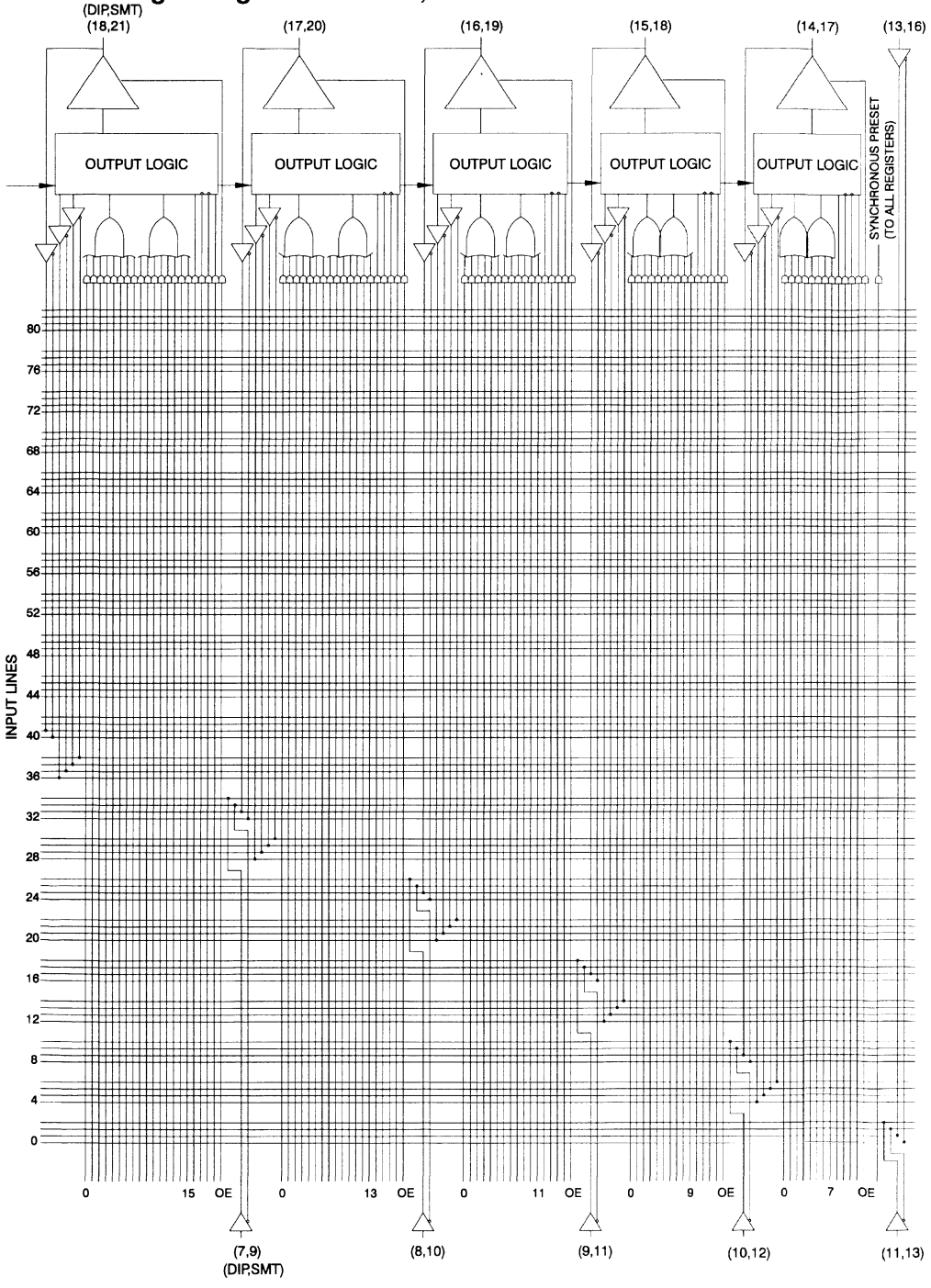
A.C. Characteristics, Input Pin Clock

		-7		B/BQ -10		B/BL/BQL -15		B/BL/BQL -25		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	Min	Max	**Units**
t_{PD}	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
t_{EA}	Input to Output Enable		7.5		10		15		25	ns
t_{ER}	Input to Output Disable		7.5		10		15		25	ns
t_{COS}	Clock to Output	0	6.5	0	7	0	9	0	15	ns
t_{CFS}	Clock to Feedback	0	3.5	0	5	0	5.5	0	7	ns
t_{SS}	Input Setup Time	4		5		8/10		9/12		ns
t_{SFS}	Feedback Setup Time	4		5		7		9		ns
t_{HS}	Hold Time	0		0		0		0		ns
t_{PS}	Clock Period	7		10		12		16		ns
t_{WS}	Clock Width	3.5		5		6		8		ns
F_{MAXS}	External Feedback $1/(t_{SS}+t_{COS})$		95		83		58/52		41/37	MHz
	Internal Feedback $1/(t_{SFS}+t_{CFS})$		133		100		80		62	MHz
	No Feedback $1/(t_{PS})$		142		100		83		62	MHz
t_{AW}	Asynchronous Reset Width	5		10		15		20		ns
t_{ARS}	Asynchronous Reset Recovery Time	5		10		15		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		8		10		15		25	ns
t_{SPS}	Setup Time, Synchronous Preset	5		5/9		11		15		ns

Functional Logic Diagram ATV750B, Upper Half

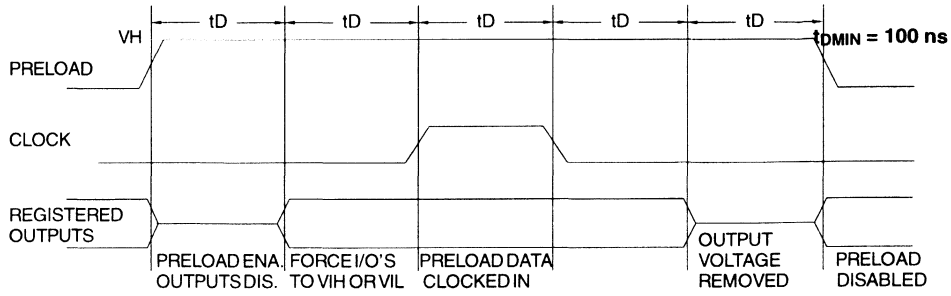


Functional Logic Diagram ATV750B, Lower Half



Preload of Registered Outputs

The ATV750B's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the output polarity. The PRELOAD state is entered by placing a 10.25 V to 10.75 V signal on pin 8 on DIPs, and lead 10 on SMDs. When the clock term is pulsed high, the data on the I/O pins is placed into the register chosen by the Select Pin.



Level forced on registered output pin during PRELOAD cycle	Select Pin State	Register #0 state after cycle	Register #1 State after cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

Power Up Reset

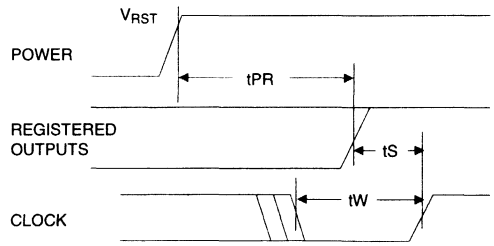
The registers in the ATV750Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Using the ATV750B's Many Advanced Features

The ATV750B's advanced flexibility packs more usable gates into 24 pins than any other logic device. The ATV750Bs start with the popular 22V10 architecture, and add several enhanced features:

- Selectable D- and T-Type Registers -
  Each ATV750B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- Selectable Asynchronous Clocks -
  Each of the ATV750B's flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- A Full Bank of Ten More Registers -
  The ATV750B provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.
- Independent I/O Pin and Feedback Paths -
  Each I/O pin on the ATV750B has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

Programming Software Support

As with all other Atmel PLDs, several third party development software products support the ATV750Bs. Several third party programmers support the ATV750B as well. Additionally, the ATV750B may be programmed to perform the ATV750/L's functional subset (no T-type flip-flops or pin clocking) using the ATV750/L JEDEC file. In this case, the ATV750B becomes a direct replacement or speed upgrade for the ATV750/L. The ATV750/L programming algorithm is different from the ATV750B algorithm. Choose the appropriate device in your programmer menu to ensure proper programming. Please refer to the *Programmable Logic Development Tools* section for a complete PLD software and programmer listing.

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750B. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750B fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

Erasure Characteristics

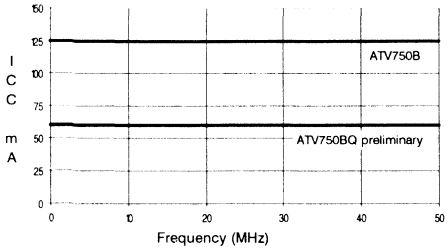
The entire memory array of an ATV750B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

Atmel CMOS PLDs

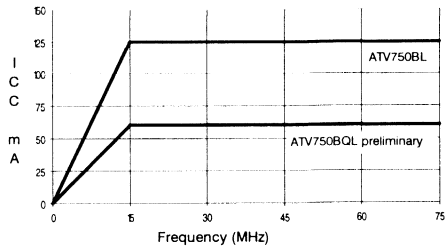
The ATV750B utilizes an advanced 0.65-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

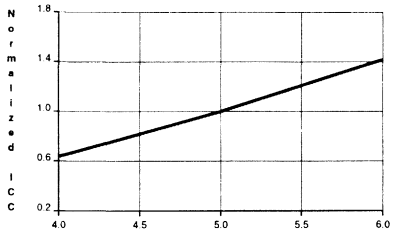
SUPPLY CURRENT vs. INPUT FREQUENCY
ATV750B (TA=25°C, VCC=5V)



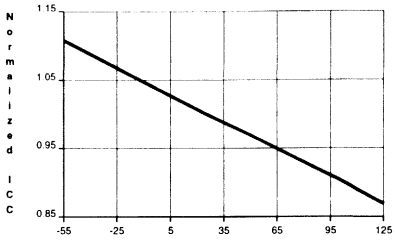
SUPPLY CURRENT vs. INPUT FREQUENCY
ATV750BL (TA=25°C, VCC=5V)



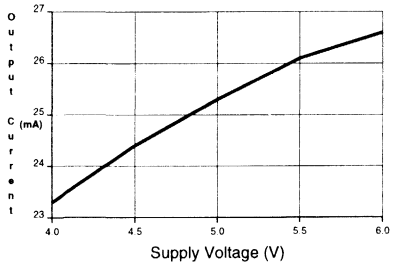
NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



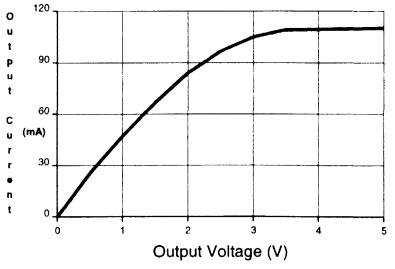
NORMALIZED ICC vs. AMBIENT TEMP.
f = 50 MHz



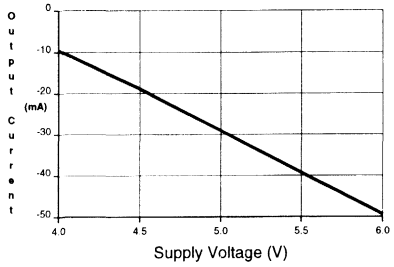
OUTPUT SINK CURRENT
vs. SUPPLY VOLTAGE (VOL = 0.5V)



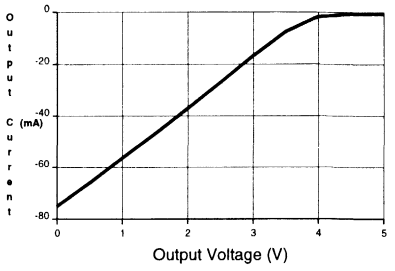
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



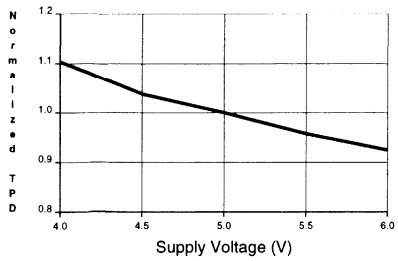
OUTPUT SOURCE CURRENT
vs. SUPPLY VOLTAGE (VOH = 2.4V)



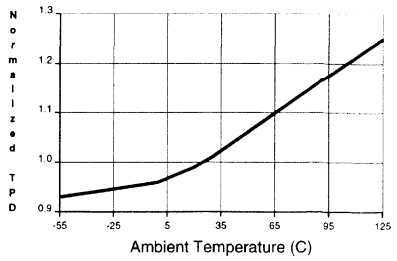
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



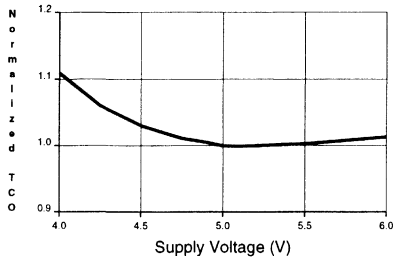
NORMALIZED TPD
vs. SUPPLY VOLTAGE



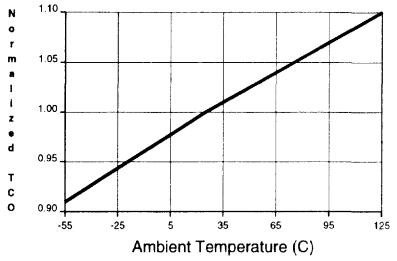
NORMALIZED TPD
vs. TEMPERATURE



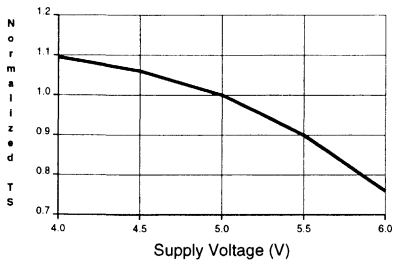
NORMALIZED TCO
vs. SUPPLY VOLTAGE



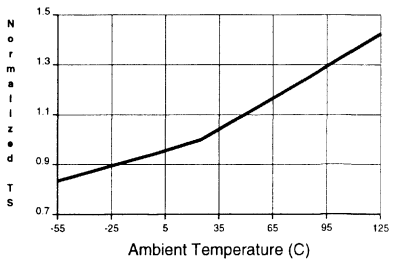
NORMALIZED TCO
vs. TEMPERATURE



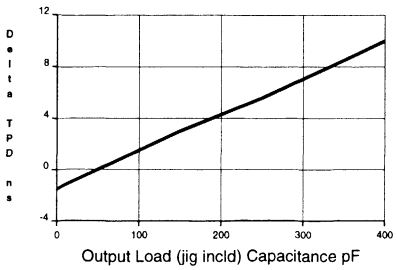
NORMALIZED TS
vs. SUPPLY VOLTAGE



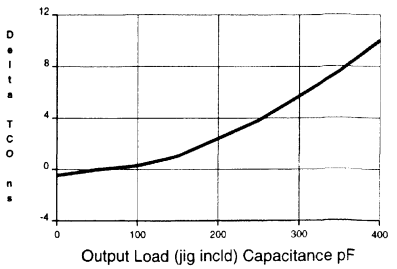
NORMALIZED TS
vs. TEMPERATURE



DELTA TPD vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



DELTA TCO vs. OUTPUT LOADING
(VCC = 4.5V, OUTPUT LOAD = COMMERCIAL)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
7.5	6.5	95	ATV750B-7DC ATV750B-7JC ATV750B-7PC	24DW3 28J 24P3	Commercial (0°C to 70°C)
10	7	83	ATV750B-10DC ATV750B-10JC ATV750B-10PC ATV750B-10SC	24DW3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-10DI ATV750B-10JI ATV750B-10PI ATV750B-10SI	24DW3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-10DM ATV750B-10LM	24DW3 28LW	Military
			ATV750B-10DM/883 ATV750B-10LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	58	ATV750B-15DC ATV750B-15JC ATV750B-15PC ATV750B-15SC	24DW3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-15DI ATV750B-15JI ATV750B-15PI ATV750B-15SI	24DW3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-15DM ATV750B-15LM	24DW3 28LW	Military (-55°C to 125°C)
			ATV750B-15DM/883 ATV750B-15LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	41	ATV750B-25DC ATV750B-25JC ATV750B-25PC ATV750B-25SC	24DW3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-25DI ATV750B-25JI ATV750B-25PI ATV750B-25SI	24DW3 28J 24P3 24S	Industrial (-40°C to 85°C)
10	7	83	5962-88726 08 LA 5962-88726 08 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	9	58	5962-88726 09 LA 5962-88726 09 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	41	5962-88726 10 LA 5962-88726 10 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	9	92	ATV750BL-15DC ATV750BL-15JC ATV750BL-15PC ATV750BL-15SC	24DW3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750BL-15DI ATV750BL-15JI ATV750BL-15PI ATV750BL-15SI	24DW3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750BL-15DM ATV750BL-15LM	24DW3 28LW	Military (-55°C to 125°C)
			ATV750BL-15DM/883 ATV750BL-15LM/883	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	37	ATV750BL-25DC ATV750BL-25JC ATV750BL-25PC ATV750BL-25SC	24DW3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750BL-25DI ATV750BL-25JI ATV750BL-25PI ATV750BL-25SI	24DW3 28J 24P3 24S	Industrial (-40°C to 85°C)
15	9	92	5962-88726 11 LX 5962-88726 11 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	37	5962-88726 12 LX 5962-88726 12 3X	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
10	7.5	7	ATV750BQ-10JC ATV750BQ-10PC	28J 24P3	Commercial (0°C to 70°C)
15	12	10	ATV750BQL-15JC ATV750BQL-15PC ATV750BQL-15SC	28J 24P3 24S	Commercial (0°C to 70°C)
25	15	12	ATV750BQL-25JC ATV750BQL-25PC ATV750BQL-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750BQL-25JI ATV750BQL-25PI ATV750BQL-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750BQL-25GM ATV750BQL-25NM	24D3 28L	Military (-55°C to 125°C)
			ATV750BQL-25GM/883 ATV750BQL-25NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

= Advance Information

Package Type	
24DW3	24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
28LW	28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

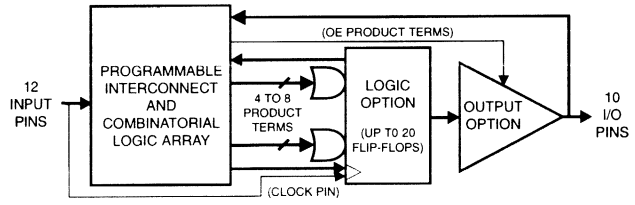
High Speed UV Erasable Programmable Logic Device

Advance Information

Features

- 3-Volt Operation - Low System Power Requirement
- Wide V_{CC} Range
  - V_{CC} = 3.0 V to 5.25 V (Commercial)
  - V_{CC} = 3.0 V to 5.5 V (Industrial)
- Advanced, High Speed Programmable Logic Device
  - 10 ns Maximum Pin-To-Pin Delay
  - Enhanced Logic Flexibility
  - Architecture Identical to ATV750B/BL
  - Backward Compatible with ATV750/L Software and Hardware
- Low Power, Low Voltage ATLV750BL - 0.5 mA Standby (Typical) at 3.6 V
- New Flip-Flop Features
  - D- or T-Type
  - Product Term or Direct Input Pin Clocking
- Highest Density Programmable Logic Available in a 24-Pin Package
- Increased Logic Flexibility
  - 42 Array Inputs, 20 Sum Terms and 20 Flip-Flops
- Enhanced Output Logic Flexibility
  - All 20 Flip-Flops Feed Back Internally
  - 10 Flip-Flops are Also Available as Outputs
- Reprogrammable - 100% Tested for Programming
- Full Commercial and Industrial Temperature Ranges
- 24-Pin, 0.300" DIP, 24-Lead SOIC, and 28-Lead Surface Mount Packages

Logic Diagram



Description

The ATLV750Bs are twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High speed logic and uniform, predictable delays guarantee fast in-system performance.

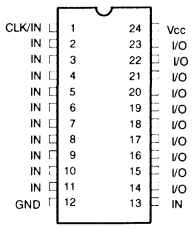
Each of the ATLV750B's 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either

(continued)

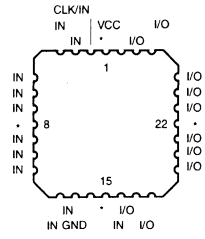
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
Vcc	+5 V Supply

DIP/SOIC



PLCC/LCC



0426A

Description (Continued)

D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. A variable format is used to assign between four to eight product terms per sum term. There are two sum terms per output, providing added flexibility. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATLV750B and ATLV750BL are low voltage and low power devices with speeds as fast as 10 ns. Architecturally identical to the ATV750B/BL, the ATLV750B/BL satisfies most low voltage, low power portable design requirements. The ATLV750BL provides the optimum low power PLD solution, with full CMOS output levels. Standby power dissipation is as low as 15 mW at 3.6-V operation. This device significantly reduces total system power, thereby allowing battery-powered operation.

D.C. and A.C. Operating Conditions

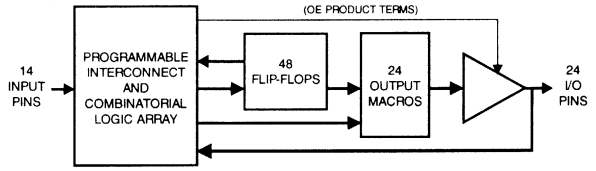
	Commercial -10, -15	Industrial -10, -15
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0 V to 5.25 V	3.0 V to 5.5 V

High Density UV Erasable Programmable Logic Device

Features

- **Third Generation Programmable Logic Structure**
  - **Easily Achieves Gate Utilization Factors of 80 Percent**
- **Increased Logic Flexibility**
  - **86 Inputs and 72 Sum Terms**
- **Flexible Output Macrocell**
  - **48 Flip-Flops - 2 per Macrocell**
  - **3 Sum Terms - Can Be OR'ed and Shared**
- **High Speed**
- **Low Power - Less than 0.5 mA Typical (ATV2500L)**
- **Multiple Feedback Paths Provide for Buried State Machines and I/O Bus Compatibility**
- **Asynchronous Clocks and Resets**
  - **Multiple Synchronous Presets - One per Four or Eight Flip-Flops**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **40-pin Dual-In-line and 44-Lead Surface Mount Packages**

Block Diagram



Description

The ATV2500H/L is the most powerful programmable logic device available in a 40-pin package. Increased product terms, sum terms, and flip-flops translate into many more usable gates. High gate utilization is easily obtainable.

The ATV2500H/L is organized around a global bus. All pin and feedback terms are always available to every logic cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 flip-flops.

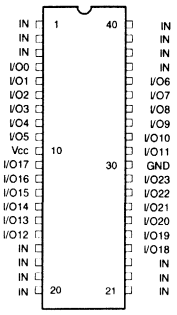
There are 416 product terms available. Four product terms are input to each sum term. The three sum terms per logic cell can be combined to provide up to 12 product terms, combinatorial and registered. Independent of output configuration, the two flip-flops are always usable, and always have at least four product term inputs.

(continued)

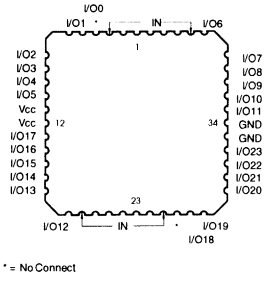
Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
*	No Internal Connection
Vcc	+5 V Supply

DIP



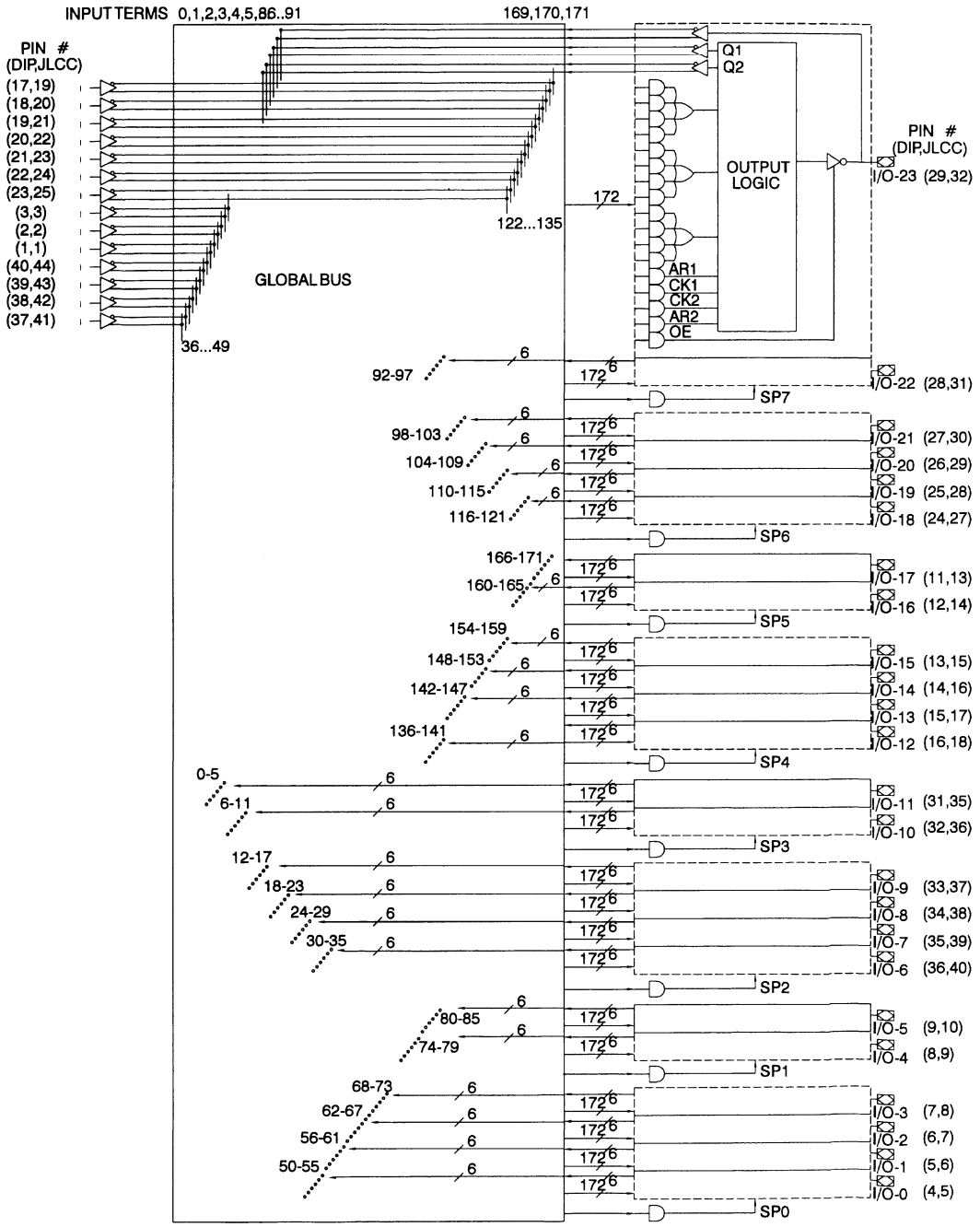
PLCC/LCC



* = No Connect

0025C

Functional Logic Diagram ATV2500H/L



Description (Continued)

Product terms are available providing asynchronous resets, flip-flop clocks, and output enables. One reset and one clock term are provided per flip-flop, with one enable term per output. Eight product terms provide local synchronous presets, divided up into banks of four and eight flip-flops. Register preload and buried register observability simplify testing. The device has an internal power up clear function.

Functional Logic Diagram Description

The ATV2500H/L Functional Logic Diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the global bus.

The ATV2500H/L is a straightforward and uniform PLD. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) flip-flop Q2 true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

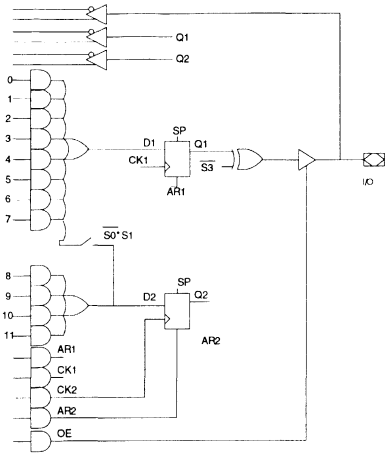
Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

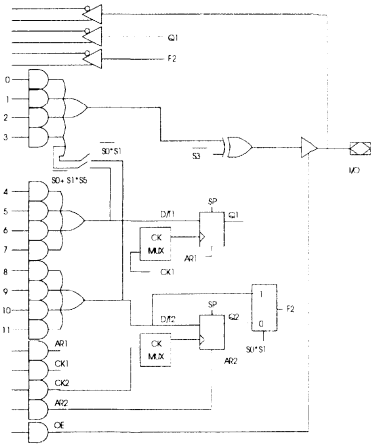
*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Output Logic, Registered [1]



Output Logic, Combinatorial [1]



Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

S2	S1	S0	Terms In D1	Terms In D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4(1)	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

S2	S1	S0	Terms In D1	Terms In D2	Output Configuration
1	0	0	4(1)	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4(1)	4(1)	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

S3	Output Configuration
0	Active Low
1	Active High

D.C. and A.C. Operating Conditions

		ATV2500H-25	ATV2500H/L-30	ATV2500H/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	ATV2500L	Com.		0.5	5	mA
				Ind.,Mil.		0.5	10	mA
			ATV2500H	Com.		80	160	mA
				Ind.,Mil.		80	180	mA
I_{CC2}	Clocked Power Supply Current (ATV2500L)	V_{CC} = MAX Outputs Open		Com.		15 (2)		mA/MHz
				Ind.,Mil.		15 (2)		mA/MHz
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA			V_{CC}-0.3			V
		I_{OH} = -4.0 mA			2.4			V

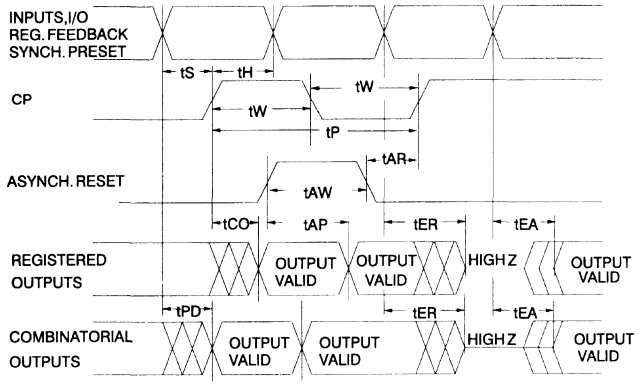
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sam pled and is not 100% tested. See Absolute Maximum Ratings.
2. See I_{CC} vs. Frequency characterization curves.

Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Waveforms [1]



Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics for the ATV2500L

Symbol	Parameter	ATV2500L-30		ATV2500L-35		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		30		35	ns
t_{EA}	Input to Output Enable		30		35	ns
t_{ER}	Input to Output Disable		30		35	ns
t_{CO}	Clock to Output	5	30	5	35	ns
t_{CF}	Clock to Feedback	10	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	20		22		ns
t_{SI2}	Input Setup Time, Buried Register[1]	20		22		ns
t_{SF}	Feedback Setup Time	10		15		ns
t_{H1}	Hold Time, Output Register	10		15		ns
t_{H2}	Hold Time, Buried Register[1]	5		5		ns
t_W	Clock Width	15		17		ns
t_P	Clock Period	30		35		ns
F_{MAX}	Maximum Frequency (1/t_P)		33		28	MHz
t_{AW}	Asynchronous Reset Width	18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35	ns

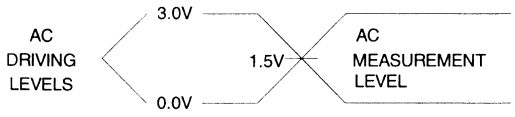
Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

A.C. Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25		ATV2500H-30		ATV2500H-35		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register(1)	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency (1/t_P)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

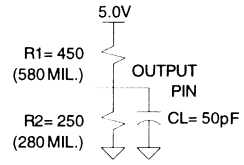
Note: 1. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

Input Test Waveforms and Measurement Levels



tR, tF < 5 ns (10% to 90%)

Output Test Load

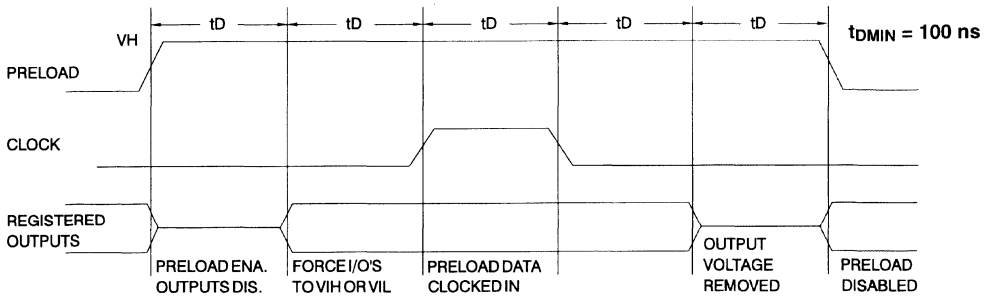


Preload and Observability of Registered Outputs

The ATV2500H/L's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The preload state is entered by placing an 11 V to 14 V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 11 V to 14 V signal on pin 2 (DIP or SMP). In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.



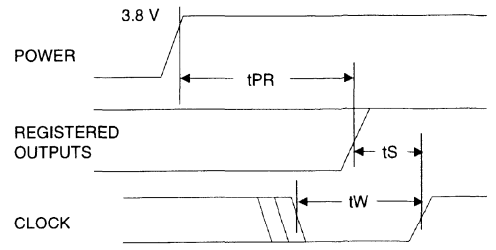
Level forced on Odd I/O pin during preload cycle.	Q Select pin state	Even/ Odd select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

The registers in the ATV2500H/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500H/L fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits preload and Q2 observability.

Atmel CMOS PLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64K to one-megabit devices.

Using the ATV2500H/L's Many Advanced Features

The ATV2500H/L's flexibility puts more usable gates in 40 pins than other PLDs. Some of the ATV2500H/L's key features are:

- Asynchronous Clocks -

Each of the flip-flops in the ATV2500H/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500H/L clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500H/L provides two flip-flops for each output macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own sum term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's output enable, facilitates designs using bi-directional I/O buses.

- Three Sum Terms per Macrocell -

The ATV2500H/L macrocell can be configured with one SUM term feeding the output, and still have two SUM terms feeding the flip-flops. This is the simplest method for interfacing with an I/O bus, and no flip-flops need be sacrificed.

- Combinable Sum Terms -

Each output macrocell's three SUM terms can be combined in an OR gate before the output or the register. This provides up to 12 product terms per output or flip-flop. When the registered output configuration is chosen, eight terms are automatically available to D1. The four terms feeding D2 can also be shared with D1, giving it a total of 12. In the combinatorial mode, four, eight, or 12 terms can feed the output, with the middle four still driving D1 and the bottom four still driving D2.

Programming Software Support

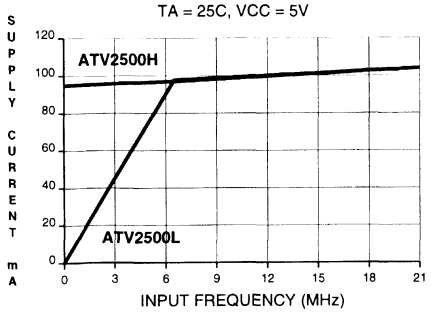
Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500H/L is currently available from several PLD software vendors. Please refer to the *Programmable Logic Development Tools* section for a complete listing of the PLD software support.

Erasure Characteristics

The entire memory array of an ATV2500H/L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

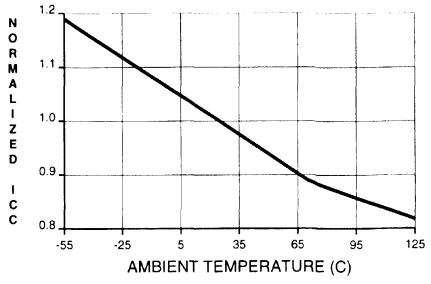
SUPPLY CURRENT vs. INPUT FREQUENCY

TA = 25C, VCC = 5V



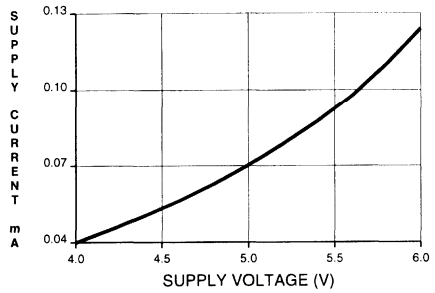
NORMALIZED ICC vs. AMBIENT TEMP.

f = 20 MHz, VCC = 5V



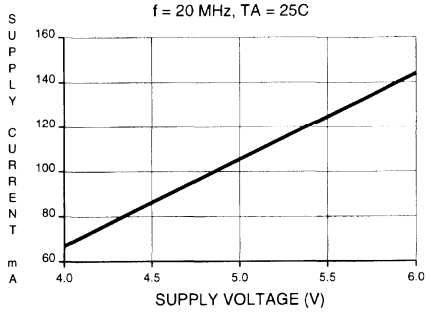
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 0 HZ, TA = 25C



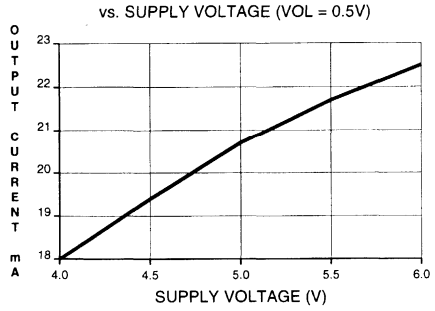
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 20 MHz, TA = 25C



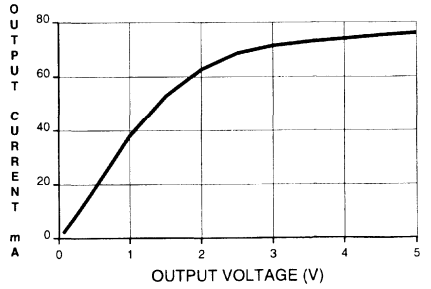
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



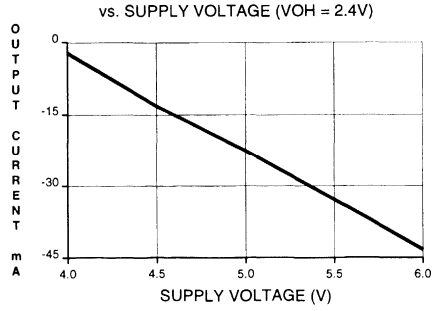
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



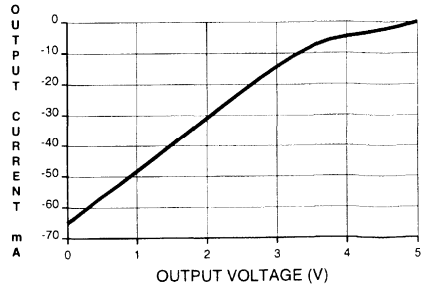
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

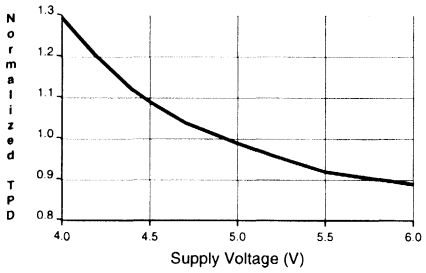


OUTPUT SOURCE CURRENT

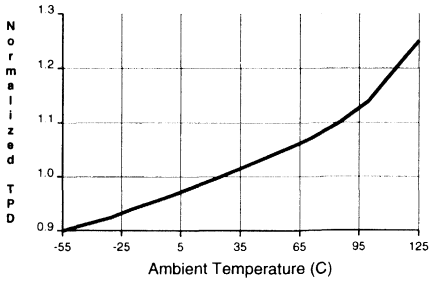
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



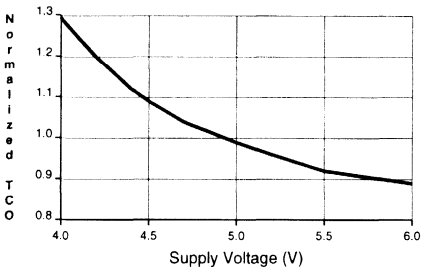
NORMALIZED TPD
vs. SUPPLY VOLTAGE



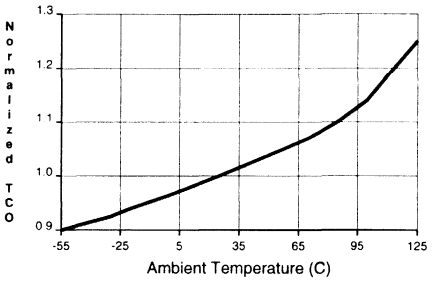
NORMALIZED TPD
vs. TEMPERATURE



NORMALIZED TCO
vs. SUPPLY VOLTAGE

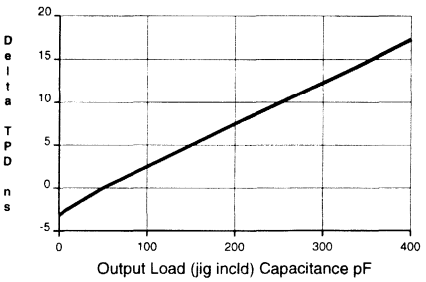


NORMALIZED TCO
vs. TEMPERATURE



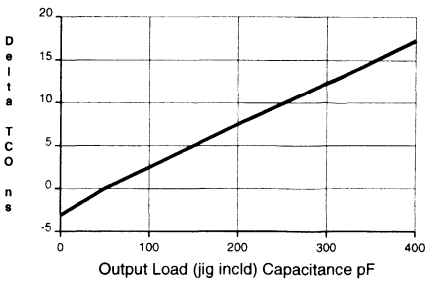
DELTA TPD vs. OUTPUT LOADING

TA = 25C, VCC = 5V



DELTA TCO vs. OUTPUT LOADING

TA = 25C, VCC = 5V



Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
25	25	40	5962-91545 02M QA 5962-91545 02M XX 5962-91545 02M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

	Package Type
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500L-30DC ATV2500L-30JC ATV2500L-30KC ATV2500L-30LC ATV2500L-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-30DI ATV2500L-30JI ATV2500L-30KI ATV2500L-30LI ATV2500L-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500L-30DM ATV2500L-30KM ATV2500L-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500L-30DM/883 ATV2500L-30KM/883 ATV2500L-30LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500L-35DC ATV2500L-35JC ATV2500L-35KC ATV2500L-35LC ATV2500L-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500L-35DI ATV2500L-35JI ATV2500L-35KI ATV2500L-35LI ATV2500L-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
30	30	33	5962-91545 03M QA 5962-91545 03M XX 5962-91545 03M YX	40DW6 44LW 44KW	Military/833C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

High Speed High Density UV Erasable Programmable Logic Device

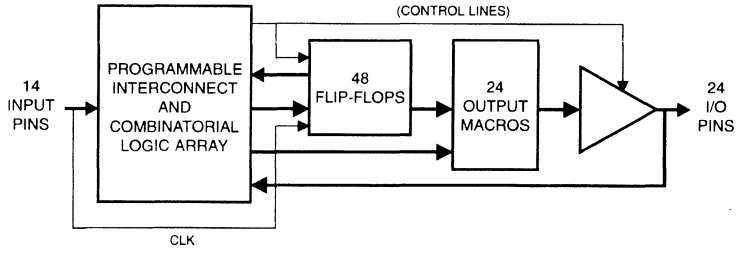
Features

- High Performance, High Density Programmable Logic Device
  - Typical 7 ns Pin-to-Pin Delay
  - Fully Connected Logic Array With 416 Product Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - Two per Macrocell
  - 72 Sum Terms
  - All Flip-Flops, I/O Pins Feed In Independently
  - Achieves Over 80% Gate Utilization
- Enhanced Macrocell Configuration Selections
  - D- or T-Type Flip-Flops
  - Product Term or Direct Input Pin Clocking
  - Registered or Combinatorial Internal Feedback
- Several Power Saving Options

Device	Icc, Stand-By
ATV2500B	110 mA
ATV2500BQ	30 mA
ATV2500BL	2 mA
ATV2500BQL	2 mA

- Backward Compatible With ATV2500H/L Software
- Proven and Reliable High Speed UV EPROM Process
- Reprogrammable - Tested 100% for Programmability
- 40-pin Dual-In-Line and 44-Pin Lead Surface Mount Packages

Block Diagram

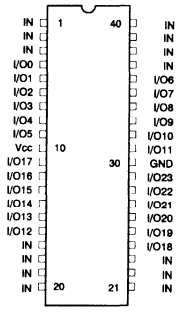


Pin Configurations

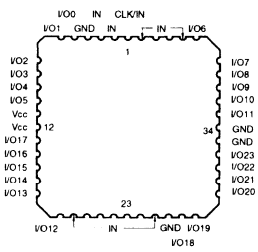
Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bidirectional Buffers
I/O 0,2,4..	"Even" I/O Buffers
I/O 1,3,5..	"Odd" I/O Buffers
GND	Ground
Vcc	+5 V Supply

Note: 1. For ATV2500BQ and ATV2500BQL (PLCC/LCC package only) pin 4 and pin 26 connections are not required.

DIP

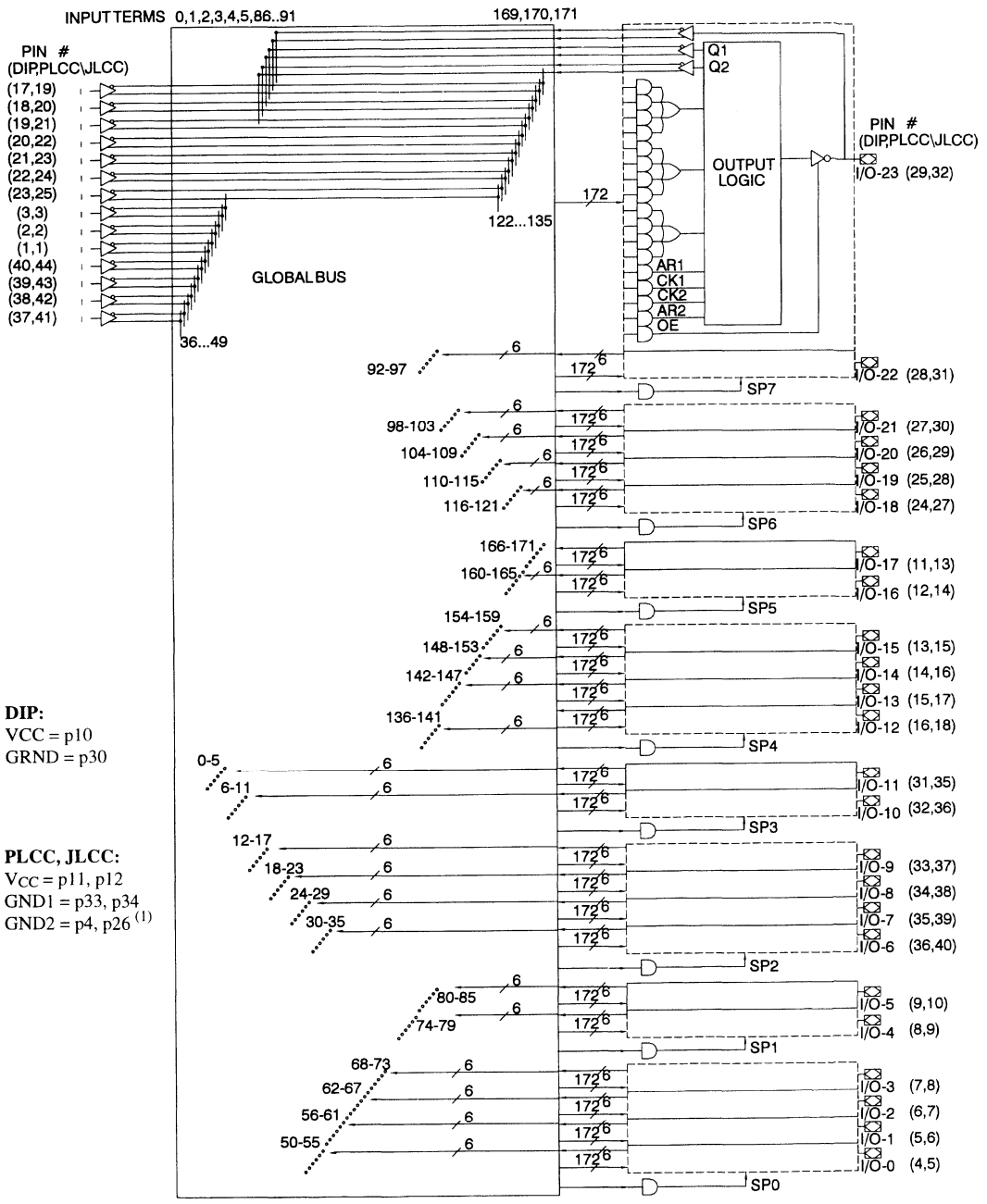


PLCC



0249D

Functional Logic Diagram ATV2500B



DIP:
VCC = p10
GRND = p30

PLCC, JLCC:
V_{CC} = p11, p12
GND1 = p33, p34
GND2 = p4, p26 (1)

Note: 1. Not required for PLCC versions of ATV2500BQ or ATV2500BQL, making them compatible with ATV2500H and ATV2500L pinout.

Description

The ATV2500Bs are the highest density PLDs available in a 40- or 44-pin package. With their fully connected logic array and flexible macrocell structure, high gate utilization is easily obtainable.

The ATV2500Bs are organized around a *single universal and-or array*. All pin and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

In the ATV2500Bs, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with *no performance penalty*. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

Several low power device options allow selection of the optimum solution for many power-sensitive applications. Each of the options significantly reduces total system power and enhances system reliability.

Functional Logic Diagram Description

The ATV2500B functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

The ATV2500Bs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2[1] true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be fed back in the ATV2500Bs.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

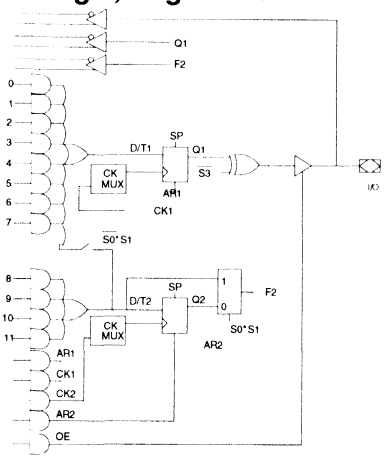
	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

Pin Capacitance (f = 1 MHz, T = 25°C) (1)

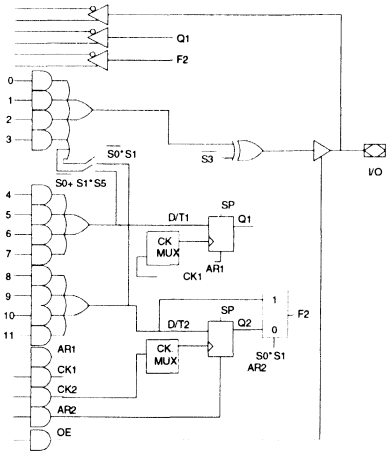
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Logic, Registered [1]



Output Logic, Combinatorial [1]



Note: 1. These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

S2 = 0		Terms In		
S1	S0	D/T1	D/T2	Output Configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4[1]	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

Note: 1. These four terms are shared with D/T1.

S2 = 1			Terms In		
S5	S1	S0	D/T1	D/T2	Output Configuration
X	0	0	4[1]	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4[1]	4[1]	Combinatorial (12 Terms); Q2 FB
1	1	1	4[1]	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

S3	Output Configuration
0	Active Low
1	Active High

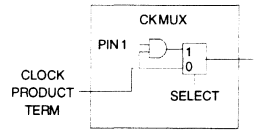
S6	Q1 CLOCK
0	CK1
1	CK1 • PIN1

S4	Register 1 Type
0	D
1	T

S7	Q2 CLOCK
0	CK2
1	CK2 • PIN1

S5	Register 2 Type
0	D
1	T

Clock Option

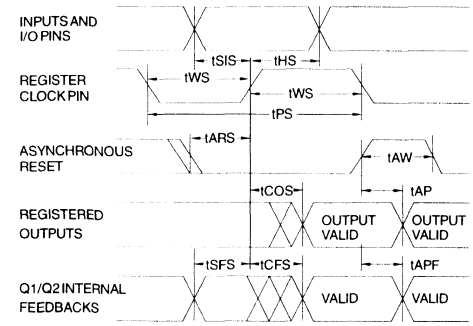


D.C. Characteristics

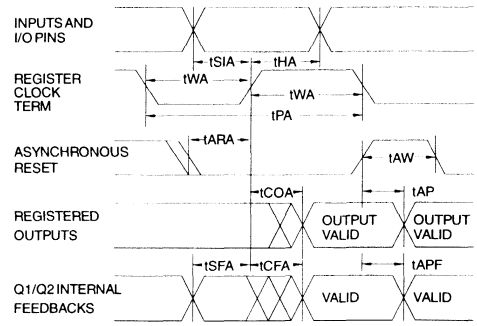
Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATV2500B	Com.		110	190	mA
				Ind., Mil.		110	210	mA
			ATV2500BQ	Com.		30	70	mA
				Ind., Mil.		30	85	mA
			ATV2500BL	Com.		2	5	mA
				Ind., Mil.		2	10	mA
			ATV2500BQL	Com.		2	4	mA
				Ind., Mil.		2	5	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX Outputs Open V_{IN} = GND or V_{CC}	ATV2500BL	Com.		6		mA/MHz(1)
				Ind., Mil.		6		mA/MHz(1)
			ATV2500BQL	Com.		8		mA/MHz(1)
				Ind., Mil.		8		mA/MHz(1)
I_{OS} (2)	Output Short Circuit Current	V_{OUT} = 0.5 V					-120	mA
V_{IL}	Input Low Voltage	MIN ≤ V_{CC} ≤ MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5 V;	I_{OL} = 8 mA Com,Ind				0.5	V
			I_{OL} = 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

Notes: 1. See Icc versus frequency characterization curves.
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

A.C. Waveforms [1]
Input Pin Clock



A.C. Waveforms [1]
Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

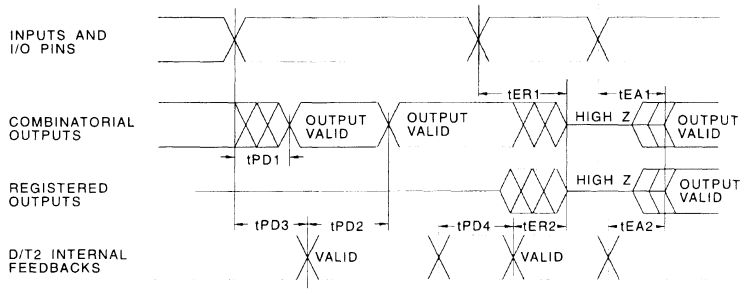
Register A.C. Characteristics, Input Pin Clock

Symbol	Parameter	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-30 Min	-30 Max	Units
t_{COS}	Clock to Output		7.5		10		11		12		15	ns
t_{CFS}	Clock to Feedback	0	4	0	5	0	6	0	7	0	8	ns
t_{SIS}	Input Setup Time	7		9		14		20		23		ns
t_{SFS}	Feedback Setup Time	7		9		14		20		23		ns
t_{HS}	Hold Time	0		0		0		0		0		ns
t_{WS}	Clock Width	5		6		7		8		9		ns
t_{PS}	Clock Period	10		12		14		16		18		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		69		52		40		31		26	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		90		71		50		37		32	MHz
	No Feedback $1/(t_{PS})$		100		83		71		62		55	MHz

Register A.C. Characteristics, Product Term Clock

Symbol	Parameter	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-30 Min	-30 Max	Units
t_{COA}	Clock to Output		12		15		20		22		25	ns
t_{CFA}	Clock to Feedback	3	7	5	12	10	16	12	18	13	20	ns
t_{SIA}	Input Setup Time	4		5		10		15		19		ns
t_{SFA}	Feedback Setup Time	4		5		8		10		10		ns
t_{HA}	Hold Time	3		5		10		12		13		ns
t_{WA}	Clock Width	5.5		7.5		11		14		15		ns
t_{PA}	Clock Period	11		15		22		28		30		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		62.5		50		33		27		23	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		90		58		38		36		24	MHz
	No Feedback $1/(t_{PS})$		90		66		45		36		33	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	3		8		12		15		18		ns

A.C. Waveforms [1]
Combinatorial Outputs and Feedback

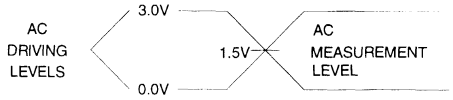


Notes: 1. Timing measurement reference is 1.5 V Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

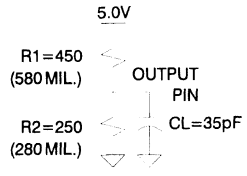
Symbol	Parameter	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-30 Min	-30 Max	Units
t_{PD1}	Input to Non-Registered Output		12		15		20		25		30	ns
t_{PD2}	Feedback to Non-Registered Output		12		15		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback		8		11		15		18		20	ns
t_{PD4}	Feedback to Non-Registered Feedback		8		11		15		18		20	ns
t_{EA1}	Input to Output Enable		12		15		20		25		30	ns
t_{ER1}	Input to Output Disable		12		15		20		25		30	ns
t_{EA2}	Feedback to Output Enable		12		15		20		25		30	ns
t_{ER2}	Feedback to Output Disable		12		15		20		25		30	ns
t_{AW}	Asynchronous Reset Width	6		8		12		15		18		ns
t_{AP}	Asynchronous Reset to Registered Output		15		18		22		28		30	ns
t_{APF}	Asynchronous Reset to Registered Feedback		12		15		19		25		30	ns

Input Test Waveforms and Measurement Levels



t_R, t_F < 3 ns (10% to 90%)

Output Test Load

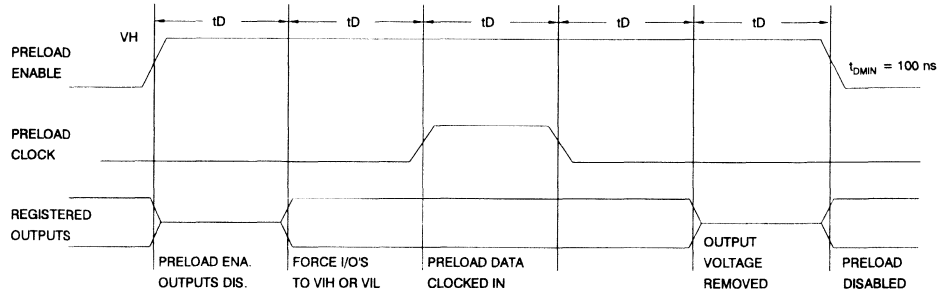


Preload and Observability of Registered Outputs

The ATV2500Bs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 10.25 V to 10.75 V signal on SMP lead 42. When the preload clock SMP lead 23 is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 10.25 V to 10.75 V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.



Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}/V_{IL}	Low	Low	High/Low	X	X	X
V_{IH}/V_{IL}	High	Low	X	High/Low	X	X
V_{IH}/V_{IL}	Low	High	X	X	High/Low	X
V_{IH}/V_{IL}	High	High	X	X	X	High/Low

Power Up Reset

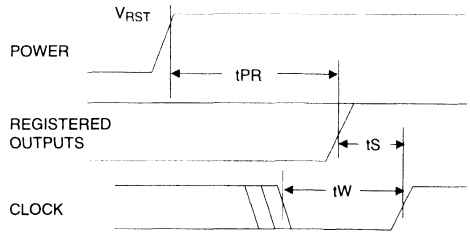
The registers in the ATV2500Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of ATV2500B fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS PLDs

The ATV2500Bs utilize an advanced 0.65-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

Using the ATV2500Bs Many Advanced Features

The ATV2500Bs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATV2500Bs key features are:

- Fully Connected Logic Array -

Each array input is always available to every product term. This makes logic placement a breeze.

- Selectable D- and T-Type Registers -

Each ATV2500B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

- Buried Combinatorial Feedback -

Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.

- Selectable Synchronous/Asynchronous Clocking -

Each of the ATV2500Bs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

- A Total of 48 Registers -

The ATV2500B provides two flip-flops per macrocell - a total of 48. Each register has its own clock and reset terms, as well as its own sum term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500B has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.

- Combinable Sum Terms -

Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with *no speed penalty.*

Programming Software Support

As with all other Atmel PLDs, several third party PLD development software products and programmers will support the ATV2500Bs.

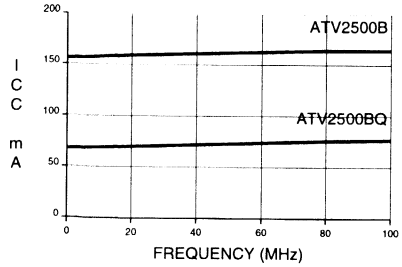
Several third party programmers will support the ATV2500B as well. Additionally, the ATV2500B may be programmed to perform the ATV2500H/Ls functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H/L JEDEC file. In this case, the ATV2500B becomes a direct replacement or speed upgrade for the ATV2500H/L (additional GND connections are required). Please refer to the Programmable Logic Development Tools section for a complete PLD software and programmer listing.

Erasure Characteristics

The entire memory array of an ATV2500B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

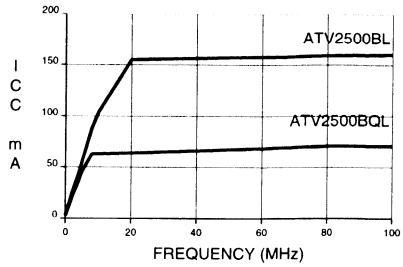
SUPPLY CURRENT vs. INPUT FREQUENCY

ATV2500B/BQ (VCC = 5V, TA = 25C)



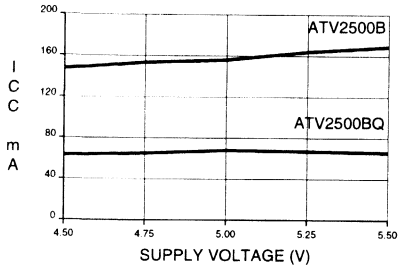
SUPPLY CURRENT vs. INPUT FREQUENCY

ATV2500BL,BQL (VCC = 5V, TA = 25C)



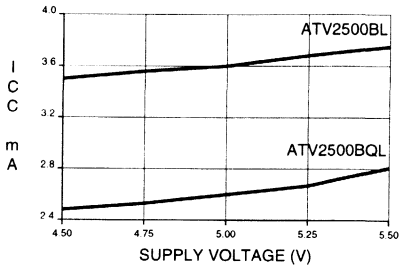
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATV2500B/BQ (TA = 25C)



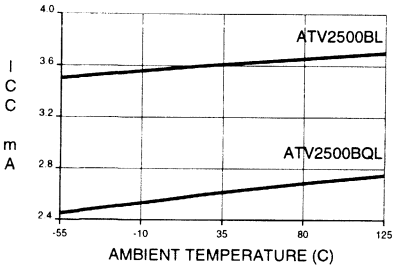
SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATV2500BL/BQL (TA = 25C)



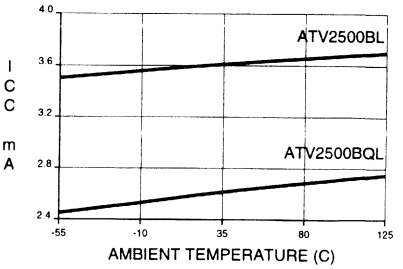
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATV2500BL/BQL (VCC = 5V)



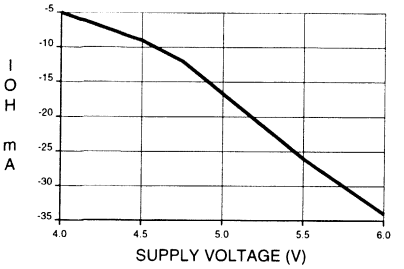
SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATV2500BL/BQL (VCC = 5V)



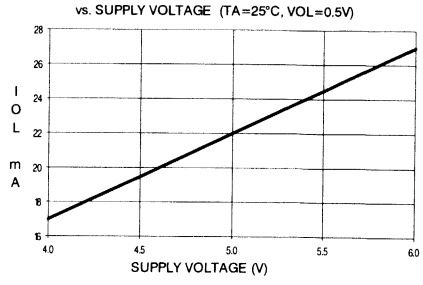
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

(TA = 25C, VOH = 2.4 V)

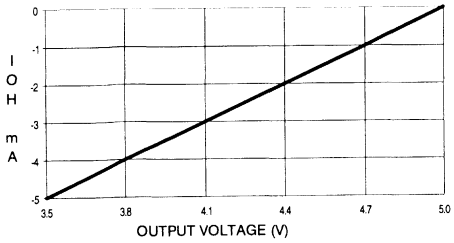


OUTPUT SINK CURRENT

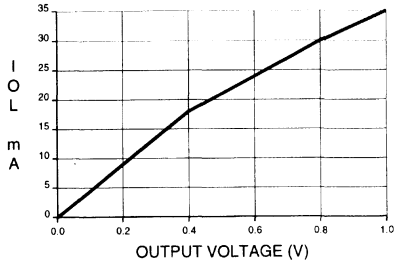
vs. SUPPLY VOLTAGE (TA=25°C, VOL=0.5V)



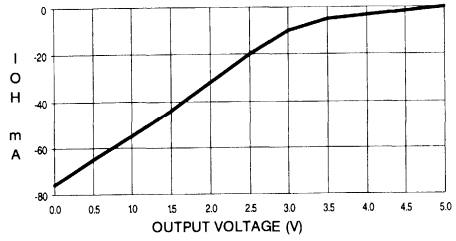
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC=5V, TA=25°C)



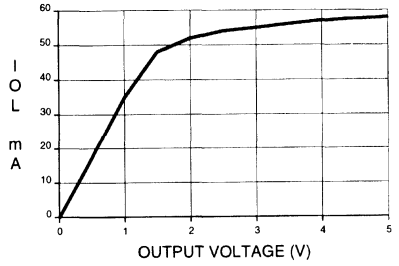
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



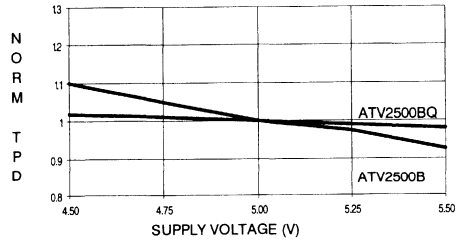
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC=5V, TA=25°C)



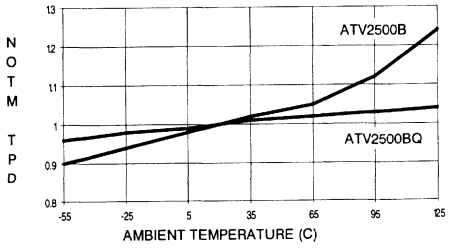
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



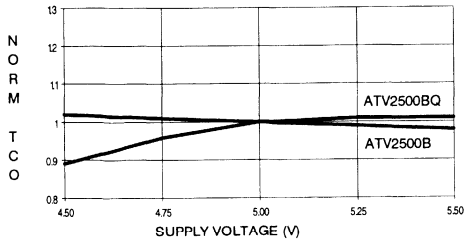
NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA=25°C)



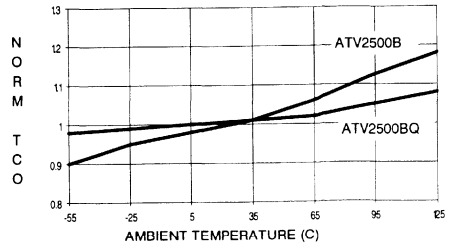
NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC=5V)



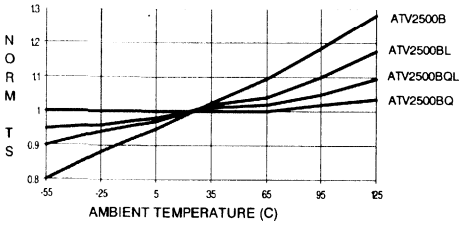
NORMALIZED TCO
vs. SUPPLY VOLTAGE (TA=25°C)



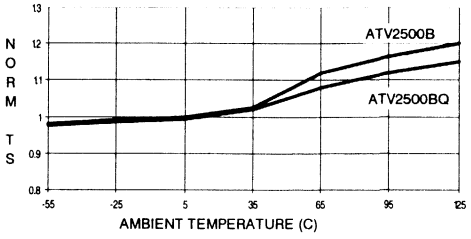
NORMALIZED TCO
vs. AMBIENT TEMPERATURE (VCC=5V)



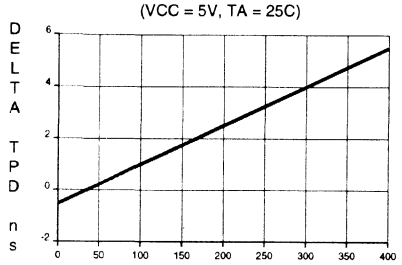
NORMALIZED t_S
vs. AMBIENT TEMPERATURE (VCC=5V)



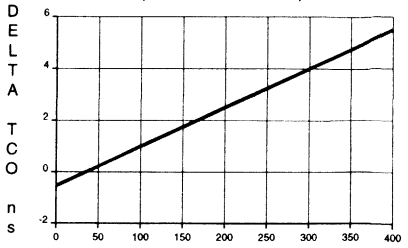
NORMALIZED t_S
vs. AMBIENT TEMPERATURE (VCC=5V)



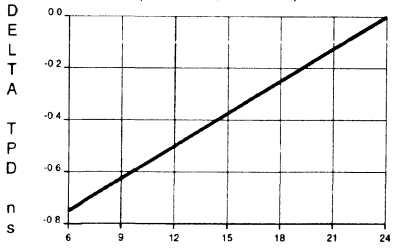
DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



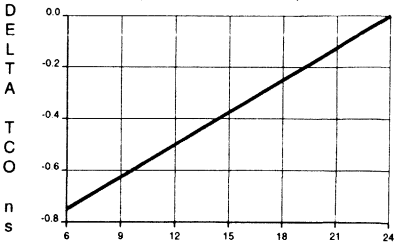
DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)



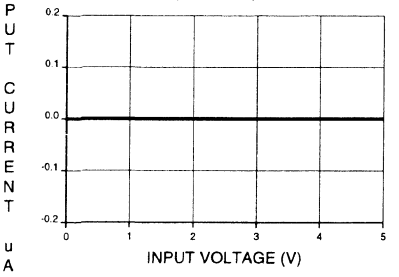
DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



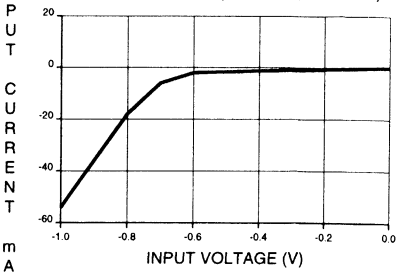
DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)



INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V)



INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
12	7.5	69	ATV2500B-12JC ATV2500B-12KC	44J 44KW	Commercial (0°C to 70°C)
15	10	52	ATV2500B-15JC ATV2500B-15KC	44J 44KW	Commercial (0°C to 70°C)
			ATV2500B-15JI ATV2500B-15KI	44J 44KW	Industrial (-40°C to 85°C)
			ATV2500B-15KM ATV2500B-15LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500B-15KM/883 ATV2500B-15LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATV2500BL-20JC ATV2500BL-20KC	44J 44KW	Commercial (0°C to 70°C)
			ATV2500BL-20JI ATV2500BL-20KI	44J 44KW	Industrial (-40°C to 85°C)
			ATV2500BL-20KM ATV2500BL-20LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BL-20KM/883 ATV2500BL-20LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATV2500BQ-20DC ATV2500BQ-20JC ATV2500BQ-20KC ATV2500BQ-20PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)
25	12	31	ATV2500BQ-25DC ATV2500BQ-25JC ATV2500BQ-25KC ATV2500BQ-25PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)
			ATV2500BQ-25DI ATV2500BQ-25JI ATV2500BQ-25KI ATV2500BQ-25PI	40DW6 44J 44KW 40P6	Industrial (-40°C to 85°C)
			ATV2500BQ-25DM ATV2500BQ-25KM ATV2500BQ-25LM	40DW6 44KW 44LW	Military/883C (-55°C to 125°C)
			ATV2500BQ-25DM/883 ATV2500BQ-25KM/883 ATV2500BQ-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	ATV2500BQL-25DC ATV2500BQL-25JC ATV2500BQL-25KC ATV2500BQL-25PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)

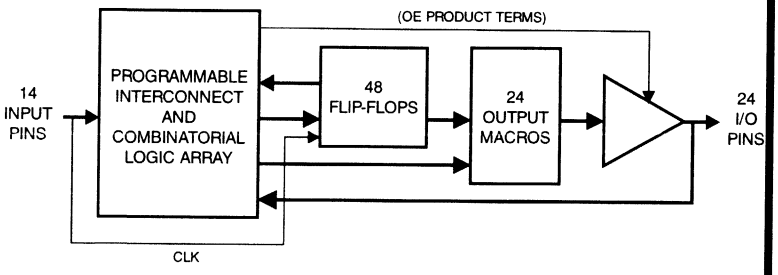
t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
25	12	31	ATV2500BQL-25DI ATV2500BQL-25JI ATV2500BQL-25KI ATV2500BQL-25PI	40DW6 44J 44KW 40P6	Industrial (-40°C to 85°C)
30	15	26	ATV2500BQL-30DM ATV2500BQL-30KM ATV2500BQL-30LM	40DW6 44KW 44LW	Military/883C (-55°C to 125°C)
30	15	26	ATV2500BQL-30DM/883 ATV2500BQL-30KM/883 ATV2500BQL-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	52	5962 - 9154504MXX 5962 - 9154504MYX	44LW 44KW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	5962 - 9154505MXX 5962 - 9154505MYX	44LW 44KW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	5962 - 9154506MXX 5962 - 9154506MYX 5962 - 9154506MQA	44LW 44KW 40DW6	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	26	5962 - 9154507MXX 5962 - 9154507MYX 5962 - 9154507MQA	44LW 44KW 40DW6	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
40DW6	40 Lead, 0.600" Wide, Ceramic, Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
40P6	40 Lead, 0.600" Wide, Plastic, Dual Inline Package OTP (PDIP)

Features

- 3-Volt Operation
- Wide V_{CC} Range
  - V_{CC} = 3.0 V to 5.25 V (Commercial)
  - V_{CC} = 3.0 V to 5.5 V (Industrial)
- High Performance, High Density Programmable Logic Device
  - Maximum 15 ns Pin-to-Pin Delay
  - Fully Connected Logic Array With 416 Product Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - Two per Macrocell
  - 72 Sum Terms
  - All Flip-Flops, I/O Pins Feed In Independently
  - Achieves Over 80% Gate Utilization
- Enhanced Macrocell Configuration Selections
  - D- or T-Type Flip-Flops
  - Product Term or Direct Input Pin Clocking
  - Registered or Combinatorial Internal Feedback
- Low Power ATLV2500BL - 7.2 mW Stand-By (Typical) at 3.6 V
- Backward Compatible With ATV2500H/L Software
- Proven and Reliable High Speed UV EPROM Process
- Reprogrammable - Tested 100% for Programmability
- 44-Lead Surface Mount Packages

Block Diagram



High Speed High Density UV Erasable Programmable Logic Device

Advance Information

Description

The ATLV2500Bs are the highest density PLDs available in a 44-pin package. With their fully connected logic array and flexible macrocell structure, high gate utilization is easily obtainable.

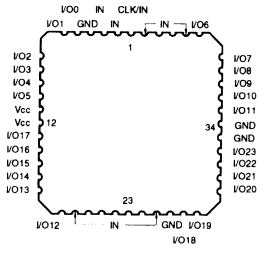
The ATLV2500Bs are organized around a *single universal input bus*. All pin and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

(continued)

Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bidirectional Buffers
GND	Ground
Vcc	+5 V Supply

SMD



0427A

Description (Continued)

In the ATLV2500Bs, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with *no performance penalty*. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power up.

The ATLV2500BL is the low voltage compatible device with speeds as fast as 20 ns. The ATLV2500BL consumes only 2 mA at standby, which provides the optimum low power PLD solution with full CMOS output levels. The ATLV2500BL significantly reduces total system power, allowing battery-powered operation.

D.C. and A.C. Operating Conditions

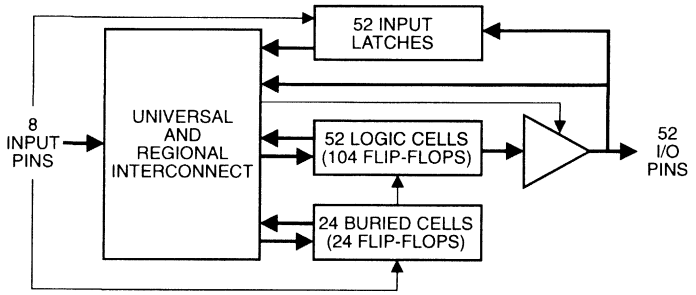
	Commercial -15, -20	**Industrial -15, -20**
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	3.0 V to 5.25 V	3.0 V to 5.5 V

High Density UV Erasable Programmable Logic Device

Features

- **Advanced Programmable Logic Device - High Gate Utilization**
- **Flexible Interconnect Architecture - Universal Routing**
- **Flexible Logic Cells - 128 Flip-Flops and 52 Latches**
- **Multiple Flip-Flop Types - Synchronous or Asynchronous Registers**
- **High Speed - 50 MHz Operation**
- **Complete Third Party Software Support**
  - **No Placement, Routing or Layout Software Required**
- **Proven and Reliable High Speed CMOS EPROM Process**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Reprogrammable - Tested 100% for Programmability**
- **Commercial, Industrial and Military Temperature Grades**

Block Diagram



Description

The Atmel V5000 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

The ATV5000 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

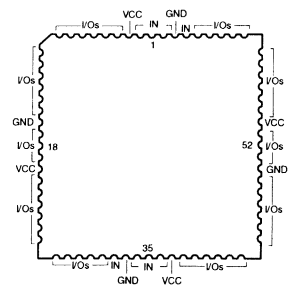
All 128 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third-party software tools and programmers support the ATV5000. This minimizes start-up investment and improves product support.

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5 V Supply

JLCC



0065B

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Functional Logic Diagram Description

There are 52 identical input/ouput logic cells and 24 identical buried logic cells in the ATV5000. Each I/O cell has two flip-flops, up to three sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least four product term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5000 has four identical quadrants (see Figure 2). The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in all four regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O logic cells contain three sum terms, two flip-flops, and an I/O buffer.

The buried logic cells each contain one flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5000

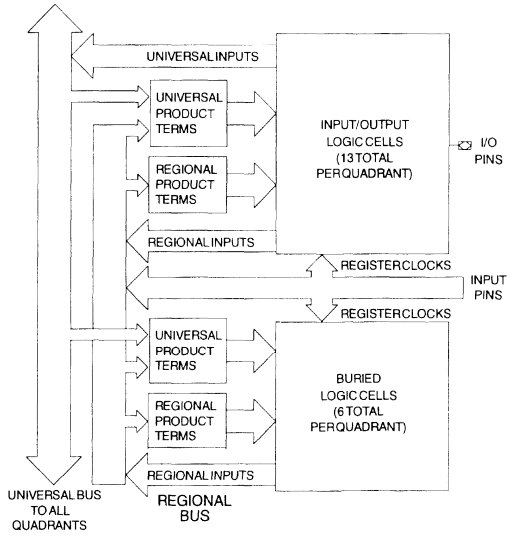


Figure 1

D.C. and A.C. Operating Range

	ATV5000-25	ATV5000/L-30	ATV5000/L-35
Operating Temperature (Case)	Commercial	Industrial	Military
	0°C - 70°C	0°C - 70°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

ATV5000 Block Diagram

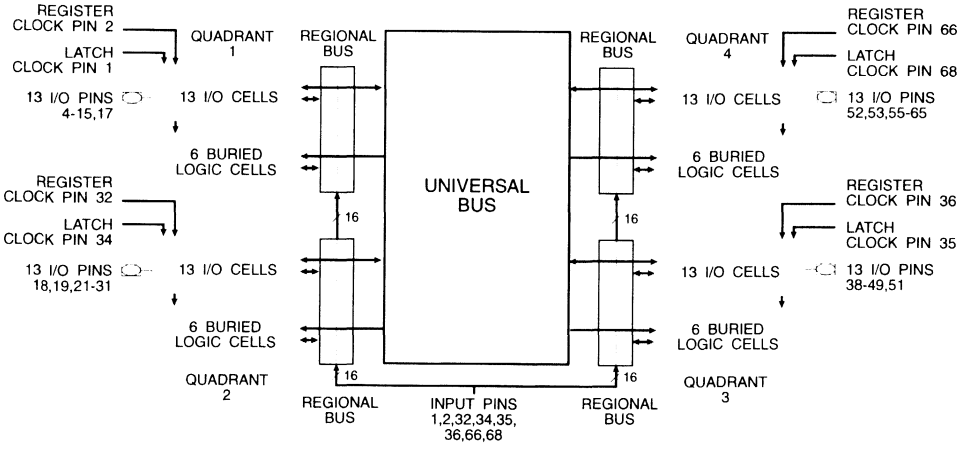


Figure 2

Quadrant Logic Diagram and Description

The ATV5000 has: four identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in every regional bus.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 3). The I/O logic cells (Figures 7, 8, 9) contain three sum terms, two flip-flops, and an I/O buffer. Sum term B has five product terms - two universal and three regional. Sum terms A and C each have four product terms - one universal and three regional. Flip-flop Q1 has global asynchronous preset, reset, and clock product terms. Flip-flop Q2 has universal asynchronous reset and clock terms and a regional asynchronous preset term. There is one universal product term for the I/O pin output enable.

The buried logic cells (Figure 4) each contain one flip-flop. The sum term has one universal product term and four regional product terms for a total of five. The flip-flop has universal asynchronous preset, reset, and clock terms. In addition, in each buried logic cell the sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip-flop inputs) and the eight dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Structure

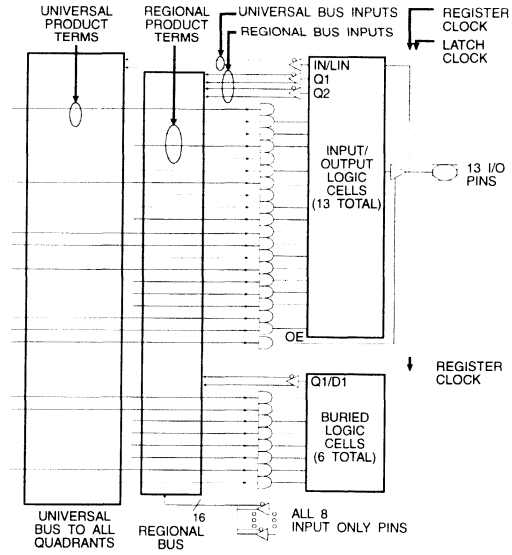


Figure 3

Logic Cell Options

The ATV5000 logic cells contain most of the chip's logic options. The standard logic cell contains two flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum term options of four, five, nine, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5000 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with five product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

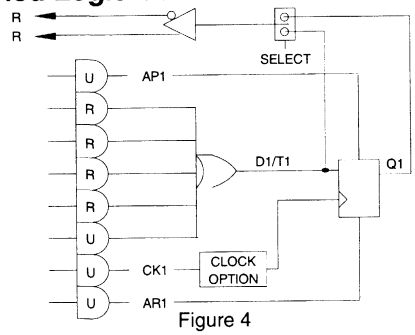


Figure 4

Clock Option

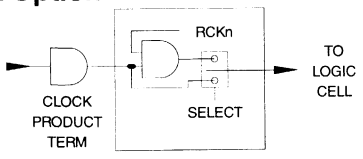


Figure 5

I/O Pin Logic

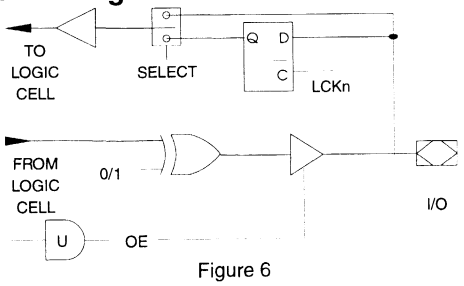


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

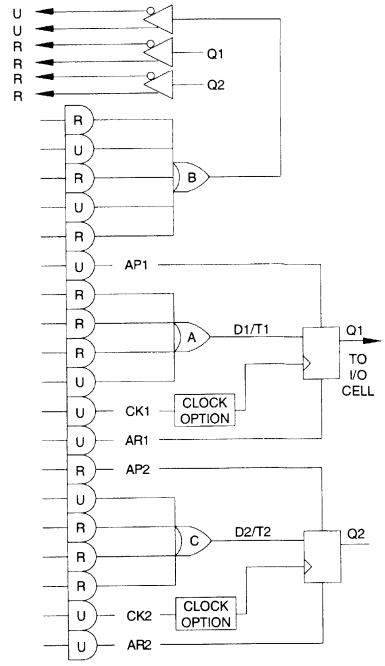


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock-to-output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5000 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5000 may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

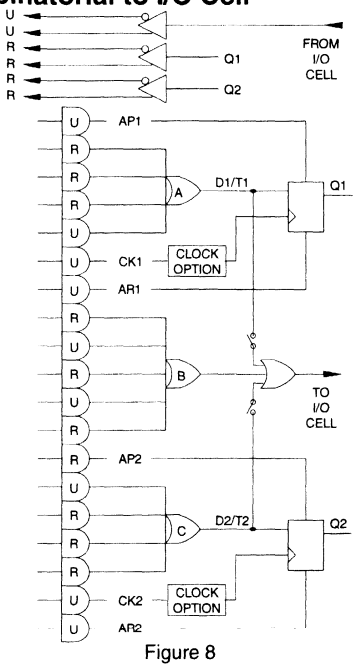


Figure 8

Logic Cell with Combinable Sum Terms, Register to I/O Cell

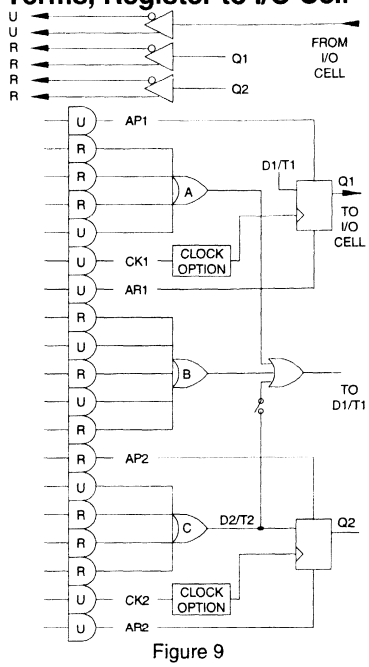


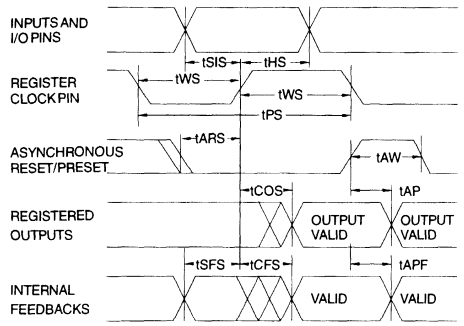
Figure 9

D.C. Characteristics

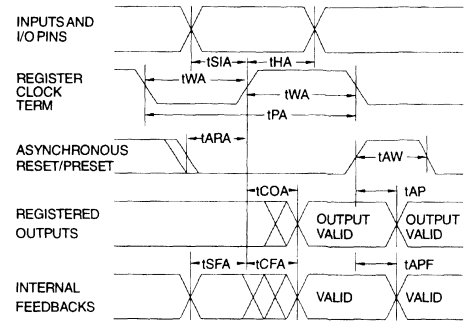
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATV5000	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5000L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		32	40	mA
			Ind.,Mil.		32	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5000L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		30 (2)		mA
			Ind.,Mil.		30 (2)		mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V				-120	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.
2. See I_{CC} vs. Frequency curve.

A.C. Waveforms [1]
Input Pin Clock



A.C. Waveforms [1]
Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

		ATV5000-25		ATV5000/L-30		ATV5000/L-35		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	**Units**
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency ($1/t_{PS}$)		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

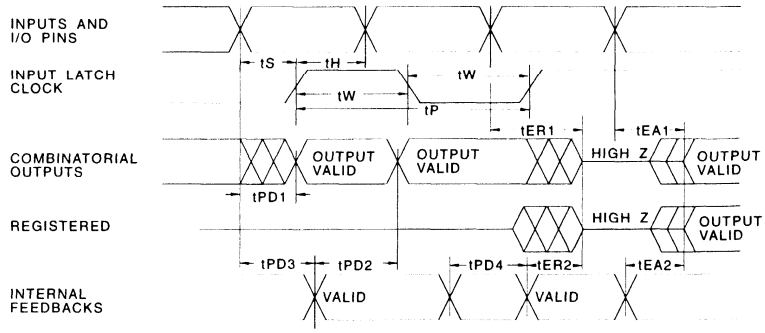
Note: 1. Add 3 ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

		ATV5000-25		ATV5000/L-30		ATV5000/L-35		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	**Units**
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency ($1/t_{PA}$)		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

Note: 1. Add 3 ns for Universal Product Terms.

A.C. Waveforms [1]



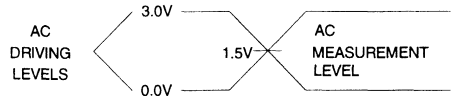
Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5000-25 Min	ATV5000-25 Max	ATV5000/L-30 Min	ATV5000/L-30 Max	ATV5000/L-35 Min	ATV5000/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency (1/t_P)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

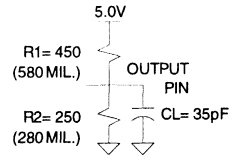
Note: 1. Add 3 ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



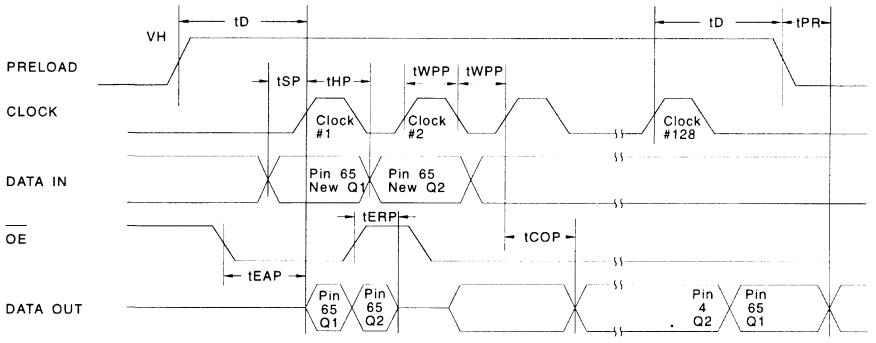
Preload and Observability of Registers

The ATV5000's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The preload/observe state is entered by placing an 11-V to 14-V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's PLD applications department.

Note: All register clock terms or pins must be low prior to entering the preload/observe state, and low prior to leaving the preload/observe state. Pin 1 must be low prior to entering the preload/observe state.



tD_{MIN} = 100 ns
tSP_{MIN} = 50 ns
tHP_{MIN} = 50 ns
$tWPP_{MIN}$ = 100 ns
tPR_{MIN} = 1000 ns
$tERP_{MAX}$ = 100 ns
$tEAP_{MAX}$ = 100 ns
$tCOP_{MAX}$ = 100 ns

Preload / Observe Register Scan Order

Quadrant	Pin															
Quadrant 1	Pin	4			5			6		•••		15			17		
	D_{IN}	Q2	Q1	B23	Q2	Q1	Q2	Q1	•••	B18	Q2	Q1	Q2	Q1		(Quadrant 2)
Quadrant 2	Pin	18			19			21		22		•••			31	
(Quadrant 1)→		Q2	Q1	Q2	Q1	B17	Q2	Q1	Q2	Q1	•••	B12	Q2	Q1		(Quadrant 3)
Quadrant 3	Pin	38			39			40		•••		49			51	
(Quadrant 2)→		Q2	Q1	B11	Q2	Q1	Q2	Q1	•••	B6	Q2	Q1	Q2	Q1		(Quadrant 4)
Quadrant 4	Pin	52			53			55		56		•••			65	
(Quadrant 3)→		Q2	Q1	Q2	Q1	B5	Q2	Q1	Q2	Q1	•••	B0	Q2	Q1		D_{OUT}

Power Up Reset

The registers in the ATV5000 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

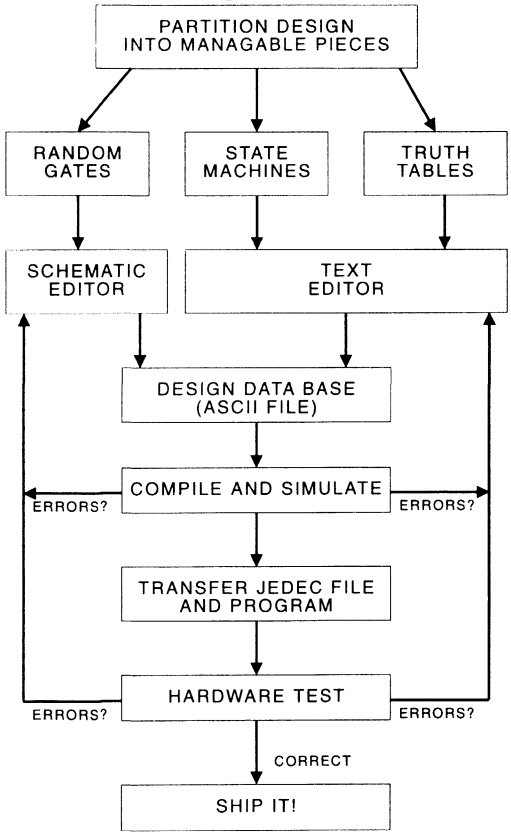
1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.

Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Design Flow Diagram



Using The ATV5000

The ATV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), MINC Inc. (PLDesigner-XL™), and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5000. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5000 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5000, and frees the designer from being required to learn all of the features of a complex device such as the ATV5000. For further information on fitters for the ATV5000, contact Atmel's PLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an PLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go— all in a matter of hours.

ABEL™, CUPL™, PLDesigner-XL™ and LOGiC™ may be trademarks of others.

ATV5000 PLCC/PGA Pin Assignments

PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5000 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

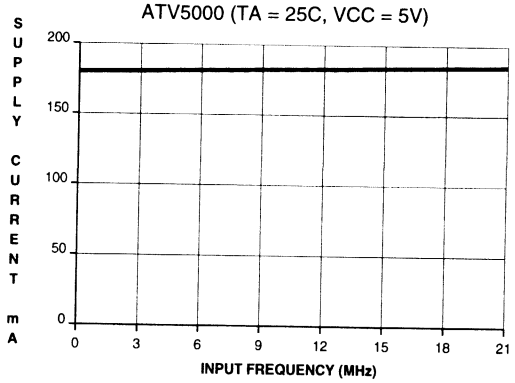
The security fuse also inhibits preload and observability.

Erasure Characteristics

The entire memory array of an ATV5000 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

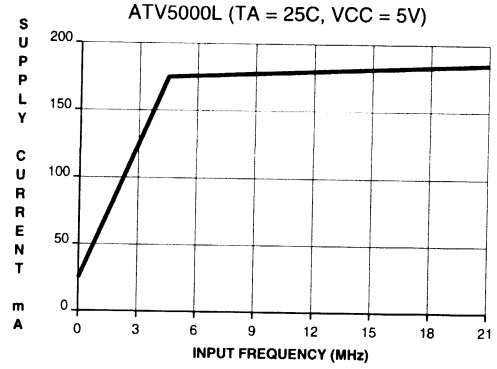
SUPPLY CURRENT vs. INPUT FREQUENCY

ATV5000 (TA = 25C, VCC = 5V)



SUPPLY CURRENT vs. INPUT FREQUENCY

ATV5000L (TA = 25C, VCC = 5V)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5000-25JC ATV5000-25KC ATV5000-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
30	20	40	ATV5000-30JC ATV5000-30KC ATV5000-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-30KI ATV5000-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-30KM ATV5000-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-30KM/883 ATV5000-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5000-35JC ATV5000-35KC ATV5000-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000-35KI ATV5000-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000-35KM ATV5000-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000-35KM/883 ATV5000-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5962-93248 02M XX ATV5962-93248 02M YX	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5000L-30JC ATV5000L-30KC ATV5000L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5000L-35JC ATV5000L-35KC ATV5000L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5000L-35KI ATV5000L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5000L-35KM ATV5000L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5000L-35KM/883 ATV5000L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5962-93248 03M XX ATV5962-93248 08M YX	68KW 68UK	Military/883C Class B, Fully Compliant (-55°C to 125°C)

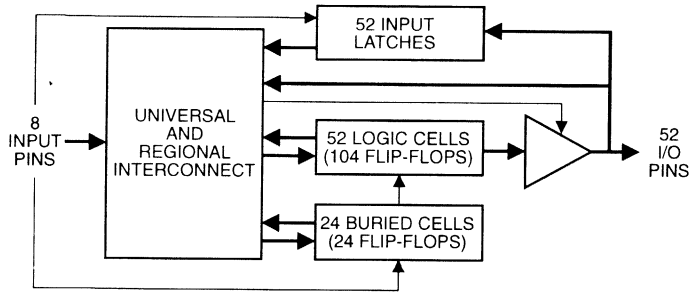
Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

High Density UV Erasable Programmable Logic Device

Features

- Advanced Programmable Logic Device - High Gate Utilization
- Pin-Compatible with Atmel's ATV5000
- Flexible Interconnect Architecture - Similar to ATV5000 with More Emphasis on Universal Routing
- Flexible Logic Cells - 128 Flip-Flops and 52 Latches
- Multiple Flip-Flop Types - Synchronous or Asynchronous Registers
- High Speed - 50 MHz Operation
- Complete Third Party Software Support
  - No Placement, Routing or Layout Software Required
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000 V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- Commercial, Industrial and Military Temperature Grades

Block Diagram



Description

The Atmel V5100 is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance. Additional universal routing simplifies design fitting.

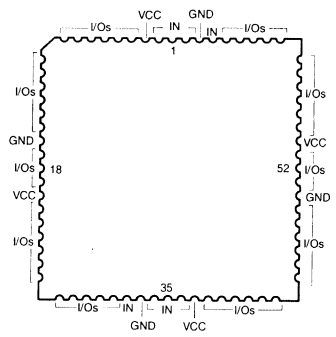
The ATV5100 has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms

(continued)

Chip Carrier Pin Configuration

Pin Name	Function
IN	Logic and Clock Inputs
Pins 2,32,36,66	Input/Register Clocks 1-4
Pins 1,34,35,68	Input/Latch Clocks 1-4
I/O	Bidirectional Buffers
VCC	+5 V Supply

JLCC



0428A

Description (Continued)

feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D- or T-types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard, off-the-shelf third-party software tools and programmers support the ATV5100. This minimizes start-up investment and improves product support.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V[1]
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V[1]
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Functional Logic Diagram Description

There are 52 identical input/ouput logic cells and 24 identical buried logic cells in the ATV5100. Each I/O cell has two flip-flops, up to three sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least four product term inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The ATV5100 has four identical quadrants (see Figure 2). The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in all four regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 1). The I/O logic cells contain three sum terms, two flip-flops, and an I/O buffer.

The buried logic cells each contain one flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

Quadrant Functional Logic Diagram ATV5100

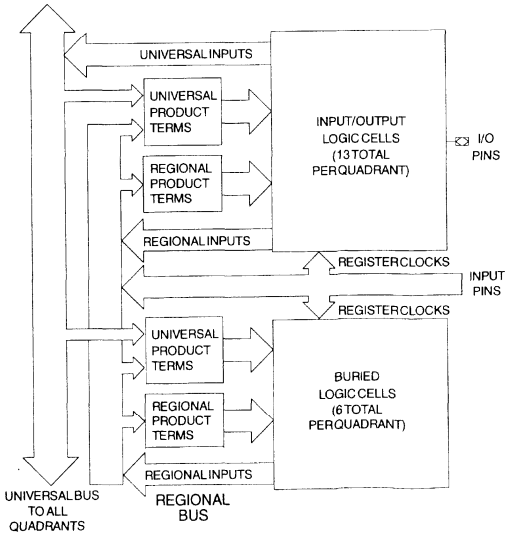


Figure 1

D.C. and A.C. Operating Range

		ATV5100-25	ATV5100/L-30	ATV5100/L-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

ATV5100 Block Diagram

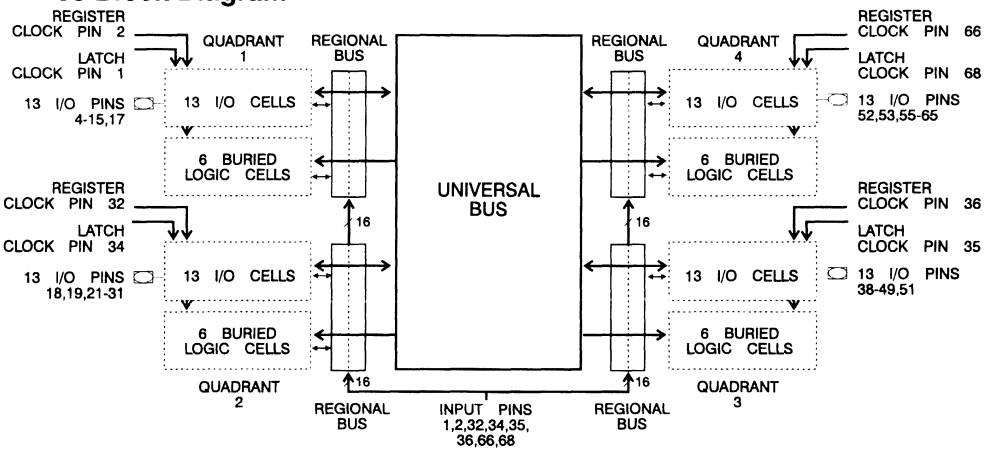


Figure 2

Quadrant Logic Diagram and Description

The ATV5100 has: four identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The eight input-only pins are available in every regional bus.

Each logic cell has a number of "regional" and "universal" product terms. The I/O logic cells contain three sum terms, two flip-flops, and an I/O buffer. Sum term B has five product terms - three universal and two regional. Sum term A has four product terms - two universal and two regional. Sum term C has four product terms - three universal and one regional (see next page). Flip-flops Q1 and Q2 have universal clock and regional preset and reset product terms. There is one regional product term for the I/O pin output enable.

The buried logic cells each contain one flip-flop. The sum term has three universal product term and two regional product terms for a total of five. The flip-flop has a universal clock product term and regional asynchronous preset and reset product terms. In addition, each buried logic cell sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip-flop inputs) and the eight dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

Quadrant Clock Pin Assignments

Quadrant Number	Register Clock Pin	Latch Clock Pin
1	2	1
2	32	34
3	36	35
4	66	68

Quadrant Logic Diagram

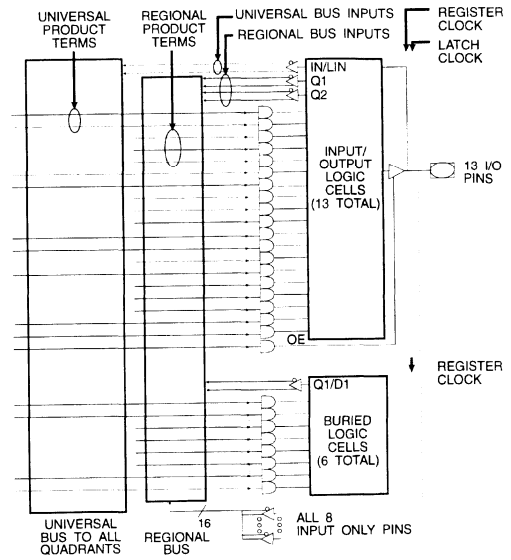


Figure 3

Logic Cell Options

The ATV5100 logic cells contain most of the chip's logic options. The standard logic cell contains two flip-flops, three sum terms and three array inputs. The three sum terms can be combined to provide sum term options of four, five, nine, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The ATV5100 retains the ATV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 8). A new feature, unique to the ATV5000 and ATV5100, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 7). This high speed logic expansion term increases the devices flexibility and gate utilization.

Buried Logic Cells

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with five product terms, a flip-flop, and individual preset, clear, and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

Buried Logic Cells

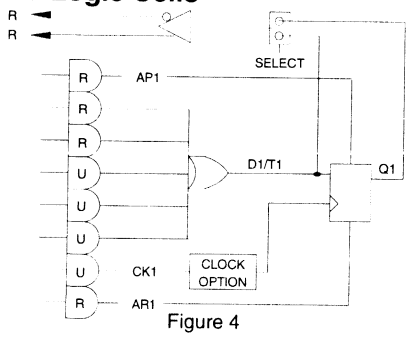


Figure 4

Clock Option

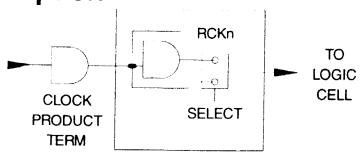


Figure 5

I/O Pin Logic

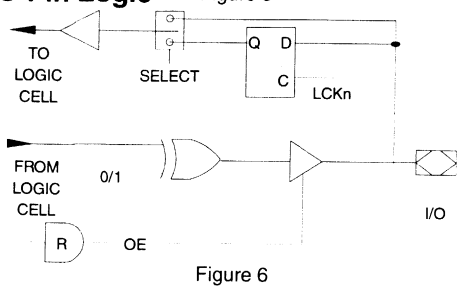


Figure 6

Logic Cell with Buried Sum Term and Register to I/O Cell

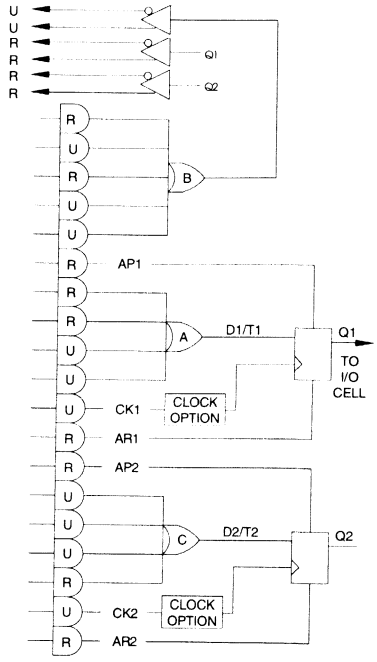


Figure 7

Flip-Flop Clock Options

Each register may be connected to its regional clock to provide fast clock-to-output timing (see Figure 5). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O Pin Latches

Each I/O pin of the ATV5100 has an input latch which can be individually enabled or disabled (see Figure 6). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is low, and data is captured on the clock's rising edge.

Flip-Flop Types

Each flip-flop in the ATV5100 may be configured as either a T- or D-type flip-flop. A T-type flip-flop can also easily be configured into a JK or SR flip-flop.

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

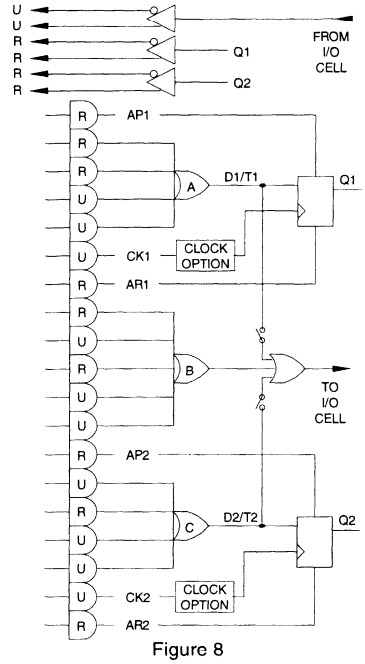


Figure 8

Logic Cell with Combinable Sum Terms, Register to I/O Cell

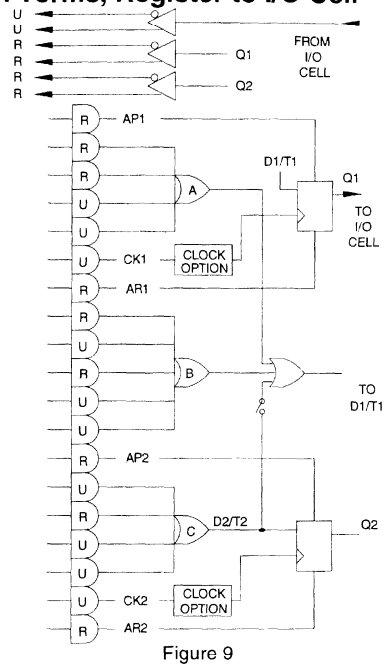


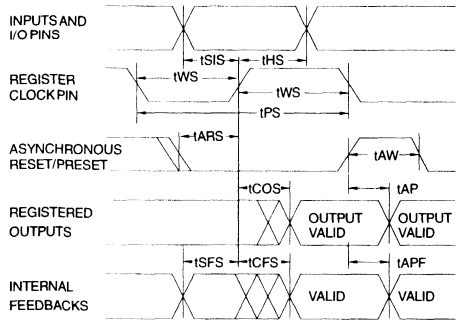
Figure 9

D.C. Characteristics

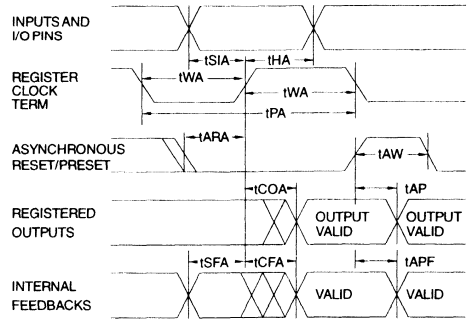
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V				10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V				10	µA
I_{CC}	Power Supply Current ATV5100	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		200	350	mA
			Ind.,Mil.		200	400	mA
I_{CC}	Power Supply Current ATV5100L	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	Com.		20	40	mA
			Ind.,Mil.		20	50	mA
I_{CC2}	Clocked Power Supply Current, ATV5100L Only	f = 1 MHz, V_{CC} = MAX Outputs Open	Com.		30 (2)		mA
			Ind.,Mil.		30 (2)		mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V				-120	mA
V_{IL}	Input Low Voltage			-0.6		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8 mA Com,Ind; 6 mA Mil.				0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3			V
		I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.
2. See I_{CC} vs. Frequency curve.

A.C. Waveforms [1] Input Pin Clock



A.C. Waveforms [1] Product Term Clock



Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

Register A.C. Characteristics, Input Pin Clock

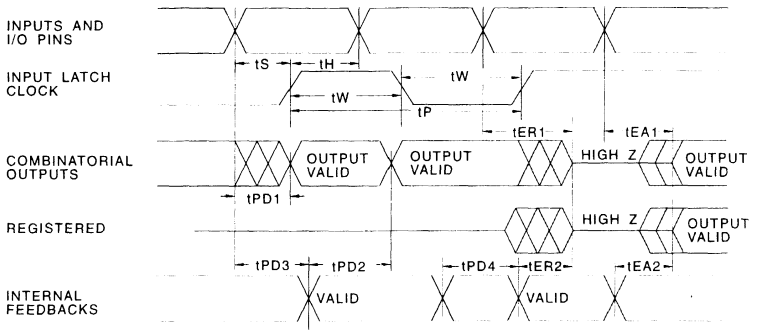
		ATV5100-25		ATV5100/L-30		ATV5100/L-35		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	**Units**
t_{COS}	Clock to Output		15		20		25	ns
t_{CFS}	Clock to Feedback	0	9	0	12	0	15	ns
t_{SIS}	Input Setup Time[1]	16		17		20		ns
t_{SFS}	Feedback Setup Time[1]	11		13		15		ns
t_{HS}	Hold Time	0		0		0		ns
t_{WS}	Clock Width	10		12		15		ns
t_{PS}	Clock Period	20		25		30		ns
F_{MAXS}	Maximum Frequency ($1/t_{PS}$)		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	20		25		30		ns

Note: 1. Add 3 ns for Universal Product Terms.

Register A.C. Characteristics, Product Term Clock

		ATV5100-25		ATV5100/L-30		ATV5100/L-35		
Symbol	**Parameter**	Min	Max	Min	Max	Min	Max	**Units**
t_{COA}	Clock to Output		25		30		35	ns
t_{CFA}	Clock to Feedback	7	20	10	25	12	27	ns
t_{SIA}	Input Setup Time[1]	10		12		15		ns
t_{SFA}	Feedback Setup Time[1]	5		8		13		ns
t_{HA}	Hold Time	8		10		12		ns
t_{WA}	Clock Width	12		15		15		ns
t_{PA}	Clock Period	25		33		40		ns
F_{MAXA}	Maximum Frequency ($1/t_{PA}$)		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	15		20		25		ns

A.C. Waveforms [1]



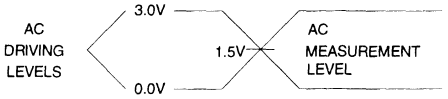
Notes: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics

Symbol	Parameter	ATV5100-25 Min	ATV5100-25 Max	ATV5100/L-30 Min	ATV5100/L-30 Max	ATV5100/L-35 Min	ATV5100/L-35 Max	Units
t_{PD1}	Input to Non-Registered Output[1]		25		30		35	ns
t_{PD2}	Feedback to Non-Registered Output[1]		20		25		30	ns
t_{PD3}	Input to Non-Registered Feedback[1]		20		25		30	ns
t_{PD4}	Feedback to Non-Registered Feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input Latch Setup Time	5		6		7		ns
t_H	Input Latch Hold Time	5		5		5		ns
t_W	Clock Width	10		12		12		ns
t_P	Clock Period	20		25		30		ns
F_{MAX}	Maximum Frequency ($1/t_P$)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset Width	15		20		20		ns
t_{AP}	Asynchronous Reset/ Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/ Preset to Registered Feedback		25		30		35	ns

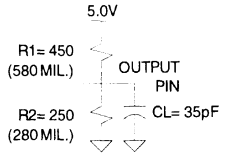
Note: 1. Add 3 ns for Universal Product Terms.

Input Test Waveforms and Measurement Levels



t_R, t_F < 5 ns (10% to 90%)

Output Test Load



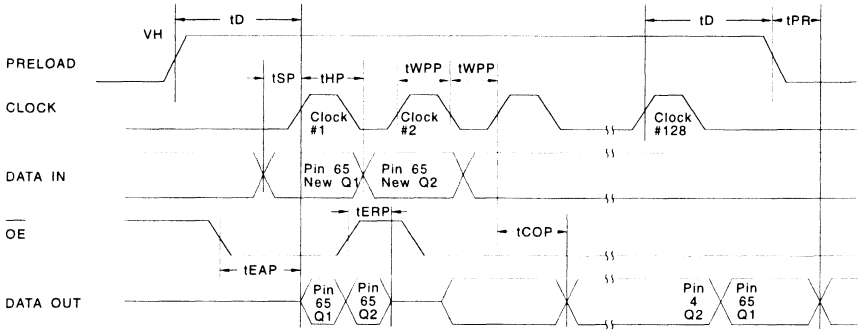
Preload and Observability of Registers

The ATV5100's registers include circuity to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The preload/observe state is entered by placing an 11-V to 14-V signal on pin 68 on the JLCC. When the clock (pin 1) is pulsed high, data (pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, OE (pin 66) can be held high and data out (pin 65) will remain high impedance.

Any user contemplating the use of register preload/obervability is encouraged to contact Atmel's PLD applications department.

Note: All register clock terms or pins must be low prior to entering the preload/observe state, and low prior to leaving the preload/observe state. Pin 1 must be low prior to entering the preload/observe state.



tD_{MIN} = 100 ns
tSP_{MIN} = 50 ns
tHP_{MIN} = 50 ns
$tWPP_{MIN}$ = 100 ns
tPR_{MIN} = 1000 ns
$tERP_{MAX}$ = 100 ns
$tEAP_{MAX}$ = 100 ns
$tCOP_{MAX}$ = 100 ns

Preload / Observe Register Scan Order

Quadrant	Pin															
Quadrant 1	Pin	4			5			6		•••		15			17		
	D_{IN}	Q2	Q1	B23	Q2	Q1	Q2	Q1	•••	B18	Q2	Q1	Q2	Q1	(Quadrant 2)	
Quadrant 2	Pin	18			19			21		22		•••			31	
(Quadrant 1)→		Q2	Q1	Q2	Q1	B17	Q2	Q1	Q2	Q1	•••	B12	Q2	Q1	(Quadrant 3)	
Quadrant 3	Pin	38			39			40		•••		49			51	
(Quadrant 2)→		Q2	Q1	B11	Q2	Q1	Q2	Q1	•••	B6	Q2	Q1	Q2	Q1	(Quadrant 4)	
Quadrant 4	Pin	52			53			55		56		•••			65	
(Quadrant 3)→		Q2	Q1	Q2	Q1	B5	Q2	Q1	Q2	Q1	•••	B0	Q2	Q1	D_{OUT}	

Power Up Reset

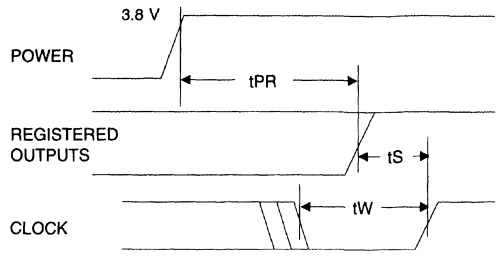
The registers in the ATV5100 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

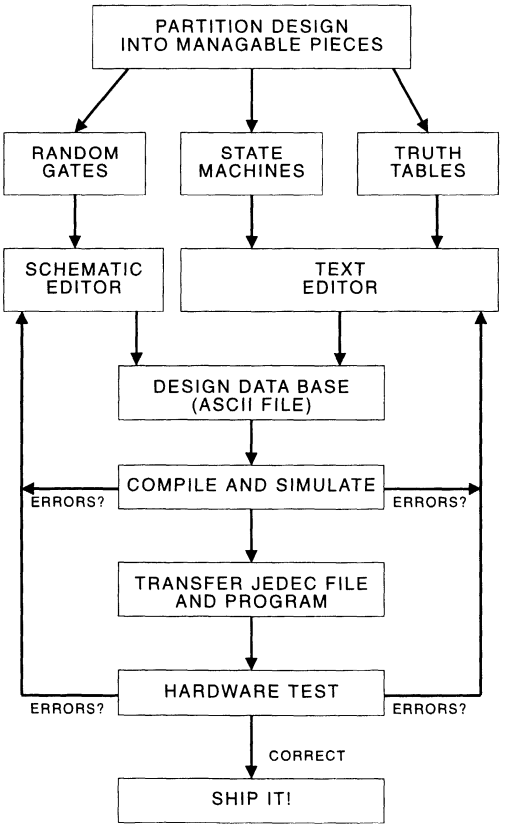
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Design Flow Diagram



Using The ATV5100

The ATV5100's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), MINC Inc. (PLDesigner-XL™) and ISDATA (LOGiC™).

The first step in designing a device as complex as the ATV5100 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the ATV5100. Random gates can be described either with boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorially and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the ATV5100 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the ATV5100, and frees the designer from being required to learn all of the features of a complex device such as the ATV5100. For further information on fitters for the ATV5100, contact Atmel's EPLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go— all in a matter of hours.

ATV5100 PLCC/PGA Pin Assignments

PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name	PLCC Pin	PGA Pin	Name
1	B6	IN	18	F2	I/O	35	K6	IN	52	F10	I/O
2	A6	IN	19	F1	I/O	36	L6	IN	53	F11	I/O
3	B5	VCC	20	G2	VCC	37	K7	VCC	54	E10	VCC
4	A5	I/O	21	G1	I/O	38	L7	I/O	55	E11	I/O
5	B4	I/O	22	H2	I/O	39	K8	I/O	56	D10	I/O
6	A4	I/O	23	H1	I/O	40	L8	I/O	57	D11	I/O
7	B3	I/O	24	J2	I/O	41	K9	I/O	58	C10	I/O
8	A3	I/O	25	J1	I/O	42	L9	I/O	59	C11	I/O
9	A2	I/O	26	K1	I/O	43	L10	I/O	60	B11	I/O
10	B2	I/O	27	K2	I/O	44	K10	I/O	61	B10	I/O
11	B1	I/O	28	L2	I/O	45	K11	I/O	62	A10	I/O
12	C2	I/O	29	K3	I/O	46	J10	I/O	63	B9	I/O
13	C1	I/O	30	L3	I/O	47	J11	I/O	64	A9	I/O
14	D2	I/O	31	K4	I/O	48	H10	I/O	65	B8	I/O
15	D1	I/O	32	L4	IN	49	H11	I/O	66	A8	IN
16	E2	GND	33	K5	GND	50	G10	GND	67	B7	GND
17	E1	I/O	34	L5	IN	51	G11	I/O	68	A7	IN

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	6	8	pF	V_{IN} = 0 V
C_{OUT}	8	12	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV5100 fuse patterns. Once programmed, all outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

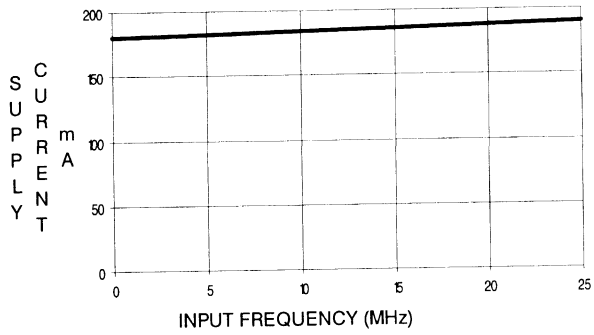
The security fuse also inhibits preload and observability.

Erasure Characteristics

The entire memory array of an ATV5100 is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 µW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

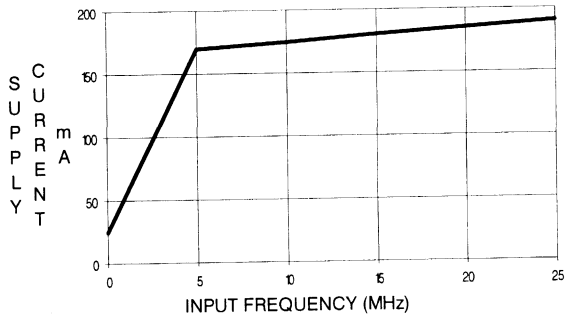
SUPPLY CURRENT vs. INPUT FREQUENCY

ATV5100 (TA=25°C, VCC=5V)



SUPPLY CURRENT vs. INPUT FREQUENCY

ATV5100L (TA=25°C, VCC=5V)



Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	15	50	ATV5100-25JC ATV5100-25KC ATV5100-25UC	68J 68KW 68UW	Commercial (0°C to 70°C)
30	20	40	ATV5100-30JC ATV5100-30KC ATV5100-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100-30KI ATV5100-30UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100-30KM ATV5100-30UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100-30KM/883 ATV5100-30UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
35	25	33	ATV5100-35JC ATV5100-35KC ATV5100-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100-35KI ATV5100-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100-35KM ATV5100-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100-35KM/883 ATV5100-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	20	40	ATV5100L-30JC ATV5100L-30KC ATV5100L-30UC	68J 68KW 68UW	Commercial (0°C to 70°C)
35	25	33	ATV5100L-35JC ATV5100L-35KC ATV5100L-35UC	68J 68KW 68UW	Commercial (0°C to 70°C)
			ATV5100L-35KI ATV5100L-35UI	68KW 68UW	Industrial (-40°C to 85°C)
			ATV5100L-35KM ATV5100L-35UM	68KW 68UW	Military (-55°C to 125°C)
			ATV5100L-35KM/883 ATV5100L-35UM/883	68KW 68UW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
68J	68 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
68KW	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
68UW	68 Pin, Windowed, Ceramic Pin Grid Array (PGA)

Contents

2

Field Programmable Gate Arrays

Features

- **High Performance**
  - **System Speeds > 100 MHz**
  - **Flip-Flop Toggle Rates > 250 MHz**
  - **1.2 ns Input Delay**
  - **3.5 ns Output Delay**
- **Thousands of Registers**
- **Cache Logic™ Design**
  - **Complete/Partial In-System Reconfiguration**
  - **No Loss of Data or Machine State**
  - **Adaptive Hardware**
- **Automatic Component Generators**
  - **Reusable Custom Hard Macro Functions**
- **Very Low Power Consumption**
  - **Standby Current of 500 µA**
  - **Typical Operating Current of 50 to 170 mA**
- **Programmable Clock Options**
  - **Independently Controlled Column Clocks**
  - **Independently Controlled Column Resets**
  - **Clock Skew Less Than 1 ns Across Chip**
- **Independently Configurable I/O (PCI Compatible)**
  - **TTL/CMOS Input Thresholds**
  - **Open Collector/Tri-state Outputs**
  - **Programmable Slew-Rate Control**
  - **I/O Drive of 16 mA (Combinable to 64 mA)**

Description

AT6000 Series SRAM-Based Field Programmable Gate Arrays (FPGAs) provide the density and performance of custom gate arrays without the prototyping and debugging delays associated with mask-programmed devices.

Supporting system speeds greater than 100 MHz and using a typical operating current of 50 to 170 mA, AT6000 Series devices are ideal for high-speed, compute-intensive designs. These FPGAs are designed to implement Cache Logic™, the ability to implement adaptive hardware and perform hardware acceleration.

The patented AT6000 Series architecture employs a symmetrical grid of small, yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 2,000 to 20,000 usable gates, and 1024 to 6400 registers. Pin locations are consistent throughout the AT6000 Series for easy design migration. High-I/O versions are available for the lower gate count devices.

AT6000 Series Field Programmable Gate Arrays

Device	AT6002	AT6003	AT6005	AT6010
Usable Gates	2,000-4,000	3,000-6,000	5,000-10,000	10,000-20,000
Cells	1,024	1,600	3,136	6,400
Registers (maximum)	1,024	1,600	3,136	6,400
I/O (maximum)	96	120	108	204
Typ. Operating Current (mA)	30	45	80	170
Cell Rows x Columns	32 x 32	40 x 40	56 x 56	80 x 80

0264B

Description (Continued)

AT6000 Series FPGAs utilize a reliable 0.8-µm single-poly, double-metal CMOS process and are 100% factory-tested.

Atmel's PC- and workstation-based Integrated Development System is used to create AT6000 Series designs. Multiple design entry methods are supported, including those from Viewlogic, Mentor, Exemplar, Cadence and Synopsys.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells (Figure 1). The array is continuous and completely uninterrupted from one edge to the other, except for bus *repeaters* spaced every eight cells (Figure 2).

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces. Buses support fast, efficient communication over medium and long distances.

The Busing Network

There are two kinds of buses: local and express (see Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses— North-South 1 and 2 (NS1 and NS2)— for every column of cells, and two local buses— East-West 1 and 2 (EW1 and EW2)— for every row of cells. In a sector each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

Figure 1. Symmetrical Array Surrounded by I/O

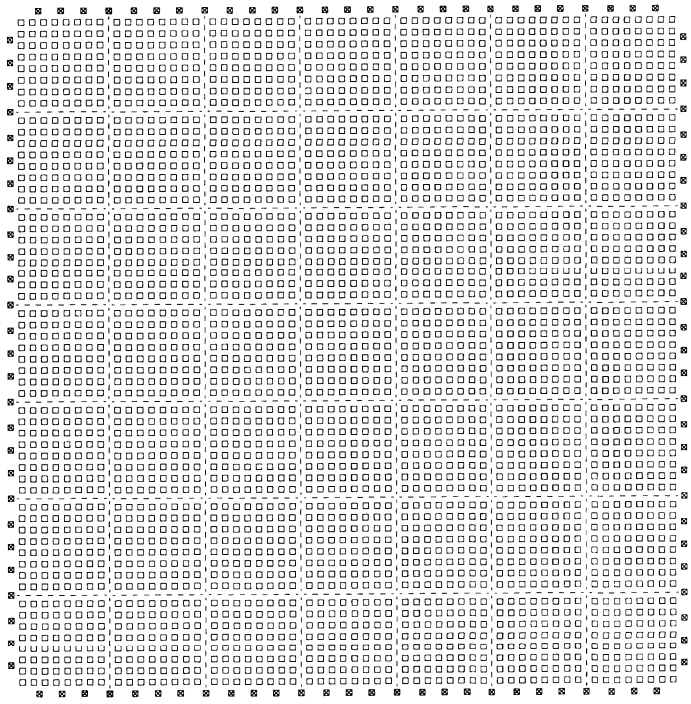


Figure 2. Busing Network

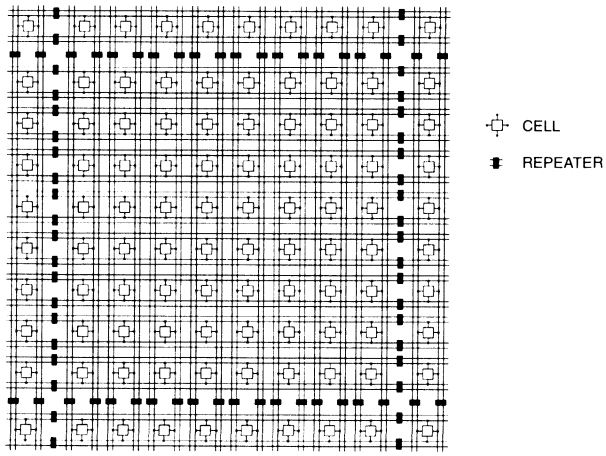
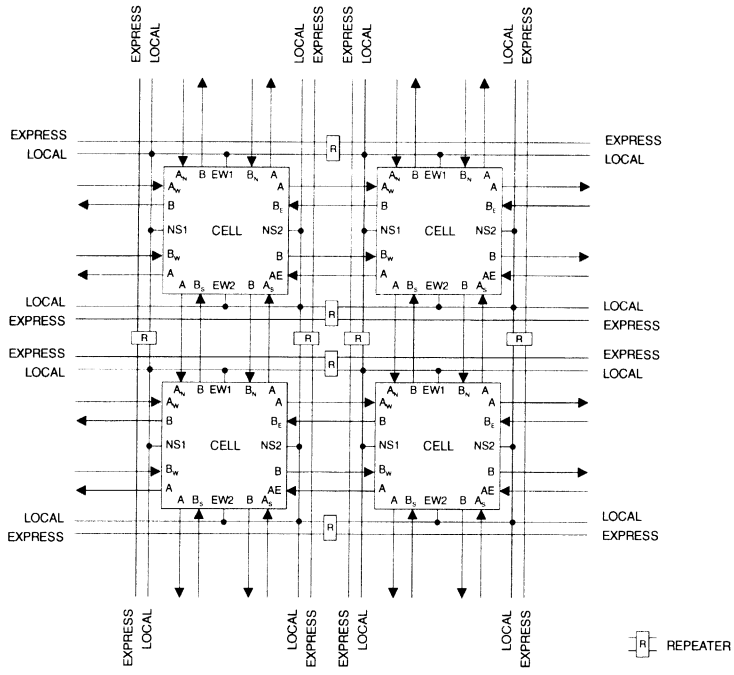


Figure 3. Cell-to-Cell and Bus-to-Bus Connections



Each cell, in addition, provides the ability to route a signal on a 90° turn between the NS1 bus and EW1 bus and between the NS2 bus and EW2 bus.

Express buses are not connected directly to cells, and thus provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus, both local and express, into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater can be programmed to provide any one of twenty-one connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

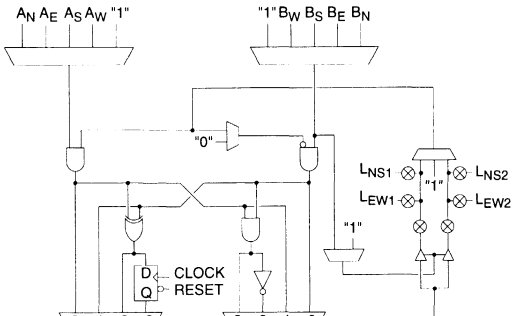
- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

In all of these cases, each connection provides signal regeneration and is thus uni-directional. For bi-directional connections, the basic repeater function for the NS2 and EW2 repeaters is augmented with a special programmable connection allowing bi-directional communication between local-bus segments. This option is primarily used to implement long, tri-state buses.

The Cell Structure

The Atmel cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Its four sides are functionally identical, so each cell is completely symmetrical.

Figure 4. Cell Structure



Read/write access to the four local buses— NS1, EW1, NS2 and EW2— is controlled, in part, by four bi-directional pass gates connected directly to the buses. To read a local bus, the pass gate for that bus is turned on and the three-input multiplexer is set accordingly. To write to a local bus, the pass gate for that bus and the pass gate for the associated tri-state driver are both turned on. The two-input multiplexer supplying the control signal to the drivers permits either: (1) active drive, or (2) dynamic tri-stating controlled by the B input. Turning between L_{NS1} and L_{EW1} or between L_{NS2} and L_{EW2} is accomplished by turning on the two associated pass gates. The operations of reading, writing and turning are subject to the restriction that each bus can be involved in no more than a single operation.

In addition to the four local-bus connections, a cell receives two inputs and provides two outputs to each of its North (N), South (S), East (E) and West (W) neighbors. These inputs and outputs are divided into two classes: "A" and "B." There is an A input and a B input from each neighboring cell and an A output and a B output driving all four neighbors. Between cells, an A output is always connected to an A input and a B output to a B input.

Within the cell, the four A inputs and the four B inputs enter two separate, independently configurable multiplexers. Cell flexibility is enhanced by allowing each multiplexer to select also the logical constant "1." The two multiplexer outputs enter the two upstream AND gates.

Downstream from these two AND gates are an Exclusive-OR (XOR) gate, a register, a downstream AND gate, an inverter and two four-input multiplexers producing the A and B outputs. These multiplexers are controlled in tandem (unlike the A and B input multiplexers) and determine the function of the cell.

- In State 0— corresponding to the "0" inputs of the multiplexers— the output of the left-hand upstream AND gate is connected to the cell's A output, and the output of the right-hand upstream AND gate is connected to the cell's B output.
- In State 1— corresponding to the "1" inputs of the multiplexers— the output of the left-hand upstream AND gate is connected to the cell's B output, the output of the right-hand upstream AND gate is connected to the cell's A output.
- In State 2— corresponding to the "2" inputs of the multiplexers— the XOR of the outputs from the two upstream AND gates is provided to the cell's A output, while the NAND of these two outputs is provided to the cell's B output.
- In State 3— corresponding to the "3" inputs of the multiplexers— the XOR function of State 2 is provided to the D input of a D-type flip-flop, the Q output of which is connected to the cell's A output. Clock and asynchronous reset signals are supplied externally as described later. The AND of the outputs from the two upstream AND gates is provided to the cell's B output.

Logic States

The Atmel cell implements a rich and powerful set of logic functions, stemming from 44 cell states. Some states use both A and B inputs. Other states are created by selecting the "1" input on either or both of the input multiplexers.

There are 20 purely combinatorial states with a range of functions, including NOR, AND, NAND, OR and two-input multi-

Figure 5a. Combinatorial States

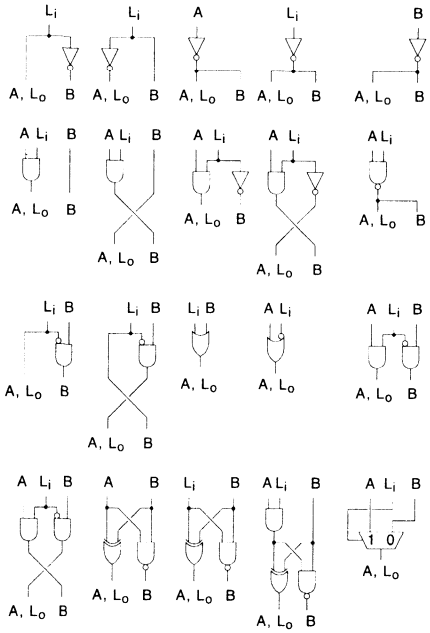


Figure 5b. Register States

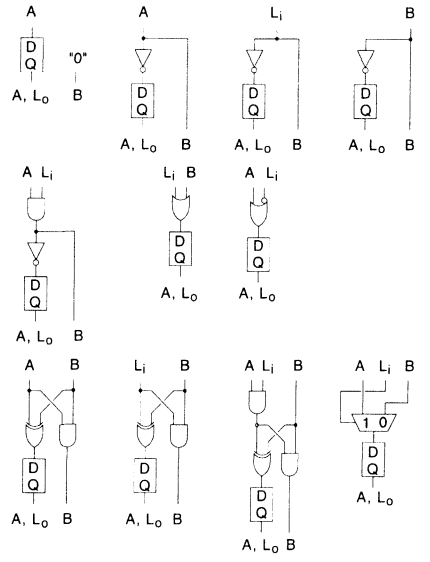


Figure 5c. Constant States

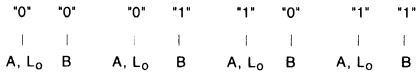


Figure 6a. Two-Input AND Feeding XOR

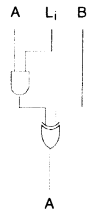
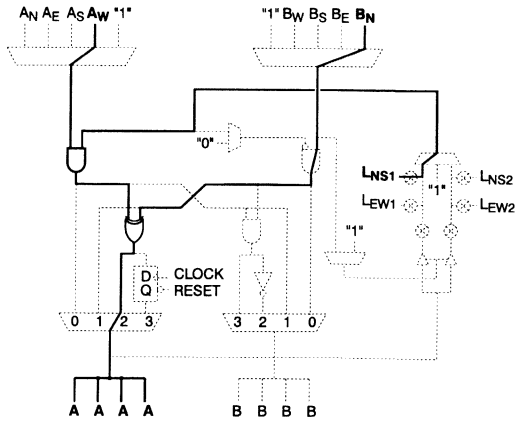


Figure 6b. Cell Configuration (A•L) XOR B



plexer (Figure 5a). There are 11 register states ranging from a simple register to a register preceded by a two-input multiplexer (Figure 5b). Five constant states produce all combinations of constant values at the two cell outputs (Figure 5c). There are five tri-state states. More complex functions are created by using cells in combination.

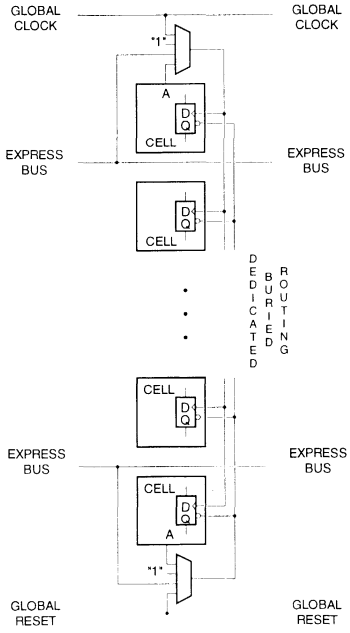
A two-input AND feeding an XOR (Figure 6a) is produced using a single cell (Figure 6b). A two-to-one multiplexer selects the logical constant "0" and feeds it to the right-hand AND gate. The AND gate acts as a feed-through, letting the B input pass through to the XOR. The three-to-one multiplexer on the right side selects the local-bus input, L_{NS1}, and passes it to the left-hand AND gate. The A and L_{NS1} signals are the inputs to the AND gate. The output of the AND gate feeds into the XOR, producing the logic state (A•L) XOR B.

Clock Distribution

Along the top edge of the array is logic for distributing clock signals to the D flip-flop in each logic cell (Figure 7). The distribution network is organized by column and permits columns of cells to be independently clocked. At the head of each column is a user-configurable multiplexer providing the clock signal for that column. It has four inputs:

- Global clock supplied through the CLOCK pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the head of the column
- Logical constant "1" to conserve power (no clock)

Figure 7. Column Clock and Column Reset



Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all the columns of the array. The global clock pin is also connected directly to the array via the A input of the upper left and right corner cells (AW on the left, and AN on the right). The express bus is useful in distributing a secondary clock to multiple columns when the global clock line is used as a primary clock. The A output of a cell is useful in providing a clock signal to a single column. The constant "1" is used to reduce power dissipation in columns using no registers.

Asynchronous Reset

Along the bottom edge of the array is logic for asynchronously resetting the D flip-flops in the logic cells (Figure 7). Like the clock network, the asynchronous reset network is organized by column and permits columns to be independently reset. At the bottom of each column is a user-configurable multiplexer providing the reset signal for that column. It has four inputs:

- Global asynchronous reset supplied through the $\overline{\text{RESET}}$ pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the foot of the column
- Logical constant "1"to conserve power

The asynchronous reset logic uses these four inputs in the same way that the clock distribution logic does. Through the global asynchronous reset, any or all columns can be reset by an externally supplied signal. The global asynchronous reset pin is also connected directly to the array via the A input of the lower left and right corner cells (AS on the left, and AE on the right). The express bus can be used to distribute a secondary reset to multiple columns when the global reset line is used as a primary reset, the A output of a cell can also provide an asynchronous reset signal to a single column, and the constant "1" is used by columns with registers requiring no reset. All registers are reset during power-up.

Input/Output

The Atmel architecture provides a flexible interface between the logic array, the configuration control logic and the I/O pins.

Two adjacent cells— an "exit" and an "entrance" cell— on the perimeter of the logic array are associated with each I/O pin.

There are two types of I/Os: A-type (Figure 8a) and B-type (Figure 8b). For A-type I/Os, the edge-facing A output of an exit cell is connected to an output driver, and the edge-facing A input of the adjacent entrance cell is connected to an input buffer. The output of the output driver and the input of the input buffer are connected to a common pin.

B-type I/Os are the same as A-type I/Os, but use the B inputs and outputs of their respective entrance and exit cells. A- and B-type I/Os alternate around the array.

Control of the I/O logic is provided by user-configurable memory bits.

TTL/CMOS Inputs

A user-configurable bit determining the threshold level— TTL or CMOS— of the input buffer.

Open Collector/Tri-state Outputs

A user-configurable bit which enables or disables the active pull-up of the output device.

Slew Rate Control

A user-configurable bit which controls the slew rate— fast or slow— of the output buffer. A slow slew rate, which reduces noise and ground bounce, is recommended for outputs that are not speed-critical. Fast and slow slew rates have the same DC-current sinking capabilities, but the rate at which each allows the output devices to reach full drive differs.

Pull-up

A user-configurable bit controlling the pull-up transistor in the I/O pin. It's primary function is to provide a logical "1" to unused input pins. When on, it is roughly equivalent to a 25K resistor to V_{CC}.

Enable Select

User-configurable bits determining the output-enable for the output driver. The output driver can be static, always on, always off, or dynamically controlled by a signal generated in the array. Four options are available from the array: (1) the control is low and always driving; (2) the control is high and never driving; (3) the control is connected to a vertical local bus associated with the output cell; and (4) the control is connected to a horizontal local bus associated with the output cell. The power-up default is never driving.

In addition to the functionality provided by the I/O logic, the entrance and exit cells provide the ability to register both inputs and outputs. Also, these perimeter cells (unlike interior cells) are connected directly to express buses: the edge-facing A and B outputs of the entrance cell are connected to express buses, as are the edge-facing A and B inputs of the exit cell. These buses are perpendicular to the edge, and provide a rapid means of bringing I/O signals to and from the array interior and the opposite edge of the chip.

Chip Configuration

The Integrated Development System generates the SRAM bit pattern required to configure a AT6000 Series device. A PC parallel port, microprocessor, EPROM or serial configuration memory can be used to download configuration patterns.

Users select from several configuration modes. Many factors, including board area, configuration speed and the number of designs implemented in parallel can influence the user's final choice.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is in operation. The number of dual-function pins required for each mode varies.

The devices can be partially reconfigured while in operation. Portions of the device not being modified remain operational during configuration. Simultaneous configuration of more than one device is also possible. Full configuration takes as little as a millisecond, partial configuration is even faster.

Refer to the Pin Function Description section following for a brief summary of the pins used in configuration. For more information about configuration, refer to the AT6000 Series Configuration data sheet.

Figure 8a. A-Type I/O Logic

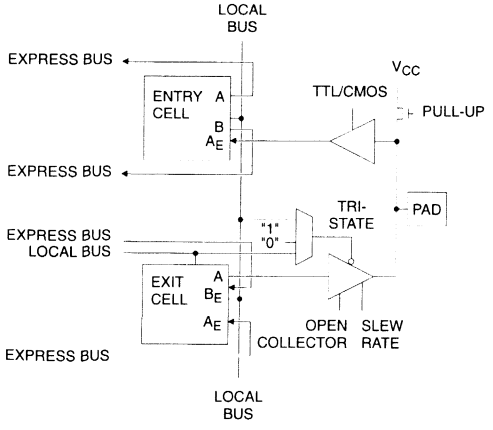
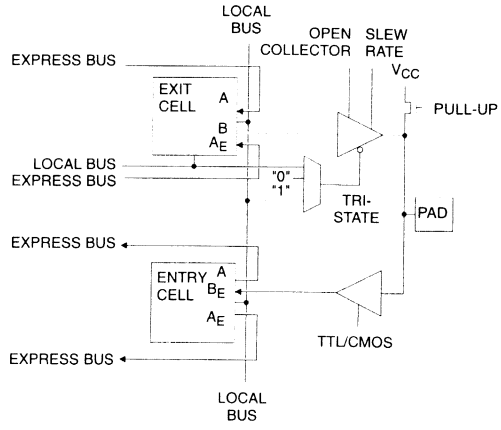


Figure 8b. B-Type I/O Logic



Pin Function Description

This section provides abbreviated descriptions of the various AT6000 Series pins. For more complete descriptions, refer to the AT6000 Series Configuration data sheet.

Pinout tables for the AT6000 series of devices follow.

Power Pins

V_{CC}, V_{DD}, GND, V_{SS}

V_{CC} and GND are the I/O supply pins, V_{DD} and V_{SS} are the internal logic supply pins. V_{CC} and V_{DD} should be tied to the same trace on the printed circuit board. GND and V_{SS} should be tied to the same trace on the printed circuit board.

Input/Output Pins

All I/O pins can be used in the same way (refer to the I/O section of the architecture description). Some I/O pins are dual-function pins used during configuration of the array. When not being used for configuration, dual-function I/Os are fully functional as normal I/O pins. On initial power-up, all I/Os are configured as TTL inputs with a pull-up.

Dedicated Timing and Control Pins

$\overline{CON}$

Configuration-in-process pin. After power-up, $\overline{CON}$ remains low until power-up initialization is complete. $\overline{CON}$ is an open collector signal. After power-up initialization, forcing $\overline{CON}$ low begins the configuration process.

$\overline{CS}$

Configuration enable pin. All configuration pins are ignored if $\overline{CS}$ is high. $\overline{CS}$ must be held low throughout the configuration process. $\overline{CS}$ is a TTL-type input pin.

M0, M1, M2

Configuration mode pins used to determine the configuration mode. All three are TTL-type input pins.

CCLK

Configuration clock pin. CCLK is an input or an output depending on the configuration mode selected. It is an output in two modes. The output modes support configuration using the fewest external components. In either of these modes, the configuration time will vary from part to part depending on clock speed. CCLK is a TTL-type input in modes that use it as an input and a CMOS-type output in those modes that use it as an output. When not in use, CCLK is set low.

CLOCK

External logic source used to drive the internal global clock line. Registers toggle on the rising edge of CLOCK. The CLOCK signal is neither used nor affected by the configuration modes. It is always a TTL input.

$\overline{RESET}$

Array register asynchronous reset. $\overline{RESET}$ drives the internal global reset. The $\overline{RESET}$ signal is neither used nor affected by the configuration modes. It is always a TTL input.

Dual-Function Pins

When $\overline{CON}$ is high, dual-function I/O pins act as device I/Os; when $\overline{CON}$ is low, dual-function pins are used as configuration control or data signals as determined by the configuration modes. Care must be taken when using these pins to ensure that configuration activity does not interfere with other circuitry associated with the pin's net.

D0 or I/O

Serial configuration modes use D0 as the serial data input pin. Parallel configuration modes use D0 as the least-significant bit. Input data must meet setup and hold requirements with respect to the rising edge of CCLK.

D1 to D7 or I/O

Parallel configuration modes use these pins as inputs. Serial configuration modes do not use them. Data must meet setup and hold requirements with respect to the rising edge of CCLK.

$\overline{CEN}$ or I/O

During address count-up/down configuration, $\overline{CEN}$ is an output. $\overline{CEN}$ can be used as the output enable of a parallel EPROM. In this case, it should be configured as a constant high, and not used as a configurable I/O pin.

A0 to A16 or I/O

During address count-up/down configuration, these pins are outputs and act as the address pins for a parallel EPROM. A0A16 eliminate the need for an external address counter if the user wishes to use an inexpensive parallel EPROM to program a device. Addresses change after the rising edge of the CCLK signal.

$\overline{CSOUT}$ or I/O

When cascading devices, $\overline{CSOUT}$ is an output used to enable other devices. $\overline{CSOUT}$ should be connected to the CS input of the downstream device. The $\overline{CSOUT}$ function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, $\overline{CSOUT}$ should be dedicated to configuration and not used as a configurable I/O.

$\overline{\text{CHECK}}$ or I/O

During configuration, $\overline{\text{CHECK}}$ is an input that can be used to enable the data check function at the beginning of a configuration cycle. No data is written to the device while $\overline{\text{CHECK}}$ is low. Instead, the configuration file being applied to D0-D7 is compared with the current contents of the internal configuration RAM. If a mismatch is detected between the data being loaded and the data already in the RAM, the $\overline{\text{ERR}}$ pin goes low. The $\overline{\text{CHECK}}$ function is optional and can be disabled during initial programming.

$\overline{\text{ERR}}$ or I/O

During configuration, $\overline{\text{ERR}}$ is an output. When the $\overline{\text{CHECK}}$ function is activated and a mismatch is detected between the current configuration data stream and the data already loaded in the configuration RAM, $\overline{\text{ERR}}$ goes low. The $\overline{\text{ERR}}$ output is a registered signal. Once a mismatch is found, the signal is set and is only reset after the configuration cycle is complete. $\overline{\text{ERR}}$ is also asserted for configuration file errors. The $\overline{\text{ERR}}$ function is optional and can be disabled during initial programming.

Device Pinout Selection

	AT6002	AT6003	AT6005	AT6010
84 PLCC	64 I/O	64 I/O	64 I/O	—
100 VQFP	80 I/O	80 I/O	80 I/O	—
132 PQFP	96 I/O	108 I/O	108 I/O	108 I/O
144 TQFP	96 I/O	120 I/O	108 I/O	120 I/O
180 CPGA	—	—	108 I/O	156 I/O
208 PQFP	—	—	—	172 I/O
240 PQFP	—	—	—	204 I/O

Bit-Stream Sizes (bytes of data)

Mode(s)	Type [1, 2]	Beginning Sequence	AT6002	AT6003	AT6005	AT6010
1	P	Preamble	2677	4153	8077	16393
2	P	Preamble	2677	4153	8077	16393
3	S	Null Byte/Preamble	2678	4154	8078	16394
4	S	Null Byte/Preamble	2678	4154	8078	16394
5	P	Preamble	2677	4153	8077	16393
6	P	Preamble/Preamble	2678	4154	8078	16394

Notes: 1. P = Parallel.
2. S = Serial.

Pinout Assignment

Left Side (Top to Bottom)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
—	—	—	I/O51(A)	—	—	—	—	B1	1	1
I/O24 or A7	I/O30 or A7	I/O27 or A7	I/O50(A) or A7	12	1	18	1	C1	2	2
—	I/O29	—	I/O49(A)	—	—	—	2	D1	3	3
—	—	—	I/O48(B)	—	—	—	—	—	—	4
—	—	—	VCC	—	—	—	—	PWR[1]	4	5
—	—	—	I/O47(A)	—	—	—	—	E1	5	6
—	—	—	GND	—	—	—	—	GND[2]	6	7
—	I/O28	I/O26	I/O46(A)	—	—	19	3	G1	7	8
I/O23 or A6	I/O27 or A6	I/O25 or A6	I/O45(A) or A6	13	2	20	4	H1	8	9
—	—	—	I/O44(B)	—	—	—	—	—	—	10
—	—	—	I/O43(A)	—	—	—	—	C2	9	11
I/O22	I/O26	I/O24	I/O42(A)	—	—	21	5	D2	10	12
I/O21 or A5	I/O25 or A5	I/O23 or A5	I/O41(A) or A5	14	3	22	6	E2	11	13
—	—	—	I/O40(B)	—	—	—	—	—	—	14
—	—	—	I/O39(A)	—	—	—	—	F2	12	15
I/O20	I/O24	I/O22	I/O38(A)	—	4	23	7	G2	13	16
I/O19 or A4	I/O23 or A4	I/O21 or A4	I/O37(A) or A4	15	5	24	8	H2	14	17
—	—	—	I/O36(B)	—	—	—	—	—	—	18
I/O18	I/O22	I/O20	I/O35(A)	—	—	25	9	D3	15	19
I/O17 or A3	I/O21 or A3	I/O19 or A3	I/O34(A) or A3	16	6	26	10	E3	16	20
I/O16	I/O20	I/O18	I/O33(A)	—	7	27	11	F3	17	21
—	—	—	I/O32(B)	—	—	—	—	—	18	22
I/O15 or A2	I/O19 or A2	I/O17 or A2	I/O31(A) or A2	17	8	28	12	G3	19	23
—	I/O18	I/O16	I/O30(A)	—	—	29	13	H3	20	24
GND	GND	GND	GND	18	9	30	14	GND[2]	21	25
VSS	VSS	VSS	VSS	19	10	31	15	GND[2]	22	26
I/O14 or A1	I/O17 or A1	I/O15 or A1	I/O29(A) or A1	20	11	32	16	F4	23	27
—	—	—	I/O28(B)	—	—	—	—	—	24	28
—	I/O16	—	I/O27(A)	—	—	—	17	G4	25	29
I/O13 or A0	I/O15 or A0	I/O14 or A0	I/O26(A) or A0	21	12	33	18	H4	26	30
I/O12 or D7	I/O14 or D7	I/O13 or D7	I/O25(A) or D7	22	13	34	19	H5	27	31
—	—	—	I/O24(B)	—	—	—	—	—	28	32
I/O11 or D6	I/O13 or D6	I/O12 or D6	I/O23(A) or D6	23	14	35	20	J4	29	33
I/O10 or D5	I/O12 or D5	I/O11 or D5	I/O22(A) or D5	24	15	36	21	K4	30	34
VDD	VDD	VDD	VDD	25	16	37	22	PWR[1]	31	35
VCC	VCC	VCC	VCC	26	17	38	23	PWR[1]	32	36
I/O9	I/O11	I/O10	I/O21(A)	—	—	39	24	J3	33	37
—	—	—	I/O20(B)	—	—	—	—	—	34	38
I/O8 or D4	I/O10 or D4	I/O9 or D4	I/O19(A) or D4	27	18	40	25	K3	35	39
I/O7	I/O9	I/O8	I/O18(A)	—	19	41	26	L3	36	40
—	—	—	I/O17(A)	—	—	—	—	M3	37	41
—	—	—	I/O16(B)	—	—	—	—	—	—	42
I/O6 or D3	I/O8 or D3	I/O7 or D3	I/O15(A) or D3	28	20	42	27	N3	38	43
—	I/07	I/O6	I/014(A)	—	—	43	28	J2	39	44
—	—	—	I/O13(A)	—	—	—	—	K2	40	45
GND	GND	GND	GND	—	—	44	29	GND[2]	41	46
—	—	—	VSS	—	—	—	—	GND[2]	42	47
—	—	—	I/O12(B)	—	—	—	—	—	—	48
I/O5 or D2	I/O6 or D2	I/O5 or D2	I/O11(A) or D2	29	21	45	30	M2	43	49
I/O4	I/O5	I/O4	I/O10(A)	—	22	46	31	N2	44	50
—	—	—	I/O9(A)	—	—	—	—	P2	45	51
—	—	—	I/O8(B)	—	—	—	—	—	—	52
I/O3 or D1	I/O4 or D1	I/O3 or D1	I/O7(A) or D1	30	23	47	32	J1	46	53
I/O2	I/O3	I/O2	I/O6(A)	—	—	48	33	K1	47	54
—	—	—	I/O5(A)	—	—	—	—	L1	48	55
—	—	—	I/O4(B)	—	—	—	—	—	—	56
—	I/O2	—	I/O3(A)	—	—	—	34	M1	49	57
I/O1 or D0	I/O1 or D0	I/O1 or D0	I/O2(A) or D0	31	24	49	35	N1	50	58
—	—	—	I/O1(A)	—	—	—	—	P1	51	59
CCLK	CCLK	CCLK	CCLK	32	25	50	36	R1	52	60

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

Pinout Assignment (Continued)

Bottom Side (Left to Right)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
CON	CON	CON	CON	33	26	51	37	M5	53	61
—	—	—	I/O204(A)	—	—	—	—	M6	54	62
I/O96 or CEN	I/O120 or CEN	I/O108 or CEN	I/O203(A) or CEN	34	27	52	38	M7	55	63
—	I/O119	—	I/O202(A)	—	—	—	39	R2	56	64
—	—	—	I/O201(B)	—	—	—	—	—	—	65
—	—	—	VCC	—	—	—	—	PWR[1]	57	66
—	—	—	I/O200(A)	—	—	—	—	R3	58	67
—	—	—	GND	—	—	—	—	GND[2]	59	68
—	I/O118	I/O107	I/O199(A)	—	—	53	40	R5	60	69
I/O95 or CSOUT	I/O117 or CSOUT	I/O106 or CSOUT	I/O198(A) or CSOUT	35	28	54	41	R6	61	70
—	—	—	I/O197(B)	—	—	—	—	—	—	71
—	—	—	I/O196(A)	—	—	—	—	R7	62	72
I/O94	I/O116	I/O105	I/O195(A)	—	—	55	42	P3	63	73
I/O93	I/O115	I/O104	I/O194(A)	36	29	56	43	P4	64	74
—	—	—	I/O193(B)	—	—	—	—	—	—	75
—	—	—	I/O192(A)	—	—	—	—	P5	65	76
I/O92	I/O114	I/O103	I/O191(A)	—	30	57	44	P6	66	77
I/O91 or CHECK	I/O113 or CHECK	I/O102 or CHECK	I/O190(A) or CHECK	37	31	58	45	P7	67	78
—	—	—	I/O189(B)	—	—	—	—	—	—	79
I/O90	I/O112	I/O101	I/O188(A)	—	—	59	46	N4	68	80
I/O89 or ERR	I/O111 or ERR	I/O100 or ERR	I/O187(A) or ERR	38	32	60	47	N5	69	81
I/O88	I/O110	I/O99	I/O186(A)	—	33	61	48	N6	70	82
—	—	—	I/O185(B)	—	—	—	—	—	71	83
I/O87	I/O109	I/O98	I/O184(A)	39	34	62	49	N7	72	84
	I/O108	I/O97	I/O183(A)			63	50	M8	73	85
GND	GND	GND	GND	40	35	64	51	GND[2]	74	86
I/O86	I/O107	I/O96	I/O182(A)	41	36	65	52	M9	75	87
—	—	—	I/O181(B)	—	—	—	—	—	76	88
—	I/O106	—	I/O180(A)	—	—	—	53	M10	77	89
I/O85	I/O105	I/O95	I/O179(A)	42	37	66	54	M11	78	90
CS	CS	CS	CS	43	38	67	55	L8	79	91
I/O84	I/O104	I/O94	I/O178(A)	44	39	68	56	M12	80	92
—	—	—	I/O177(B)	—	—	—	—	—	81	93
I/O83	I/O103	I/O93	I/O176(A)	45	40	69	57	N8	82	94
—	—	—	VDD	—	—	—	—	PWR[1]	83	95
VCC	VCC	VCC	VCC	46	41	70	58	PWR[1]	84	96
I/O82	I/O102	I/O92	I/O175(A)	47	42	71	59	N11	85	97
I/O81	I/O101	I/O91	I/O174(A)	—	—	72	60	N12	86	98
—	—	—	I/O173(B)	—	—	—	—	—	87	99
I/O80	I/O100	I/O90	I/O172(A)	48	43	73	61	N13	88	100
I/O79	I/O99	I/O89	I/O171(A)	—	44	74	62	P8	89	101
—	—	—	I/O170(A)	—	—	—	—	P9	90	102
—	—	—	I/O169(B)	—	—	—	—	—	—	103
I/O78	I/O98	I/O88	I/O168(A)	49	45	75	63	P10	91	104
—	I/O97	I/O87	I/O167(A)	—	—	76	64	P11	92	105
—	—	—	I/O166(A)	—	—	—	—	P12	93	106
GND	GND	GND	GND	—	—	77	65	GND[2]	94	107
—	—	—	I/O165(B)	—	—	—	—	—	—	108
I/O77	I/O96	I/O86	I/O164(A)	50	46	78	66	P13	95	109
I/O76	I/O95	I/O85	I/O163(A)	—	47	79	67	P14	96	110
—	—	—	I/O162(A)	—	—	—	—	R8	97	111
—	—	—	I/O161(B)	—	—	—	—	—	—	112
I/O75	I/O94	I/O84	I/O160(A)	51	48	80	68	R9	98	113
I/O74	I/O93	I/O83	I/O159(A)	—	—	81	69	R10	99	114
—	—	—	I/O158(A)	—	—	—	—	R11	100	115
—	—	—	I/O157(B)	—	—	—	—	—	—	116
—	I/O92	—	I/O156(A)	—	—	—	70	R12	101	117
I/O73	I/O91	I/O82	I/O155(A)	52	49	82	71	R13	102	118
—	—	—	I/O154(A)	—	—	—	—	R14	103	119
RESET	RESET	RESET	RESET	53	50	83	72	R15	104	120

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

Pinout Assignment (Continued)

Right Side (Bottom to Top)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
—	—	—	I/O153(A)	—	—	—	—	P15	105	121
I/O72	I/O90	I/O81	I/O152(A)	54	51	84	73	N15	106	122
—	I/O89	I/O80	I/O151(A)	—	—	85[3]	74	M15	107	123
—	—	—	I/O150(B)	—	—	—	—	—	—	124
—	—	—	VCC	—	—	—	—	PWR[1]	108	125
—	—	—	I/O149(A)	—	—	—	—	L15	109	126
—	—	—	GND	—	—	—	—	GND[2]	110	127
—	I/O88	—	I/O148(A)	—	—	85[4]	75	J15	111	128
I/O71	I/O87	I/O79	I/O147(A)	55	52	86	76	H15	112	129
—	—	—	I/O146(B)	—	—	—	—	—	—	130
—	—	—	I/O145(A)	—	—	—	—	N14	113	131
I/O70	I/O86	I/O78	I/O144(A)	—	—	87	77	M14	114	132
I/O69	I/O85	I/O77	I/O143(A)	56	53	88	78	L14	115	133
—	—	—	I/O142(B)	—	—	—	—	—	—	134
—	—	—	I/O141(A)	—	—	—	—	K14	116	135
I/O68	I/O84	I/O76	I/O140(A)	—	54	89	79	J14	117	136
I/O67	I/O83	I/O75	I/O139(A)	57	55	90	80	H14	118	137
—	—	—	I/O138(B)	—	—	—	—	—	—	138
I/O66	I/O82	I/O74	I/O137(A)	—	—	91	81	M13	119	139
I/O65	I/O81	I/O73	I/O136(A)	58	56	92	82	L13	120	140
I/O64	I/O80	I/O72	I/O135(A)	—	57	93	83	K13	121	141
—	—	—	I/O134(B)	—	—	—	—	—	122	142
I/O63	I/O79	I/O71	I/O133(A)	59	58	94	84	J13	123	143
—	I/O78	I/O70	I/O132(A)	—	—	95	85	H13	124	144
GND	GND	GND	GND	60	59	96	86	GND[2]	125	145
VSS	VSS	VSS	VSS	61	60	97	87	GND[2]	126	146
I/O62	I/O77	I/O69	I/O131(A)	62	61	98	88	K12	127	147
—	—	—	I/O130(B)	—	—	—	—	—	128	148
—	I/O76	—	I/O129(A)	—	—	—	89	J12	129	149
I/O61	I/O75	I/O68	I/O128(A)	63	62	99	90	H12	130	150
I/O60	I/O74	I/O67	I/O127(A)	64	63	100	91	H11	131	151
—	—	—	I/O126(B)	—	—	—	—	—	132	152
I/O59	I/O73	I/O66	I/O125(A)	65	64	101	92	G12	133	153
I/O58	I/O72	I/O65	I/O124(A)	66	65	102	93	F12	134	154
VDD	VDD	VDD	VDD	67	66	103	94	PWR[1]	135	155
VCC	VCC	VCC	VCC	68	67	104	95	PWR[1]	136	156
I/O57	I/O71	I/O64	I/O123(A)	—	—	105	96	G13	137	157
—	—	—	I/O122(B)	—	—	—	—	—	138	158
I/O56	I/O70	I/O63	I/O121(A)	69	68	106	97	F13	139	159
I/O55	I/O69	I/O62	I/O120(A)	—	69	107	98	E13	140	160
—	—	—	I/O119(A)	—	—	—	—	D13	141	161
—	—	—	I/O118(B)	—	—		—	—	—	162
I/O54	I/O68	I/O61	I/O117(A)	70	70	108	99	C13	142	163
—	I/O67	I/O60	I/O116(A)	—	—	109	100	G14	143	164
—	—	—	I/O115(A)	—	—	—	—	F14	144	165
GND	GND	GND	GND	—	—	110	101	GND[2]	145	166
—	—	—	VSS	—	—	—	—	GND[2]	146	167
—	—	—	I/O114(B)	—	—	—	—	—	—	168
I/O53	I/O66	I/O59	I/O113(A)	71	71	111	102	D14	147	169
I/O52	I/O65	I/O58	I/O112(A)	—	72	112	103	C14	148	170
—	—	—	I/O111(A)	—	—	—	—	B14	149	171
—	—	—	I/O110(B)	—	—	—	—	—	—	172
I/O51	I/O64	I/O57	I/O109(A)	72	73	113	104	G15	150	173
I/O50	I/O63	I/O56	I/O108(A)	—	—	114	105	F15	151	174
—	—	—	I/O107(A)	—	—	—	—	E15	152	175
—	—	—	I/O106(B)	—	—	—	—	—	—	176
—	I/O62	—	I/O105(A)	—	—	—	106	D15	153	177
I/O49	I/O61	I/O55	I/O104(A)	73	74	115	107	C15	154	178
—	—	—	I/O103(A)	—	—	—	—	B15	155	179
M2	M2	M2	M2	74	75	116	108	A15	156	180

Notes:
1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.
3. 85 = Pin 85 on AT6005.
4. 85 = pin 85 on AT6003 and AT6010.

Pinout Assignment (Continued)

Top Side (Right to Left)										
AT6002	AT6003	AT6005	AT6010	84 PLCC	100 VQFP	132 PQFP	144 TQFP	180 CPGA	208 PQFP	240 PQFP
M1	M1	M1	M1	75	76	117	109	D11	157	181
—	—	—	I/O102(A)	—	—	—	—	D10	158	182
I/O48	I/O60	I/O54	I/O101(A)	76	77	118	110	D9	159	183
—	I/O59	—	I/O100(A)	—	—	—	111	A14	160	184
—	—	—	I/O99(B)	—	—	—	—	—	—	185
—	—	—	VCC	—	—	—	—	PWR[1]	161	186
—	—	—	I/O98(A)	—	—	—	—	A13	162	187
—	—	—	GND	—	—	—	—	GND[2]	163	188
—	I/O58	I/O53	I/O97(A)	—	—	119	112	A11	164	189
I/O47	I/O57	I/O52	I/O96(A)	77	78	120	113	A10	165	190
—	—	—	I/O95(B)	—	—	—	—	—	—	191
—	—	—	I/O94(A)	—	—	—	—	A9	166	192
I/O46	I/O56	I/O51	I/O93(A)	—	—	121	114	B13	167	193
I/O45	I/O55	I/O50	I/O92(A)	78	79	122	115	B12	168	194
—	—	—	I/O91(B)	—	—	—	—	—	—	195
—	—	—	I/O90(A)	—	—	—	—	B11	169	196
I/O44	I/O54	I/O49	I/O89(A)	—	80	123	116	B10	170	197
I/O43	I/O53	I/O48	I/O88(A)	79	81	124	117	B9	171	198
—	—	—	I/O87(B)	—	—	—	—	—	—	199
I/O42	I/O52	I/O47	I/O86(A)	—	—	125	118	C12	172	200
I/O41	I/O51	I/O46	I/O85(A)	80	82	126	119	C11	173	201
I/O40	I/O50	I/O45	I/O84(A)	—	83	127	120	C10	174	202
—	—	—	I/O83(B)	—	—	—	—	—	175	203
I/O39	I/O49	I/O44	I/O82(A)	81	84	128	121	C9	176	204
—	I/O48	I/O43	I/O81(A)	—	—	129	122	D8	177	205
GND	GND	GND	GND	82	85	130	123	GND[2]	178	206
I/O38	I/O47	I/O42	I/O80(A)	83	86	131	124	D7	179	207
—	—	—	I/O79(B)	—	—	—	—	—	180	208
—	I/O46	—	I/O78(A)	—	—	—	125	D6	181	209
I/O37 or A16	I/O45 or A16	I/O41 or A16	I/O77(A) or A16	84	87	132	126	D5	182	210
CLOCK	CLOCK	CLOCK	CLOCK	1	88	1	127	E8	183	211
I/O36 or A15	I/O44 or A15	I/O40 or A15	I/O76(A) or A15	2	89	2	128	D4	184	212
—	—	—	I/O75(B)	—	—	—	—	—	185	213
I/O35 or A14	I/O43 or A14	I/O39 or A14	I/O74(A) or A14	3	90	3	129	C8	186	214
—	—	—	VDD	—	—	—	—	PWR[1]	187	215
VCC	VCC	VCC	VCC	4	91	4	130	PWR[1]	188	216
I/O34 or A13	I/O42 or A13	I/O38 or A13	I/O73(A) or A13	5	92	5	131	C5	189	217
I/O33	I/O41	I/O37	I/O72(A)	—	—	6	132	C4	190	218
—	—	—	I/O71(B)	—	—	—	—	—	191	219
I/O32 or A12	I/O40 or A12	I/O36 or A12	I/O70(A) or A12	6	93	7	133	C3	192	220
I/O31	I/O39	I/O35	I/O69(A)	—	94	8	134	B8	193	221
—	—	—	I/O68(A)	—	—	—	—	B7	194	222
—	—	—	I/O67(B)	—	—	—	—	—	—	223
I/O30 or A11	I/O38 or A11	I/O34 or A11	I/O66(A) or A11	7	95	9	135	B6	195	224
—	I/O37	I/O33	I/O65(A)	—	—	10	136	B5	196	225
—	—	—	I/O64(A)	—	—	—	—	B4	197	226
GND	GND	GND	GND	—	—	11	137	GND[2]	198	227
—	—	—	I/O63(B)	—	—	—	—	—	—	228
I/O29 or A10	I/O36 or A10	I/O32 or A10	I/O62(A) or A10	8	96	12	138	B3	199	229
I/O28	I/O35	I/O31	I/O61(A)	—	97	13	139	B2	200	230
—	—	—	I/O60(A)	—	—	—	—	A8	201	231
—	—	—	I/O59(B)	—	—	—	—	—	—	232
I/O27 or A9	I/O34 or A9	I/O30 or A9	I/O58(A) or A9	9	98	14	140	A7	202	233
I/O26	I/O33	I/O29	I/O57(A)	—	—	15	141	A6	203	234
—	—	—	I/O56(A)	—	—	—	—	A5	204	235
—	—	—	I/O55(B)	—	—	—	—	—	—	236
—	I/O32	—	I/O54(A)	—	—	—	142	A4	205	237
I/O25 or A8	I/O31 or A8	I/O28 or A8	I/O53(A) or A8	10	99	16	143	A3	206	238
—	—	—	I/O52(A)	—	—	—	—	A2	207	239
M0	M0	M0	M0	11	100	17	144	A1	208	240

Notes: 1. PWR = Pins connected to power plane = F1, E4/E5, L2, R4, K15, L12, E14, A12.
2. GND = Pins connected to ground plane = L4, M4, N9, N10, E12, D12, C7, C6.

A.C. Timing Characteristics

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: Vcc = 4.75 V to 5.25 V. Temperature = 0°C to 70°C.

Cell Function	Parameter	From	To	Load	- 2	- 4	Units
Wire (4)	t_{PD} (max) (4)	A, B, L	A, B	1	1.2	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	2.2	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	2.4	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	2.2	3.2	ns
MUX	t_{PD} (max)	A, B	A	1	2.3	4.0	ns
		L	A	1	3.0	4.9	ns
D-Flip-Flop (5)	t_{setup} (min)	A, B, L	CLK		2.0	3.0	ns
D-Flip-Flop (5)	t_{hold} (min)	CLK	A, B, L		0.0	0.0	ns
D-Flip-Flop	t_{PD} (max)	CLK	A	1	2.0	3.0	ns
Bus Driver	t_{PD} (max)	A	L	2	2.6	4.0	ns
Repeater	t_{PD} (max)	L, E	E	3	1.6	2.3	ns
		L, E	L	2	2.1	3.0	ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	2.4	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	2.4	3.0	ns
Clock Buffer (5)	t_{PD} (max)	CLOCK PIN	GCLK	4	2.0	2.9	ns
Reset Buffer (5)	t_{PD} (max)	RESET PIN	GRES	5	1.9	2.8	ns
TTL Input (1)	t_{PD} (max)	I/O	A	3	1.2	1.5	ns
CMOS Input (2)	t_{PD} (max)	I/O	A	3	1.4	2.3	ns
Fast Output (3)	t_{PD} (max)	A	I/O PIN	6	3.5	6.0	ns
Slow Output (3)	t_{PD} (max)	A	I/O PIN	6	8.0	12.0	ns
Output Disable (5)	t_{PXZ} (max)	L	I/O PIN	6	3.3	5.5	ns
Fast Enable (3, 5)	t_{PZX} (max)	L	I/O PIN	6	4.0	6.5	ns
Slow Enable (3, 5)	t_{PZX} (max)	L	I/O PIN	6	8.5	12.5	ns

Device	Cell Types	Outputs	Icc (max)
Cell (6)	Wire, XWire, Half-Adder, Flip-Flop	A, B	4.5 µA/MHz
Bus (6)	Wire, XWire, Half-Adder, Flip-Flop, Repeater	L	2.5 µA/MHz
Column Clock (6)	Column Clock Driver	CLK	40 µA/MHz

Notes:
1. TTL buffer delays are measured from a V_{IH} of 1.5 V at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
3. Buffer delay is to a pad V_{IH} of 1.5 V with one output switching.
4. Max specifications are the average of max t_{PDLH} and t_{PDHL}
5. Parameter based on characterization and simulation; not tested in production.
6. Exact power calculation is available in an Atmel application note.

Load Definition:
1. Load of one A or B input
2. Load of one L input
3. Constant Load
4. Load of 28 Clock Columns
5. Load of 28 Reset Columns
6. Tester Load of 50 pF

Absolute Maximum Ratings*

Supply Voltage (V_{CC})	-0.5 V to +7.0 V
DC Input Voltage (V_{IN})	-0.5 V to VCC + 0.5 V
DC Output Voltage (V_{ON})	-0.5 V to VCC + 0.5 V
Storage Temperature Range (TSTG)	-65°C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP}=1.5K, C_{ZAP}=100 pF)	2000 V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2

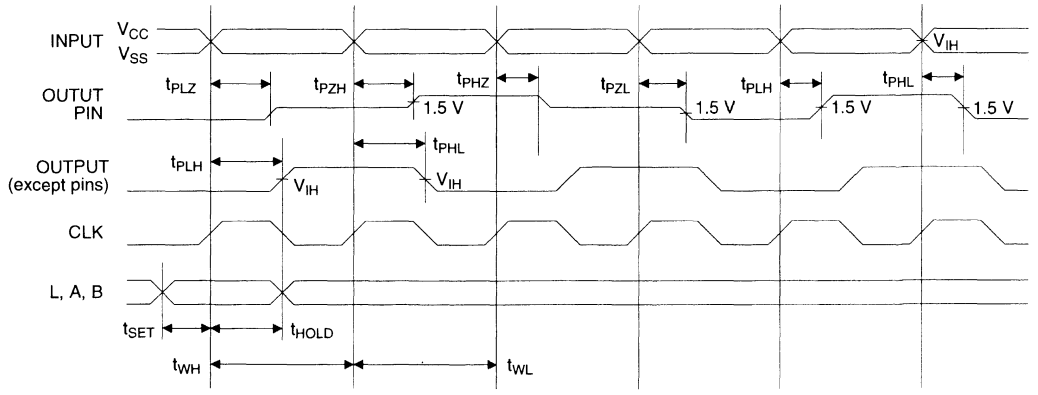
D.C. and A.C. Operating Range

		AT6002-2/4 AT6003-2/4 AT6005-2/4 AT6010-2/4 Commercial	AT6002-2/4 AT6003-2/4 AT6005-2/4 AT6010-2/4 Industrial	AT6002-4 AT6003-4 AT6005-4 AT6010-4 Military
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%
Input Voltage Level (TTL)	High (V_{IHT})	2.0 V - V_{CC}	2.0 V - V_{CC}	2.0 V - V_{CC}
	Low (V_{ILT})	0 V - 0.8 V	0 V - 0.8 V	0 V - 0.8 V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% VCC	0 - 30% V_{CC}
Input Signal Transition Time	(T_{IN})	50 ns (max)	50 ns (max)	50 ns (max)

D.C. Characteristics

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	High-Level Input Voltage	Commercial	CMOS	70% V_{CC}	V_{CC}	V
			TTL	2.0	V_{CC}	V
V_{IL}	Low-Level Input Voltage	Commercial	CMOS	0	20% V_{CC}	V
			TTL	0	0.8	V
V_{OH}	High-Level Output Voltage	Commercial	I_{OH} = -4 mA, V_{CC} min	3.9		V
			I_{OH} = -16 mA, V_{CC} min	3.0		V
V_{OL}	Low-Level Output Voltage	Commercial	I_{OL} = -4 mA, V_{CC} min		0.4	V
			I_{OL} = -16 mA, V_{CC} min		0.5	V
I_{OZH}	High-Level Tristate Output Leakage Current	V_O = V_{CC} (max)			10	µA
I_{OZL}	Low-Level Tristate	Without Pull-Up, V_O = V_{SS}		-10		µA
	Output Leakage Current	With Pull-Up, V_O = V_{SS}		-500		µA
I_{IH}	High-Level Input Current	VIN = V_{CC} (max)			10	µA
I_{IL}	Low-Level Input Current	Without Pull-Up, V_{IN} = V_{SS}		-10		µA
		With Pull-Up, V_{IN} = V_{SS}		-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator (Standby)			500	µA
C_{IN}	Input Capacitance	All Pins			10	pF

Device Timing: During Operation



Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
2,000	2	AT6002-2AC AT6002A-2AC AT6002-2JC AT6002-2QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
2,000	4	AT6002-4AC AT6002A-4AC AT6002-4JC AT6002-4QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
		AT6002-4AI AT6002A-4AI AT6002-4JI AT6002-4QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
3,000	2	AT6003-2AC AT6003A-2AC AT6003-2JC AT6003-2QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
3,000	4	AT6003-4AC AT6003A-4AC AT6003-4JC AT6003-4QC	100A 144A 84J 132Q	Commercial (0°C to 70°C)
		AT6003-4AI AT6003A-4AI AT6003-4JI AT6003-4QI	100A 144A 84J 132Q	Industrial (-40°C to 85°C)

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
5,000	2	AT6005-2AC AT6005A-2AC AT6005-2JC AT6005-2QC AT6005-2UC	100A 144A 84J 132Q 180U	Commercial (0°C to 70°C)
5,000	4	AT6005-4AC AT6005A-4AC AT6005-4JC AT6005-4QC AT6005-4UC	100A 144A 84J 132Q 180U	Commercial (0°C to 70°C)
		AT6005-4AI AT6005A-4AI AT6005-4JI AT6005-4QI AT6005-4UI	100A 144A 84J 132Q 180U	Industrial (-40°C to 85°C)

Ordering Information

Usable Gates	Speed Grade (ns)	Ordering Code	Package	Operation Range
10,000	2	AT6010A-2AC AT6010-2QC AT6010-2UC AT6010A-2QC AT6010H-2QC	144A 132Q 180U 208Q 240Q	Commercial (0°C to 70°C)
10,000	4	AT6010A-4AC AT6010-4QC AT6010-4UC AT6010A-4QC AT6010H-4QC	144A 132Q 180U 208Q 240Q	Commercial (0°C to 70°C)
		AT6010A-4AI AT6010A-4QI AT6010-4UI AT6010A-4QI AT6010H-4UI	144A 132Q 180U 208Q 240Q	Industrial (-40°C to 85°C)

Ordering Information

Package Type	
84J	84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
100A	100 Lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
144A	144 Lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
180U	180 Pin, Ceramic Pin Grid Array (PGA)
132Q	132 Lead, Bumpered Plastic Gull Wing Quad Flat Package (BQFP)
208Q	208 Lead, Plastic Gull-Wing Quad Flat Package (PQFP)
240Q	240 Lead, Plastic Gull-Wing Quad Flat Package (PQFP)

Field Programmable Gate Array

Configuration Guide

AT6000 Series Configuration

Configuration is the process of loading a design into an AT6000 Series field programmable gate array (FPGA). AT6000 Series devices are SRAM-based and can be configured any number of times. The entire device or select portions of a design can be configured. Sections of the device can be configured while others continue to operate undisturbed.

Configuration data is transferred to the device in one of six modes. Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is operating. Three pins, M0, M1 and M2 determine the configuration mode (Table 1). The number of dual-function pins required for each mode varies (Table 2).

One of the modes is automatically initiated after power-up reboot; the others are initiated by the user. Configuration data can come from a variety of external logic sources, including a PC parallel port, microprocessor, EPROM or E^2PROM Serial Configuration Memory (AT17128).

The user determines the configuration mode for loading the bit pattern into the device. The Integrated Development System generates the SRAM bit pattern required to configure an AT6000 Series FPGA. Many factors can influence the user's choice of configuration mode, including device size, board space, required configuration speed, number of devices to be configured, and design size.

This document suggests guidelines for device configuration and describes each of the configuration modes in detail.

A basic understanding of the device architecture, as described in the AT6000 Series data sheet, is assumed.

Features

Variety of Formats

- PC Parallel Port
- Microprocessor
- Serial/Parallel EPROM
- Serial/Parallel E^2PROM

Configuration Windows

- Full or Partial Reconfiguration
- Bit-Stream Compression Algorithm

Reprogrammable

- Download Configuration any Number of Times
- Reconfigure In-System Down to Cell Level

Fast

- Full Configuration: 1-8 Milliseconds
- Partial Configuration: 0.2 µseconds/Cell

0436A

Table 1. AT6000 Series Configuration Modes

Mode	Description	M2	M1	M0	Application
0	Configuration Reset	0	0	0	Clearing the Device
1	Address Count-Up, External CCLK	0	0	1	Fast Configuration; Parallel EPROM
2	Address Count-Down, External CCLK	0	1	0	Fast Configuration; Parallel EPROM
3	Bit-Sequential, External CCLK	0	1	1	Serial Communication Port to UART
4	Bit-Sequential, Internal CCLK	1	0	0	Serial EPROM; Auto Configuration
5	Address Count-Up, Internal CCLK	1	0	1	Parallel EPROM
6	Byte-Sequential, External CCLK	1	1	0	Parallel Port of Microprocessor

Configuration Modes

Powering up an AT6000 Series FPGA is a three-step process. When power is first applied, the device enters an initialization state that takes up to 16 milliseconds and resets the SRAM to all zeros. Cells in the array become cross wires with no A or B inputs selected, all bus drivers are switched off, repeaters are disabled, I/Os are set as TTL inputs with the pull-up enabled, column clocks are set to "0," and column resets are set to "1."

After initialization, the device enters the configuration state and writes to the memory bits that control cell functionality and interconnection.

Seven configuration modes are available:

Mode 0:Configuration Reset
Mode 1:Address Count-Up, External CCLK
Mode 2:Address Count-Down, External CCLK
Mode 3:Bit-Sequential, External CCLK
Mode 4:Bit Sequential, Internal CCLK
Mode 5:Address Count-Up, Internal CCLK
Mode 6:Byte-Sequential, External CCLK

Mode 0 is not a true configuration mode because it does not load a design into the FPGA. Instead, mode 0 initiates the reboot sequence and clears the device, preparing it for configuration or reconfiguration.

Modes 1, 2 and 5 generate external address outputs so the user can conveniently access sequential data from a standard parallel EPROM. The generated output addresses bear no relation to the internal addresses of the FPGA's configuration SRAM, they simply count up or down with each CCLK edge to create a sequential byte stream. Mode 6 is similar to modes 1, 2 and 5 but assumes a system-generated bit stream and does not generate external address outputs. Modes 3 and 4 use a serial bit stream received from the system, an industry-standard E^2PROM (AT17C65/128/256) or the download cable provided with the Integrated Development System. The data in each byte is serialized with the least-significant-bit supplied first. Mode 4 can be initiated automatically by the FPGA with the AT17C65/128/256 Serial Configuration Memory.

Modes 3 and 4 will typically be the most popular configuration modes because they require the fewest pins and receive data from small foot-print serial E^2PROMs that take up little board space.

Pins used for Configuration

AT6000 Series FPGAs have three kinds of pins: dedicated I/O pins, dedicated configuration pins, and dual-function pins which act as I/O during operation but are used for various control signals during configuration. (For more on device pins refer to the AT6000 Series data sheet.)

Dedicated Configuration Pins

There are six signals dedicated to programming: M0, M1, M2, CCLK, $\overline{\text{CON}}$ and $\overline{\text{CS}}$.

M0, M1, M2

The mode pins are inputs that determine the configuration mode to be used. Table 1 (this page) lists the states for each configuration mode. M0, M1 and M2 can be fixed in modes 1 through 6 and ignored. Mode 0, configuration reset, can be initiated by asynchronously driving M0, M1 and M2 low, then returning them to the proper mode selection value.

CCLK

CCLK is the configuration clock signal. It is an input or an output depending on the mode of operation. In modes 1, 2, 3 and 6 it is an input, in modes 4 and 5 it is an output with a typical frequency of 1 MHz. In all modes, the rising edge of the CCLK signal is used to sample inputs and change outputs.

$\overline{\text{CON}}$

CON is a bidirectional open-collector pin that provides the configuration control and status signal. Configuration starts on the first CCLK edge when $\overline{\text{CON}}$ is driven and held low. Configuration continues until $\overline{\text{CON}}$ is pulled high by a pull-up or by the configuration system. $\overline{\text{CON}}$ is driven low by the device until

Table 2. Dual-Function Pin Usage

N = Not used, R = Required, O = Optional

Mode	Minimum Dual-Function Pins	Optional Dual-Function Pins	A0-16 Outputs	D0 Input	D1-7 Inputs	$\overline{\text{CHECK}}$ Input	$\overline{\text{ERR}}$ Output	$\overline{\text{CSOUT}}$ Output
0	0	0	N	N	N	N	N	N
1	25	4	R	R	R	O	O	O
2	25	4	R	R	R	O	O	O
3	1	3	N	R	N	O	O	O
4	1	3	N	R	N	O	O	O
5	25	4	R	R	R	O	O	O
6	8	3	N	R	R	O	O	O

configuration is complete. The device moves to the operation state on the first CCLK edge after $\overline{\text{CON}}$ is high.

$\overline{\text{CS}}$

$\overline{\text{CS}}$ is the configuration chip select pin. $\overline{\text{CS}}$ must be low for configuration to occur. Pulling $\overline{\text{CS}}$ high during configuration does not stop the process, but the pin should be held low throughout configuration. $\overline{\text{CS}}$ can be used to cascade devices (see Figures 9 and 14) and create an addressed, multiple-device programming system (see Figure 15).

Dual-Function Pins

Dual-function pins are programming pins during configuration and I/O pins during operation. The number of dual-function pins used during configuration varies from mode to mode. Some dual-function pins act as configuration status pins and are optional regardless of mode. The optional pins are most useful when cascading devices to program multiple FPGAs from a single data source. Table 2 lists the dual-function pins used with each mode.

D0-D7

D0-D7 are data input pins. Parallel modes 1, 2, 5 and 6 use all eight data inputs, serial modes 3 and 4 use only one, D0.

$\overline{\text{CEN}}$ or I/O

During address count-up/down configuration, $\overline{\text{CEN}}$ is an output. $\overline{\text{CEN}}$ can be used as the output enable of a parallel EPROM. In this case, it should be configured as a constant high, and not used as a configurable I/O pin. For the AT6002, AT6003, and AT6005, $\overline{\text{CEN}}$ output is enabled after powerup and/or reboot. It switeches low one clock after CON is activated. It may become inactive one clock after the loading of the configuration control register during a configuration download, depending on the value of bit B7. $\overline{\text{CEN}}$ is active for modes 1,2,3,4,5, and 6. For the AT6010, $\overline{\text{CEN}}$ output is disabled after powerup and/or reboot. It may become active one clock after the loading of the configuration control register during a configuration download, depending on the value of B7. $\overline{\text{CEN}}$ is active for modes 1,2, and 5 only.

A0-A16

A0-A16 are address output signals, used by modes 1, 2 and 5, to drive an EPROM or other external addressed-memory device.

$\overline{\text{CSOUT}}$

CSOUT drives $\overline{\text{CS}}$ of the next device in a configuration chain.

$\overline{\text{CHECK}}$

$\overline{\text{CHECK}}$ is an input that enables an internal SRAM checking feature when used without B3 of the Configuration Control Register.

ERR

ERR is an output that switches low when an error is detected. It is used with the $\overline{\text{CHECK}}$ function, or when protocol errors occur during configuration. CHECK and $\overline{\text{ERR}}$ work together to perform simple and advanced diagnostic tests. For example, they can be used to verify the accuracy of a configuration run. With the $\overline{\text{CHECK}}$ pin low, download the configuration file a second time. The device systematically compares the data values in the configuration file with the data already programmed into the device's SRAM. If a mismatch is found, the $\overline{\text{ERR}}$ pin switches and remains low until the end of the configuration cycle.

Pin Status

The status of dual-function pins is determined by the device state. All I/Os are disabled during initialization. To move from the initialization state to configuration, the $\overline{\text{CON}}$ and $\overline{\text{CS}}$ pins are driven low. During configuration, the dual-function pins used by the selected mode are converted to inputs and outputs as required. To move from the configuration state to operation, the configuration file must be loaded completely and either $\overline{\text{CON}}$ or $\overline{\text{CS}}$ must be high. During operation, the I/O pins behave according to the specified design.

Control Register

The Integrated Development System generates the bit-stream file used to configure the FPGA. In addition to the actual data to be loaded into the SRAM, the bit stream loads a control register containing eight bits used to control various configuration sequence parameters (Figure 1).

Figure 1. Control Register

B7	B6	B5	B4	B3	B2	B1	B0

B0

B0 controls the value of the device's memory address counter after each configuration sequence. The default resets the value, so subsequent configuration sequences load the configuration file from the same address. In modes 1 and 5, the default address is 0000, in mode 2 it is 1FFFF. When B0 is set, the memory address counter retains its last value, so the user can store multiple designs sequentially in an External Memory Device.

B1

B1 controls loading of a jump address into the device's memory address counter. The default ignores any jump addresses. With B1 set, the memory address counter jumps to the specified address. Using B1, configuration files can be stored as a continuous stream or as a pointer-based list.

B2

B2 controls operation of the dual-function pin $\overline{\text{CSOUT}}$. When B2 is set, this pin is disabled. This is useful when a minimum pin-count configuration is desired.

B3

B3 controls the operation of the dual-function pins $\overline{\text{ERR}}$ and $\overline{\text{CHECK}}$. When B3 is set, both pins are disabled. This is useful when a minimum pin-count configuration is desired, or when design security is a concern.

B4

B4 controls the writing of configuration data after the initialization state. When B4 is set, configuration data can not be written into the device by subsequent configuration cycles. B4 can only be reset by rebooting the device.

B5 and B6

B5 and B6 control the operation of the global clock signal received through the CLOCK pin:

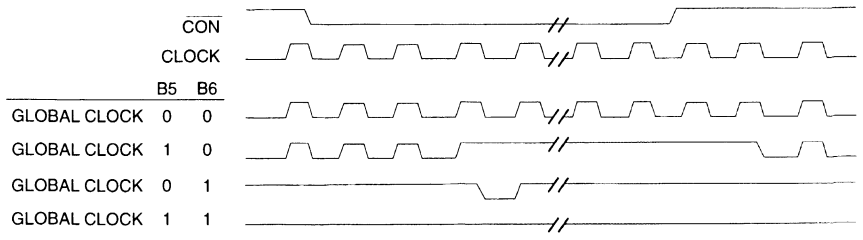
B5	B6	Global Clock Operation
0	0	Normal operation.
1	0	Stops after third rising edge of CLOCK after $\overline{\text{CON}}$ is low. Continues after second rising edge of CLOCK after CON is high.
0	1	Stops after fourth rising edge of CLOCK after CON is high. Each configuration cycle thereafter, it receives one pulse after the third rising edge of CLOCK after $\overline{\text{CON}}$ is low.
1	1	Stops at second rising edge of CLOCK after CON is high. Remains stopped regardless of $\overline{\text{CON}}$.

Figure 2 shows the waveforms associated with each combination.

B7

B7 controls the $\overline{\text{CEN}}$ pin. When B7 is set, $\overline{\text{CEN}}$ is disabled.

Figure 2. Global Clock Signal During Operation



Configuration State Machine

Configuration is executed by a synchronous state machine that controls the flow of configuration data into the FPGA (Figure 3). The state machine is clocked by CCLK whether the signal is externally supplied or generated internally. On each CCLK cycle a different byte or bit of the configuration file is loaded into the state machine.

Data flow is controlled by the external input signals M0, M1, M2, $\overline{CON}$, $\overline{CS}$, $\overline{CHECK}$, D0-D7 and the values in the configuration control register. The state machine generates all the internal control signals as well as the A0-A16 output signals, $\overline{ERR}$ output, and $\overline{CSOUT}$ signal. Data is loaded into the device in a stream format and has no absolute address.

The process starts on power-up or when a mode 0 reset is applied. The reboot phase lasts for approximately 8000 up to approximately 16000 internal clock cycles while all the internal SRAM cells are written to a "0" value. During reboot the mode pins are sampled and the configuration-clock output starts.

Mode 4 supports automatic configuration. During reboot, the CCLK pin is enabled for output. After reboot, mode 4 releases the $\overline{CON}$ pin, allowing it to be pulled high, and then drives it low again to begin a configuration cycle automatically.

In the modes 1,2,3 and 6, CCLK remains an input but is ignored until the reboot process is complete. After reboot, the other modes release $\overline{CON}$ and allow it to float high. Control of the state machine is then transferred from the internal clock to the CCLK input signal. The device remains in idle until the $\overline{CON}$ pin is driven low.

Driving $\overline{CON}$ low puts the device in the preamble check loop, a synchronizing procedure for both parallel and serial configuration modes. Configuration is dependent on the sequence of data, and the preamble specifies the first byte of the data stream. In modes 3 and 4, the preamble also defines the byte boundary of serial data, which may be parallel before being processed by the state machine.

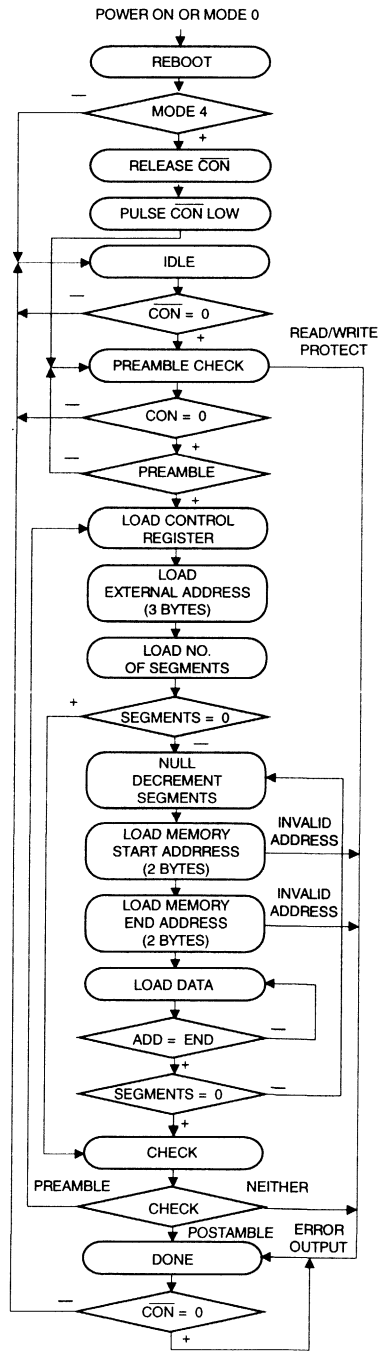
The first error test is done during the preamble check. If a read or write protect bit appears in the control register of the preamble, the $\overline{ERR}$ pin goes low and the device goes directly to the done state.

After the preamble check, the state machine loads the configuration control register and drives and holds the $\overline{CON}$ signal low until configuration is complete. Loading the configuration control register puts the next byte in the stream file into the control register, which controls features and variations in the configuration process.

The state machine then loads the next three bytes into a temporary register used to parallel-load the external address counter. This action is similar to a microprocessor "jump" command. The address bytes are loaded in all modes, but the jump can only be used by modes 1, 2 and 5.

The next byte in the stream file indicates the number of data strings, or segments. A single file can have 0 to 255 segments. The byte is loaded into a counter which is decremented at the end of each data string until it reaches zero and configuration is complete.

Figure 3. Configuration State Machine



If the register count is not zero, the state machine loads a null byte. If the B1 bit of the control register is equal to one the first time the state machine enters the null state, the external address is loaded. The byte loaded, while in the null state, is not used. If the segment count is zero, the state machine goes to the check state.

The data segment loop consists of the null byte, two bytes which load the internal pointer start address, two bytes which load the internal pointer end address, and enough data bytes to equal the difference between the end points. The state machine loops, loading data and incrementing the address counter, until the internal address pointer equals the end address pointer. Then it checks the segment counter. If more segments are to be loaded, the machine returns to the null state; and the data segment loop is executed again. If the segment counter is zero, the state machine goes to the check state. If an invalid value is encountered for the internal start or end address, the $\overline{ERR}$ signal switches low; and the state machine moves directly to the done state.

In the check state, the next byte in the stream file is examined. When a single device is being configured, this byte is a postamble, and the state machine moves to the done state. When devices are cascaded together for multiple configurations, this byte is a preamble for the next configuration file. The state machine transfers the data to the downstream device and monitors the downstream bit stream data to determine the next check for a preamble byte. If the state machine encounters a byte that isn't a preamble or a postamble, the $\overline{ERR}$ signal switches low; and the state machine enters the done state.

The done state releases the $\overline{CON}$ pin and loops until $\overline{CON}$ goes high and the device enters the idle state. In modes 1, 2, 5 and 6, the device enters the idle state three CCLK edges after $\overline{CON}$ is high. In modes 3 and 4, it takes twenty-four CCLK edges for the device to reach idle. The CCLK signal must therefore continue after the postamble until the device reaches the idle state.

Partial Configuration

Figure 4 gives the bit stream file used to configure a hypothetical device that has a 6 x 6 array of cells lined with four I/O on each side. Configuration begins with the bottom left cell, number 0, and ends with the upper right cell, number 35. Then the I/O cells are configured, beginning at number 36 and proceeding clockwise to number 51.

By placing windows in the bit stream file, it is possible to configure only a portion of the array. Figure 5 gives the bit stream file used to configure the lower right portion of the array and I/Os 45, 46 and 47— the program leaves darkened cells untouched.

On line six the program states that there are four segments of data to configure. The start address is the left-most cell in the bottom row to be configured, number 9, and the end address is the right-most cell in the row, number 11. Four bytes of data are used to load the cell between the two points, number 10. The next segment configures the row above. Notice that the cells between the first segment end address and the second segment start address are omitted. The data in these cells is left untouched— only the cell being programmed on a given clock cycle is changed. The other cells function as if in their normal operational mode. This means a portion of the array can be configured while the rest of the array remains operational.

Configuration Compression

A configuration compression algorithm, included in the Integrated Development System, uses windowing to compress the configuration file. On power-up, all cells in the FPGA are programmed to be logical zeros. Unused cells in a design remain zeros, so they do not need to be configured. The compression algorithm skips unused cells and can reduce file size by up tp 80%. This in turn reduces configuration time and memory storage requirements. It even makes designs less susceptible to reverse engineering, due to the random start and end array addresses in the compressed bit stream. For more information about the configuration compression algorithm, refer to the FPGA application notes.

Bit-Stream Sizes (bytes of data)

Mode(s)	Type [1, 2]	Beginning Sequence	6002	6003	6005	6010
1	P	Preamble	2677	4153	8077	16393
2	P	Preamble	2677	4153	8077	16393
3	S	Null Byte/Preamble	2678	4154	8078	16394
4	S	Null Byte/Preamble	2678	4154	8078	16394
5	P	Preamble	2677	4153	8077	16393
6	P	Preamble/Preamble	2678	4154	8078	16394

Notes: 1. P = Parallel.
2. S = Serial.

Figure 4. Full Configuration Example

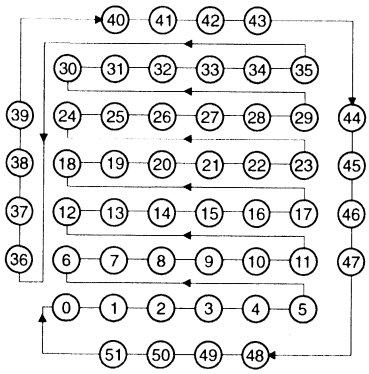
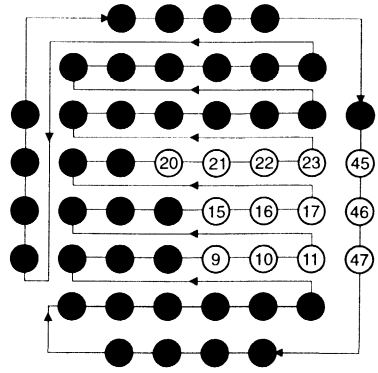


Figure 5. Partial Configuration Example



Full Configuration

```
10110010  ; preamble
00000000; control register
00000000; external address lsb
00000000;
00000000; external address msb
11111110; number of window segments
00000000; null
00000000; start address
00000000;
00000000; end address
00110011;
00000000; data
00000001
00000010
00000011
00000100
.
.
00110010
00110011
01001101; postamble
```

Partial Configuration

```
10110010  ; preamble
00000000; control register
00000000; external address lsb
00000000;
00000000; external address msb
11111011; number of window segments
00000000; null
00000000; start address segment 1
00001001;
00000000; end address
00010011;
00001001; data
00001010
00001011
00000000; null
00000000; start address segment 2
00001111;
00000000; end address
00010001;
00001111; data
00010001
00010001
.
.
00000000; null
00000000; start address segment 4
00101101;
00000000; end address
00101111;
00101101; data
00101110
00101111
01001101; postamble
```

Configuration Modes

This section gives setup requirements and usage guidelines for each configuration mode.

Mode 0: Configuration Reset

Configuration Data Source	Internal
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	None
Optional Dual-Function Pins	None

Mode 0 initiates the reboot sequence— it is equivalent to turning power to the device off and on again. Mode 0 overrides any other configuration sequences and cannot be stopped. In AT6000 devices, mode 0 is enabled by asserting $\overline{CS}$, $\overline{CON}$, M0, M1 and M2 low during the rising edge of CCLK. Reboot starts when the mode pins are released from mode 0 to any other mode. Because of this, the device should not be powered up in mode 0. One clock after entering mode 0, $\overline{CSOUT}$ tristates. Users who cascade devices and intend to use the mode 0 reboot function should insert logic to guarantee that the $\overline{CS}$ signal sent to the downstream cascaded device is driven low.

Mode 1: Address Count-Up, External CCLK

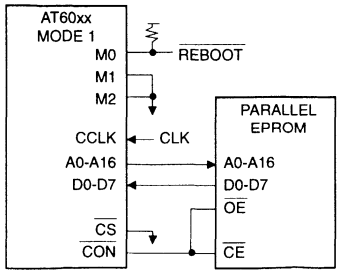
Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, CEN

Mode 1 (Figure 6) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 1, the external address counter starts at 00000 and counts up (see mode 2 description).

Using a maximum clock rate of 10 MHz, mode 1 can configure a single device in under 1 millisecond. Cascading devices limits the parallel data rate to 800 kHz.

Figure 6. Mode 1 Configuration



Mode 2: Address Count-Down, External CCLK

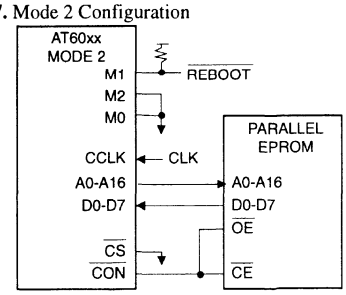
Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, CEN

Mode 2 (Figure 7) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user supplies a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

A typical microprocessor uses the highest or lowest address to load its own reboot address vector. If the FPGA is sharing a large EPROM with a microprocessor, the addresses used must start from the opposite end of the EPROM address map so that configuration does not interfere with the microprocessor, and vice versa. In mode 2, the external address counter starts at 1FFFF and counts down (see mode 1 description).

Using a maximum clock rate of 10 MHz, mode 2 can configure a single device in under one millisecond. Cascading devices limits the parallel data rate to 800 kHz.

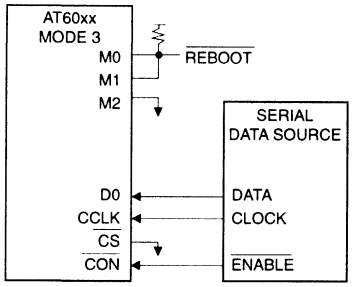
Figure 7. Mode 2 Configuration



Mode 3: Bit-Sequential, External CCLK

Configuration Data Source	Serial EPROM, Serial Comm. Port, UART, Download Cable
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Figure 8. Mode 3 Configuration



Mode 3 (Figure 8) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. The user must supply a configuration clock to CCLK. Configuration is initiated by driving $\overline{CON}$ low.

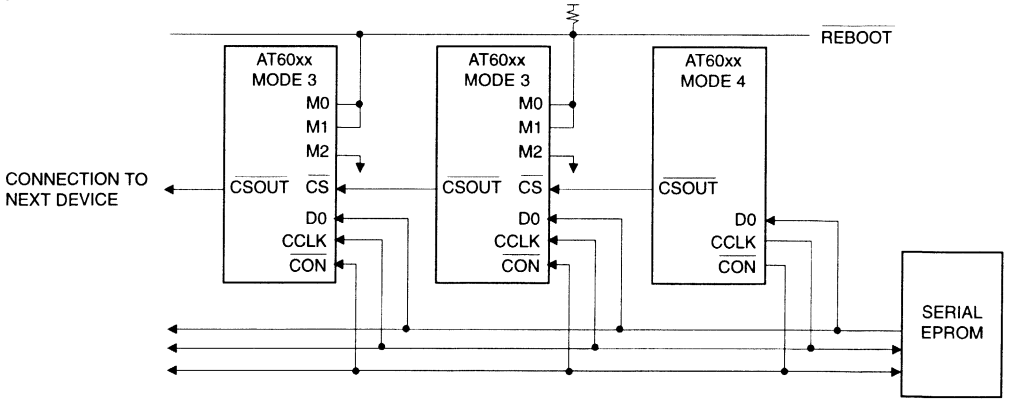
As long as data setup and hold requirements are satisfied, CCLK pulses can have arbitrary periods. This is helpful when using asynchronous communication ports or UARTs for configuration. If CCLK is stopped entirely between configurations, allow 24 preceding and trailing clock pulses with respect to $\overline{CON}$ going low or high (refer to the AC timing table in the AT6000 Series data sheet).

Depending on the speed of the user-supplied clock, mode 3 configuration can take as little as 8 milliseconds.

Mode 3 can be used to configure multiple devices cascaded together (Figure 9). The first device in the cascade chain must use either Mode 3 or Mode 4. If the configuration file contains a second preamble instead of a postamble (see the configuration-file format section), then the first device in the chain drives $\overline{CSOUT}$ low enabling the next device in the chain to receive configuration data from the serial data source. Configuration for downstream devices proceeds in a similar manner with "chip select" ($\overline{CS}$) propagating through the chain.

Mode 3 is used when configuring with the download cable provided in the Integrated Development System.

Figure 9. Mode 3 Cascade



Mode 4: Bit-Sequential, Internal CCLK E²PROM (AT17XXX)

Configuration Data Source	Serial E²PROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Mode 4 (Figure 10) asserts the $\overline{CON}$ pin low during the power-up boot sequence. $\overline{CON}$ is released for one CCLK period after initialization to reset the serial E²PROM. $\overline{CON}$ is then automatically re-asserted low and an internal oscillator toggles CCLK. This causes the E²PROM to begin downloading configuration data. One bit of data is loaded from the D0 pin on each rising edge of CCLK until configuration is complete. $\overline{CON}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the internal oscillator, but typically takes about 8 milliseconds.

The power supply ramp-up rate is critical in mode 4. The device generates a reset pulse 8 milliseconds after the supply voltage crosses the V_{TRIP} level (Figure 11). The supply voltage must be at the minimum for the serial E²PROM before the FPGA generates its reset pulse. Otherwise, the E²PROM's operation may be sporadic.

Mode 5: Address Count-Up, Internal CCLK

Configuration Data Source	Parallel EPROM
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7, A0-A16
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$, $\overline{CEN}$

Mode 5 (Figure 12) does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. Configuration is initiated by driving $\overline{CON}$ low. An internal oscillator toggles CCLK. This causes the FPGA to generate addresses A0-A16, beginning at 0, to read a configuration file from a parallel EPROM. One byte of configuration data is loaded from the D0-D7 pins on each rising edge of CCLK until configuration is complete. $\overline{CON}$ is then released, indicating the device is ready to use. Configuration time varies depending on the speed of the oscillator, but typically takes 8 milliseconds for the AT6005, and 16 milliseconds for the AT6002/3/10.

Only 13 address bits are required to fully program a single device; the four extra addresses allow multiple device configuration and let the device share memory space with other components of a system.

Figure 10. Mode 4 Configuration

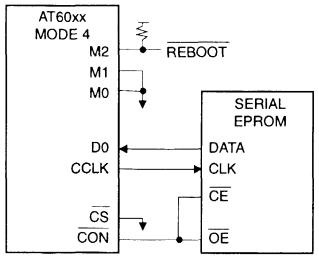


Figure 12. Mode 5 Configuration

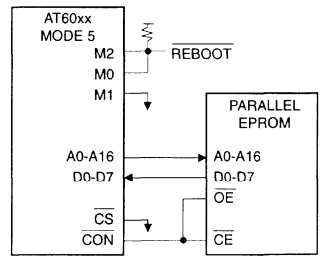
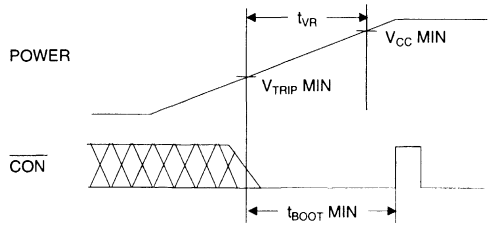


Figure 11. Power Supply Ramp-Up (Mode 4)



V_{CC} min	Minimum voltage for E²PROM operation
V_{TRIP} min	Minimum FPGA supply voltage to initiate reboot
t_{BOOT} min	Minimum reboot cycle time
t_{VR}	Minimum rise time of power supply from V_{TRIP} to V_{CC} min.

Mode 6: Byte-Sequential, External CCLK

Configuration Data Source	Parallel port of microprocessor
Dedicated Configuration Pins Used	$\overline{CON}$, $\overline{CS}$, M0, M1, M2, CCLK
Dual-Function Pins Used	D0-D7
Optional Dual-Function Pins	$\overline{ERR}$, $\overline{CHECK}$, $\overline{CSOUT}$

Figure 13. Mode 6 Configuration

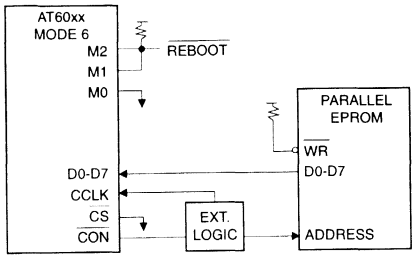


Figure 14. Mode 6 Cascade

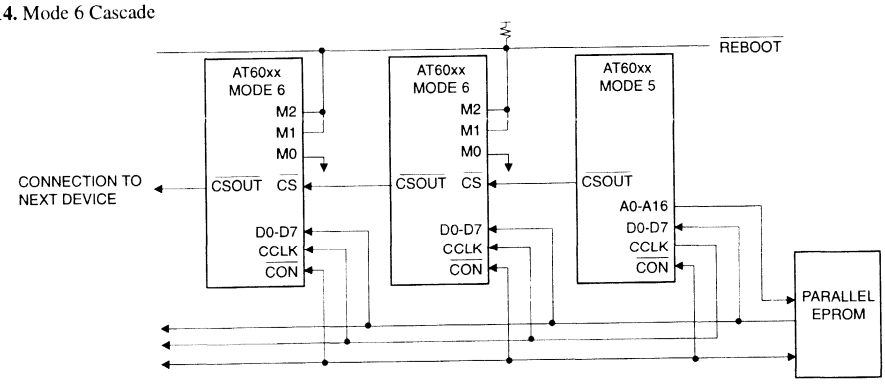
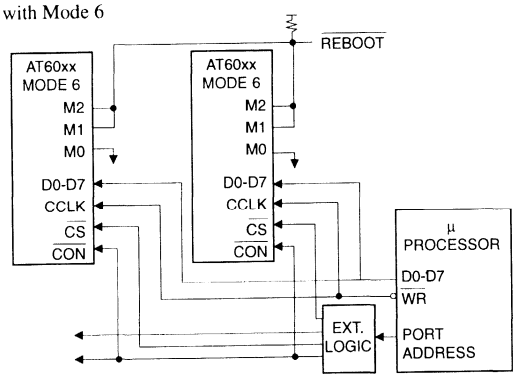


Figure 15. Parallel Configuration with Mode 6



Configuration Timing Parameters

These AC parameters are based on the timing diagrams that follow.

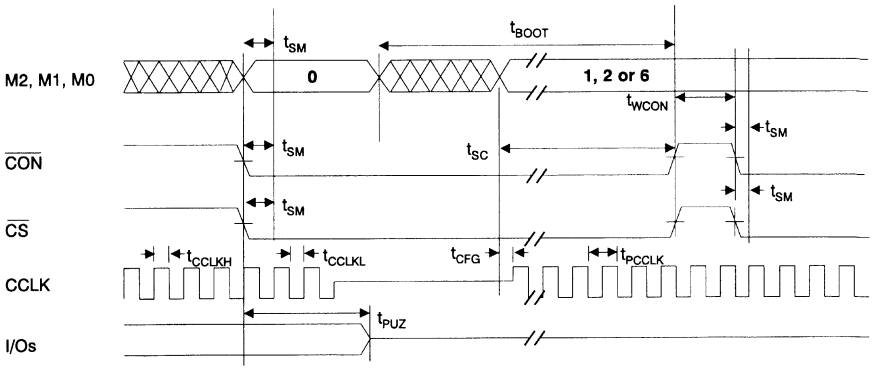
Parameter	Description		Min	Typ	Max	Units
t_{BOOT}	Delay from release of mode 0 or Power on (V_{CC} > Vsth min) to $\overline{CON}$ released.	AT6002/3: modes 1,2,3,5,6	1.3	2.7	5.4	ms
		AT6002/3/10: mode 4	8.1	16.3	32.6	ms
		AT6005: modes 1,2,3,4,5,6	4.4	8.8	17.6	ms
		AT6010: modes 1,2,3,5,6	0.05	0.1	0.2	ms
t_{WCON}	$\overline{CON}$ and $\overline{CS}$ high pulse width. Measured in CCLK clock cycles in modes 1, 2, 3 and 6.		2			cyc
t_{PCON}	$\overline{CON}$ high pulse width. Measured in CCLK clock cycles in modes 4 and 5.		2		2	cyc
t_{PUZ}	Delay from power-up or entry into mode 0 to user I/Os being tri-stated.			2000	4000	ns
t_{DERR}	Delay time from CCLK to change in $\overline{ERR}$. $\overline{ERR}$ will typically be high, and only go low if there is an error during confiugration or a mismatch during the check function.				30	ns
t_{SM}	Setup time from M0, M1, M2, $\overline{CS}$ and $\overline{CON}$ to rising edge of CCLK to initiate configuration or reboot.		30			ns
t_{HMP}	Hold time for $\overline{CS}$ and $\overline{CON}$ from rising edge of CCLK with preamble data present. Valid in modes 1, 2, 5 and 6.		2			cyc
t_{HMS}	Hold time for $\overline{CS}$ and $\overline{CON}$ from rising edge of CCLK with the least-significant-bit of the preamble present. Valid in modes 3 and 4.		17			cyc
t_{HCD}	Hold time for configuration data with respect to rising edge of CCLK.		5			ns
t_{SCD}	Setup time for configuration data with respect to rising edge of CCLK.		10			ns
t_{CFG}	Delay from rising edge of CCLK to change in I/O pin direction, as required when moving between the configuration and operation states.				50	ns
t_{DA}	Delay from CCLK rising edge to external address change.				35	ns
t_{CONH}	Delay from rising edge of CCLK to $\overline{CON}$ release. Delay measured with 2.7k pull-up resistor on $\overline{CON}$.				35	ns
t_{SC}	Setup time for M0, M1, M2 and CCLK to $\overline{CON}$ high.		10			cyc
V_{TRIP}	Supply voltage at which FPGA initiates reboot.		2.8		4.75	V
t_{CS}	Delay time from falling edge of CCLK to change in $\overline{CSOUT}$.				30	ns

Table 3. CCLK Parameters

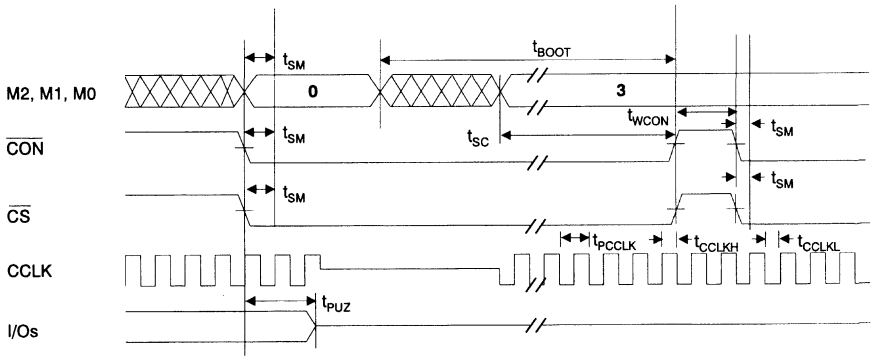
Mode(s)	Condition	t_{CCLKL} Min	t_{CCLKH} Min	t_{PCCLK} Min	t_{PCCLK} Typ	t_{PCCLK} Max
1, 2, 6	Without Cascade, without $\overline{\text{CHECK}}$	40 ns	40 ns	80 ns		
1, 2, 6	With Cascade, without $\overline{\text{CHECK}}$	150 ns	150 ns	1.25 µs		
1, 2, 6	Without Cascade, with $\overline{\text{CHECK}}$	200 ns	200 ns	500 ns		
1, 2, 6	With Cascade, with $\overline{\text{CHECK}}$	200 ns	200 ns	1.25 µs		
4, 5	CCLK is Output	240 ns	240 ns	500 ns	800 ns	1200 ns
3	Without $\overline{\text{CHECK}}$	40 ns	40 ns	80 ns		
3	With $\overline{\text{CHECK}}$	200 ns	200 ns	500 ns		

Reboot Cycle

Modes 1, 2 and 6

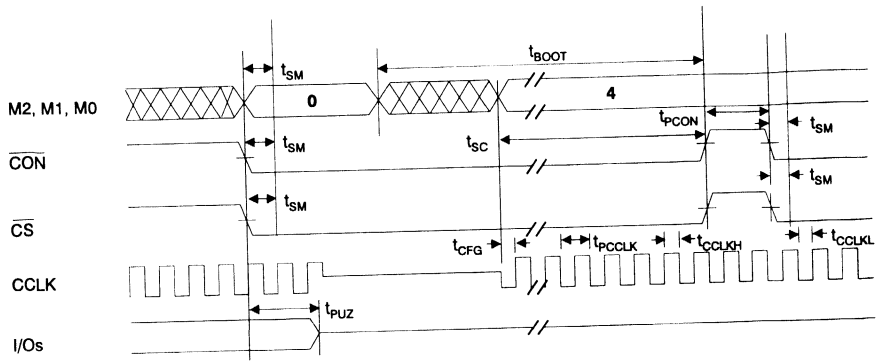


Mode 3

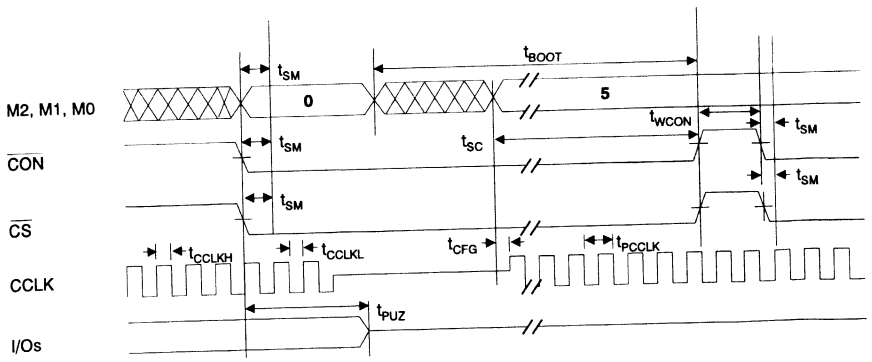


Reboot Cycle (Continued)

Mode 4

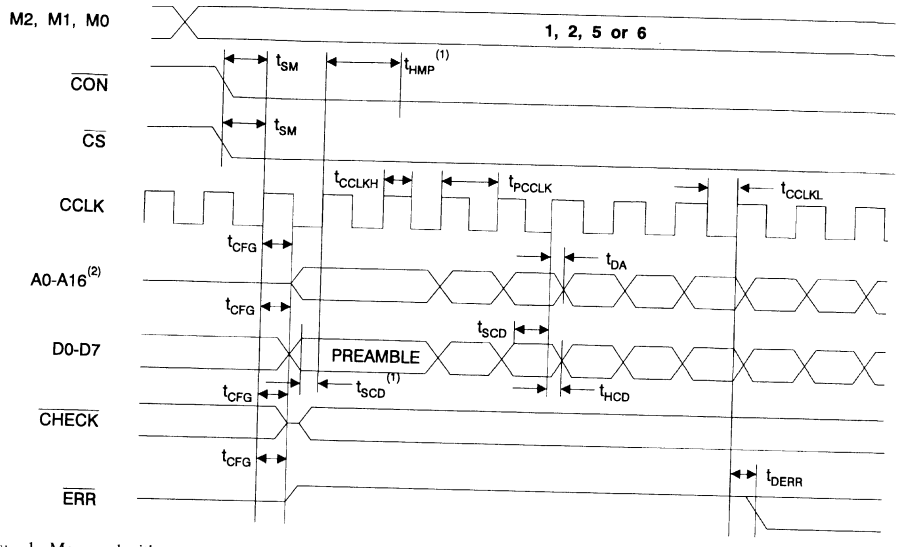


Mode 5



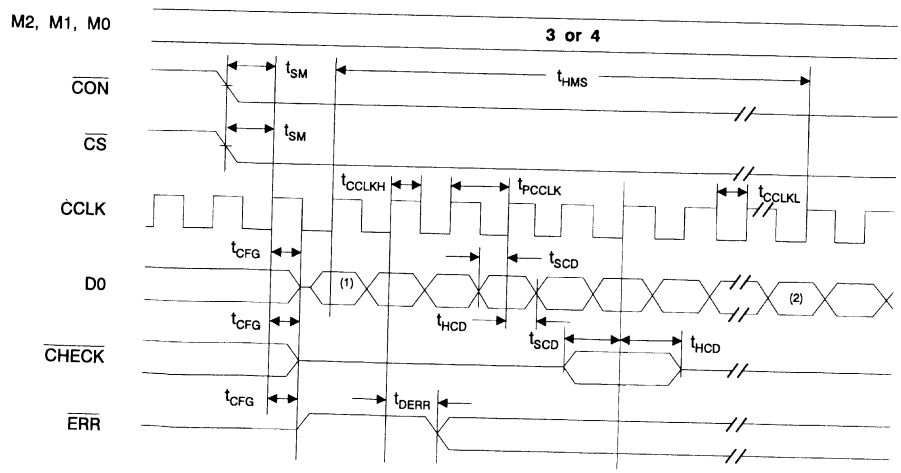
Beginning of Configuration

Modes 1, 2, 5 and 6



Notes: 1. Measured with respect to the edge of CCLK, which clocks in the preamble.
2. A0-A16 not used in mode 6.

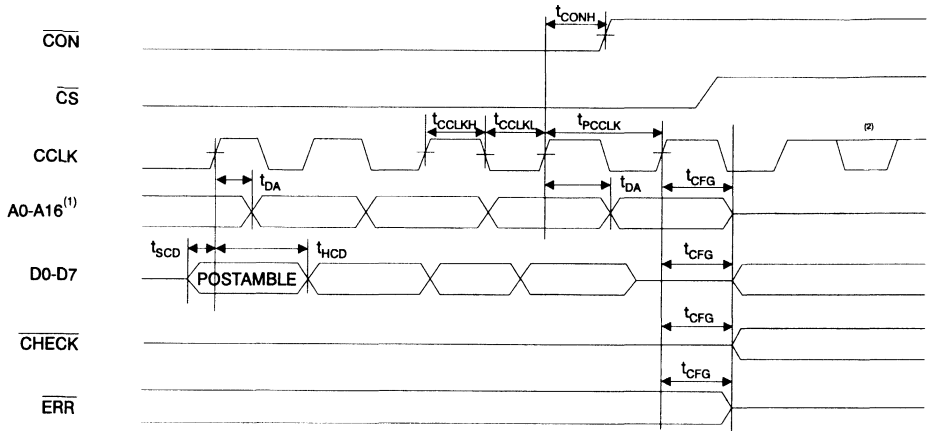
Modes 3 and 4



Note: 1. Preamble LSB.
2. Preamble MSB.

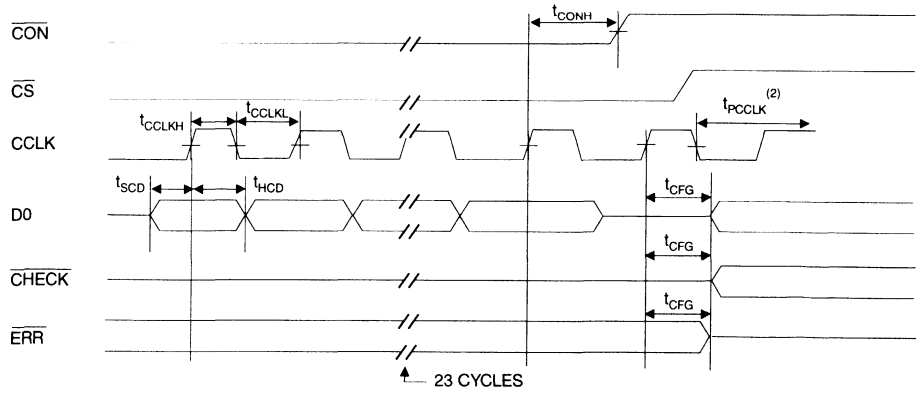
End of Configuration without Cascading

Modes 1, 2, 5 and 6



Note: 1. A0-A16 not used in mode 6.
2. CCLK remains high in mode 5.

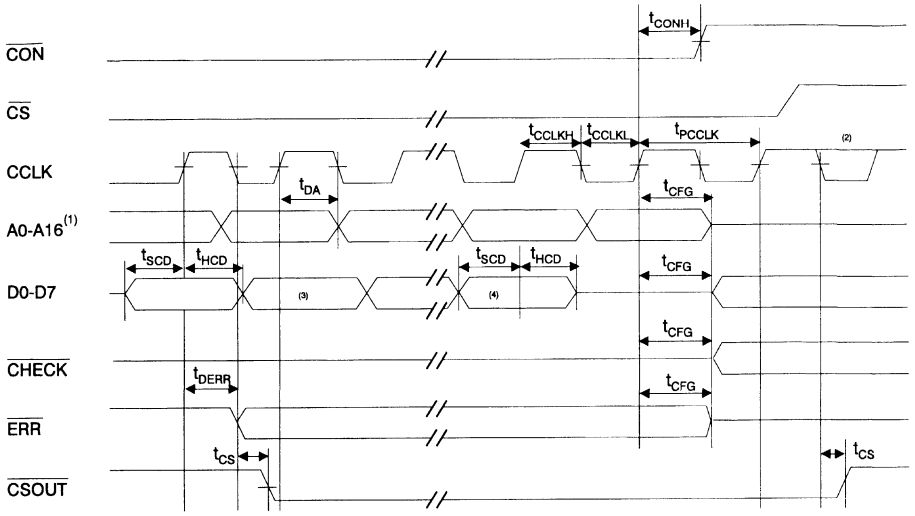
Modes 3 and 4



Note: 1. Postamble LSB.
2. CCLK remains high in mode 4.

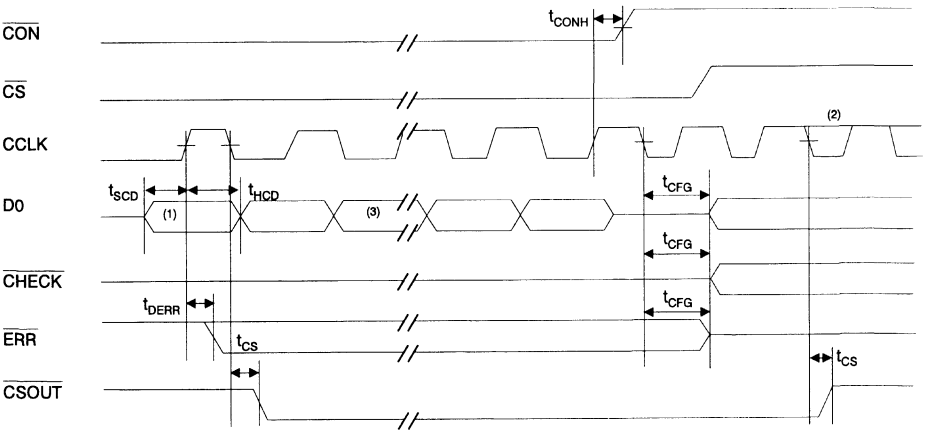
End of Configuration with Cascading

Modes 1, 2, 5 and 6



Note: 1. A0-A16 not used in mode 6.
2. CCLK remains high in mode 5.
3. End address of final window.
4. Postamble of final chip in cascade chain.

Modes 3 and 4



Note: 1. Preamble LSB.
2. CCLK remains high in mode 4.
3. Postamble of final chip in cascade chain.

Contents

Features

- **E^2 Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1 bit serial memories designed to store configuration programs for Programmable Gate Arrays**
- **Simple interface to SRAM FPGAs requires only one user I/O pin**
- **Compatible with AT6000 FPGAs, ATT3000 FPGA, XC2000, XC3000, XC4000 FPGAs**
- **Cascadable to support additional configurations or future higher-density arrays**
- **Low-power CMOS EEPROM process**
- **Programmable reset polarity**
- **Available in the space-efficient plastic DIP, or surface-mount PLCC and SOIC packages**
- **In-system programmable via 2-wire bus**
- **Emulation of 24CXXX Serial EPROMs**

FPGA Configuration E^2PROM

65K, 128K, and 256K

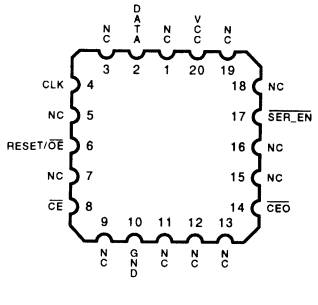
3

Description

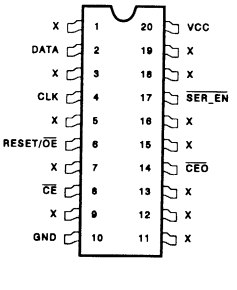
The AT17C65/128/256 (AT17CXX family) FPGA Configuration EEPROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Both the AT17C65 and the AT17C128 are packaged in the 8-pin DIP and the popular 20-pin Plastic Leaded Chip Carrier, and SOIC. The AT17C256 is available in 14-pin SOIC or 20-pin PLCC or SOIC packages. The AT17CXX family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17CXX organization supplies enough memory to configure one or multiple smaller FPGAs. Multiple configurations for a single FPGA can also be loaded from the AT17CXX family. Using a special feature of the AT17CXX, the user can select the polarity of the reset function by programming a special EEPROM bit.

The AT17C65/128/256 can be programmed with the standard programmers from other manufacturers.

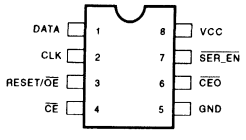
20-PIN PLCC



20-PIN SOIC



8-PIN DIP



0391B

Controlling The AT17C65/128/256 Serial EEPROMs

Most connections between the FPGA device and the Serial EEPROM are simple and self-explanatory:

- The DATA output of the AT17C65/128/256 drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17C65/128/256.
- The CEO output of any AT17C65/128/256 to drive the CE input of the next AT17C65/128/256 in a cascade chain of PROMs.
- Pin 7 must be connected to V_{CC}.

There are, however, two different ways to use the inputs CE and OE,as shown in the AC Characteristics Waveform.

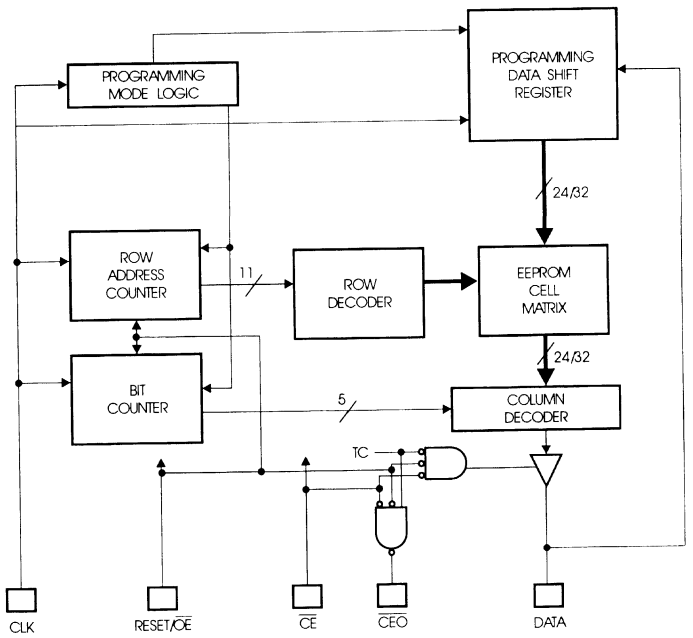
Condition 1

The FPGA D/$\overline{P}$ or LDC output drives both $\overline{CE}$ and $\overline{OE}$ in parallel. This is the simplest connection, but it fails when a user applies $\overline{RESET}$ during the FPGA configuration process. If $\overline{RESET}$ is applied, the FPGA aborts the original configuration and then restarts a new configuration, as intended. The problem is that the AT17C65/128/256 does not reset its address counter, since it never experiences a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length, count etc. Since the FPGA device is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}), and D/$\overline{P}$ goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA device and on its out pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Condition 2

The FPGA D/$\overline{P}$ or LDC output drives only the $\overline{CE}$ input of the AT17C65/128/256, while its $\overline{OE}$ input is driven by the inversion of the FPGA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. The High level on the $\overline{OE}$ input during $\overline{RESET}$ clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. Most designs have a spare inverter or inverting gate that can be used for this purpose. The AT17C65/128/256 does not require this inverter since the RESET polarity is programmable. AT17C65/128/256 that it is compatible with the FPGA device.

Block Diagram



Pin Configurations

PLCC/SOIC	DIP			
Pin	**Pin**	**Name**	**I/O**	**Description**
2	1	DATA	I/O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
6	3	RESET/$\overline{OE}$	I	Output Enable input. A Low level both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data ouput driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or OE/RESET. This document describes the pin as RESET/$\overline{OE}$..
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.
10	5	GND		Ground pin.
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
17	7	$\overline{SER\_EN}$	I	Serial enable normally high during FPGA loading operations. Bringing SER_EN low, enables the two wire serial interface mode for programming.
20	8	V_{CC}		+5 V power supply input

3

FPGA Master Serial Mode Summary

The I/O and logic functions of the FPGA and their associated interconnections, are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins.

In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1 V to V_{CC} +0.5 V
Supply Voltage (V_{CC})	-0.5 V to +7.0 V
Maximum Soldering Temp. (10 s @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100pF)	2000 V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Cascading Serial Configuration EEPROMs (AT17C128 and AT17C256)

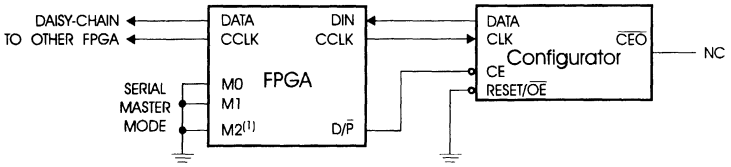
For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

After the last bit from the first Configurator is read, the next clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if $\overline{RESET}$ goes Low forcing the RESET/$\overline{OE}$ on each Configurator to go High.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground.

Address Counters Not Reset



Standby Mode

The AT17CXX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 0.5 mA of current. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ low. In this mode the chip can be programmed by a 2-wire interface. The programming is done at V_{CC} supply only. High voltages are generated inside the chip. See the Programming Specification for Atmel's Configuration Memories Application Note for further information.

AT17CXX Reset Polarity

The AT17CXX lets the user choose the reset polarity as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$.

Operating Conditions

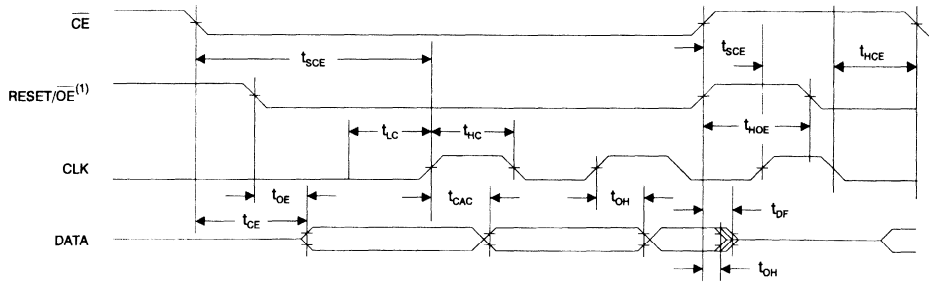
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to + 70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to + 85°C	4.5	5.5	V
	Military	Supply voltage relative to GND -55°C to 125°C	4.5	5.5	V

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (IOL = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_{CCS}	Supply current, standby mode			0.5	mA
I_L	Input or output leakage current		-10	10	µA

3

AC Characteristics Over Operating Conditions 1



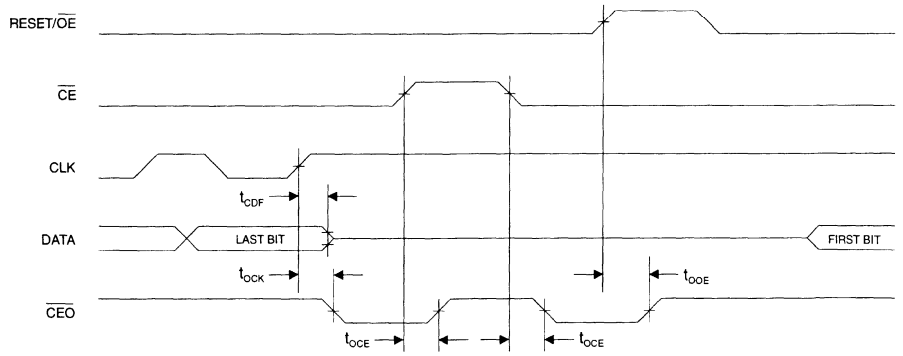
Note 1: CLK must be held low when RESET/$\overline{OE}$ is active

AC Characteristics Over Operating Conditions 1

Symbol		Description	Limits		Units
			Min	Max	
1	T_{OE}	$\overline{OE}$ to Data Delay		150	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		50	ns
3	T_{CAC}	CLK to Data Delay		50	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50	ns
6	T_{LC}	CLK Low Time	25		ns
7	T_{HC}	CLK High Time	25		ns
8	T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		ns
9	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)[4]	0		ns
10	T_{HOE}	$\overline{OE}$ High Time (Guarantees Counter Are Reset)	20		ns

Notes 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delay are measured with minimum tester ac load and maximum dc load.
4. With respect to falling edge of clock.

AC Characteristics Over Operating Conditions 2



AC Characteristics Over Operating Conditions 2

Symbol		Description	Limits		Units
			Min	Max	
1	T_{CDF}	CLK to Data Float Delay		50	ns
2	T_{OCK}	CLK to $\overline{CEO}$ Delay		55	ns
3	T_{OCE}	CE to $\overline{CEO}$ Delay		55	ns
4	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		55	ns

Ordering Information

Memory Size (K)	Ordering Code	Package	Operation Range
64K	AT17C65-10PC AT17C65-10JC AT17C65-10SC	8P3 20J 20S	Commercial (0°C to +70°C)
	AT17C65-10PI AT17C65-10JI AT17C65-10SI	8P3 20J 20S	Industrial (-40°C to +85°C)
128K	AT17C128-10PC AT17C128-10JC AT17C128-10SC	8P3 20J 20S	Commercial (0°C to +70°C)
	AT17C128-10PI AT17C128-10JI AT17C128-10SI	8P3 20J 20S	Industrial (-40°C to +85°C)
256K	AT17C256-10JC AT17C256-10SC	20J 20S	Commercial (0°C to +70°C)
	AT17C256-10JI AT17C256-10SI	20J 20S	Industrial (-40°C to +85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual InLine Package (PDIP)
20J	20 Lead, Plastic Leaded Chip Carrier (PLCC)
20S	20 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (SOIC)

Programming Specification for Atmel's Configuration Memories (AT17CXXX and AT34CXXX)

The Configurator

The Configurator is a serial memory which can be used not only as a serial memory but also can be used to load programmable devices. It can perform that latter action either as a slave, in which it responds to demands from the programmable logic and the address is implied, or as a master in which it autonomously loads the programmable logic. Its behavior is controlled by a program which is stored, interleaved with the data it contains, within the EEPROM memory. This memory can be read from or written to while the Configurator is in the system. The Configurator can also be programmed before it is inserted into the system. This document describes only the features needed to program the Configurator before it is placed in the system.

Configurator Versions

The Configurator comes in two versions: the AT17CXXX, and the AT34CXXX (generically referred to as "the device" in this document). There is only one difference in the programming specification for these two devices. The AT17CXXX has an additional step, to set the default reset polarity in the user mode.The programming algorithm is independent of the package; only 8 pins are used in either package for programming. The pins not used in the 20 pin version are set to zero.

Serial Bus Overview

The serial bus is a two wire bus; one wire (CLOCK) functions as a clock and is provided by the programmer, the second wire (DATA) is a bi-directional signal and is used to provide data and control information.

Information is transmitted on the serial bus in messages. Each MESSAGE is preceded by a START BIT and is ended with a STOP BIT. The message consists of an integer number of bytes, each byte consists of 8 bits of data and is followed by a ninth ACKNOWLEDGE BIT. This ACKNOWLEDGE BIT is provided by the recipient of the data. This is possible because devices only drive the CLOCK and DATA low, the system (in the programming case the Programmer) provides a small pull-up current (3k Ohm equivalent).

The MESSAGE FORMAT consists of the bytes shown in the Message Bytes table below. The MESSAGE FORMAT is preceded by a start bit and ended by a stop bit. The complete MESSAGE FORMAT is shown in the Message Format table below.

Message Bytes

DEVICE ADDRESS	1ST ADDRESS WORD	2ND ADDRESS WORD	DATA BYTE(S)

Message Format

START BIT	DEVICE ADDRESS	1ST ADDRESS WORD	1ST ADDRESS WORD	DATA BYTE(S)	STOP BIT

0437A

Serial Bus Overview (Continued)

The programmer provides all the bytes except for the data bytes when the device is being read. Note that each byte is individually acknowledged. This acknowledgment is provided by the Configurator in all cases except for the data bytes in the read mode, in which case the acknowledge is provided by the programmer.

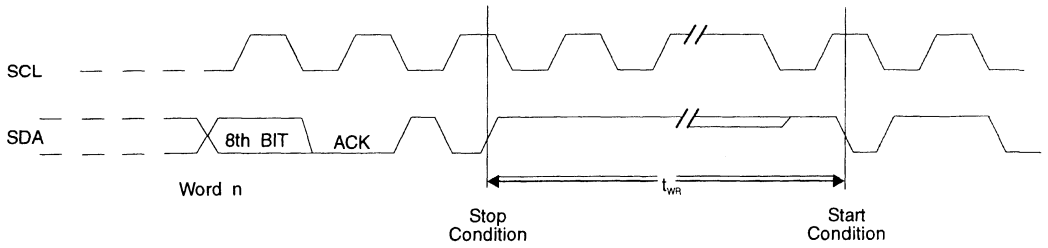
Bit Format

Data on the DATA pin may change only during CLOCK low times.

Start and Stop Bits

The START BIT is indicated by a high-to-low transition of DATA when CLOCK is high. Similarly, the STOP BIT is generated by a low-to-high transition of DATA when CLOCK is high, as shown below.

Start and Stop Bits



Acknowledge Bit

The ACKNOWLEDGE BIT is shown in the above figure. Note that the ACKNOWLEDGE BIT is provided by the device receiving the byte. The receiving device can accept the byte, by asserting a low value, on DATA or it can refuse the byte by asserting (not driving the signal) a 1 on DATA. All bytes must be terminated by either the ACKNOWLEDGE BIT or a STOP BIT.

Bit Ordering Protocol

The most significant bit is the first bit of a byte transmitted on DATA for the DEVICE ADDRESS BYTE and the EEPROM ADDRESS BYTES. It is followed by the lesser significant bits until the eighth bit, the least significant bit is transmitted. This is followed by the acknowledge bit. However, for DATA BYTES (both writing and reading) the first bit transmitted is the least significant bit. This protocol is shown in the tables below:

Device Address Byte

The contents of the Device Address Byte are shown below, along with the order in which the bits are clocked into the device. The A_2 bit is provided to allow 2 devices to share a common bus; when programming a single device, the A2 bit and the A_2 pin on the device will usually both be at 0v.

MSB							*LSB*
1	0	1	0	A_2	1	1	R/W#
1st	2nd	3rd	4th	5th	6th	7th	8th

Where:R/W#=1 Read
=0 Write

A2=1 if A2 pin is at VCC
=0 if A2 pin is at GROUND

EEPROM Address

The EEPROM address consists of two bytes, each of which is followed by an acknowledge bit. These two bytes define a 14 bit address A_{13}-A_0 where A_{13} is the most significant address bit.

The order in which each byte is clocked into the device is also indicated.

MSB							*LSB*		*MSB*							*LSB*	
0	0	A_{13}	A_{12}	A_{11}	A10	A_9	A_8	Ack	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Ack
1st	2nd	3rd	4th	5th	6th	7th	8th		1st	2nd	3rd	4th	5th	6th	7th	8th	

Data Byte

The organization of the Data Byte is shown below. Note that in this case, the data byte is clocked into the device LSB first and MSB last.

Writing

All writing takes place in pages. A page is 64 bytes long and the page boundaries are addresses where A5-0 are all zero. Writing can start at any address within a page and the number of bytes written is the number of data bytes transmitted and must be 64. The first byte is written at the transmitted address. The address is incremented in the device following the receipt of each data word received. Only the lower six bits of the address are incremented and the if the address is incremented after the 64th byte in the page is sent, then the next byte to be written is the first byte of the page.

LSB							*MSB*
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}	6^{th}	7^{th}	8^{th}

A write action consists of
a Start Bit
a Device Address with R/W# =0
An Acknowledge Bit From the device
First Word of the Address
An Acknowledge Bit From the device
Second Word of the Address
An Acknowledge Bit From the device
One or more data bytes
Each followed by an Acknowledge Bit From the device
a Stop bit

On receipt of the stop bit, the device enters an internally timed write cycle. While the device is busy with this write cycle it will not acknowledge any transfers. Thus the programmer can start the next page write by sending the Start Bit followed by the Device Address. If this is not acknowledged, then the programmer should abandon the transfer without asserting a stop bit. The programmer can then repeat this until an acknowledge is received. When this is received the write action can proceed i.e. the next byte to be sent is the device address.

Reading

Read operations are initiated the same way as write operations with the exception that the R/W# bit in the device address is set to one. There are three read operations: current address read, random read and sequential read.

A current address read action consists of
a Start Bit
a Device Address with R/W# =1
An Acknowledge Bit From the device
a data byte from the device
a stop bit from the programmer.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. If the last operation was a read at address n, then the current address would be n+1. If the final operation was a write at address n, then the current address would again be n+1 with one exception. If address 4 was the 64th byte address in the memory row, the incremented address n+1 would "roll over" to the 1st byte address in the page.

Once the device address with the R/W# select bit set is clocked in and acknowledged by the device the current address word is serially clocked out. The programmer does not acknowledge the read but does generate a following stop condition.

Random Read: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the device, the programmer must generate another start condition. The programmer now initiates a current address read by sending a device address with the R\W# bit high. The device acknowledges the device address and serially clocks out the data word. The programmer does not acknowledge the read but does generate a following stop condition.

A random address read action consists of
a Start Bit
a Device Address with R/W# =0
An Acknowledge Bit From the device
First Word of the Address
An Acknowledge Bit From the device
Second Word of the Address
An Acknowledge Bit From the device
a Start Bit
a Device Address with R/W# =1
An Acknowledge Bit From the device
a data byte from the device
a stop bit from the programmer.

Sequential Read: Sequential reads are initiated by either a current address read or a random address read. After the programmer receives a data word, it responds with an acknowledge. As long as the device receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the programmer does not respond with an acknowledge but generates a stop condition.

Programming Pins

Eight pins are used to program the devices. These eight pins, and their mapping to the package pins are shown in the following table.

Pin	8-Pin Device	20-Pin Device [1]
DATA	1	2
CLOCK	2	4
RESET/OE#	3	6
CE#	4	8
GROUND	5	10
A2 OR CEO#	6	14
SER_EN#	7	17
VCC	8	20

Note: 1. The unused pins in the 20-pin package must be grounded during programming.

Programmer Functions

The programmer needs to perform the following functions:

1. Check the Manufacturers Code and the Device Code
2. Program the device
3. Verify the device
4. AT17CXXX only:
5. Set the Reset Polarity option.

In the order given above. The are performed in the following manner.

Reading Manufacturers and Device Code

These two bytes are read from addresses 0 and 1 respectively with :

RESET/OE#=0V

CE#=11.5 ± 0.5ς

A2=(Same as applied to A2 Pin, usually 0v)

SER_EN#=0V

The correct codes are [1]

Manufacturers Code	-	Byte 0	1E	(Both devices)
Device Code	-	Byte 1	FF	AT17CXXX
			FE	AT34CXXX

Note: 1. The Manufacturer's Code and Device Code are read using the same byte ordering specified in the beginning of this document; i.e. LSB first, MSB last.

Programming the Device

All the bytes in the device's 64 byte page must be written. The order is not important but it is suggested that the device be written sequentially from Byte 0. Writing is accomplished by using the DATA and CLOCK pins and setting the other programming pins as follows:

RESET/OE#=0V

CE#=0V

A2=(Same as applied to A2 Pin, usually 0v)

SER_EN#=0V

Verifying the Device

All bytes in the device must be read and compared to their intended values. Reading is done using the CLOCK and DATA pins with the other programming pins set to the same value as in programming i.e.

RESET/OE#=0V

CE#=0V

A2=(Same as applied to A2 Pin, usually 0v)

SER_EN#=0V

AT17CXXX Only - Setting the Polarity Option

The AT17CXXX can has a programmable polarity on the
RESET/OE# pin. This has a default value of ACTIVE LOW but it can be changed during the programming. If a data file is used to program the AT17CXXX, the four bytes defining the polarity are stored at address 4000H in the file. If these bytes are:

FF FF FF FFRESET/OE# polarity must be set ACTIVE LOW as indicated below

00 00 00 00RESET/OE# polarity must be set ACTIVE HIGH as indicated below

Any other valueinvalid (no action need be taken)

Setting the Polarity Option Active Low:

Write a byte of data set to FF to address 3FFF, using CLOCK and DATA, with the other programming pins set to the following:

RESET/OE#=5±0.25ϖ

CE#=5±0.25ϖ

A2=(Same as applied to A2 Pin, usually 0v)

SER_EN#=0v

This will change RESET/OE# pin functionality to RESET#/OE.

Setting the Polarity Option Active High:

Write a byte of data set to FF to address 3FFF , using CLOCK and DATA, with the other programming pins set to the following:

RESET/OE#=0v

CE#=5±0.25 v

A2=(Same as applied to A2 Pin, usually 0v)

SER_EN#=0v

This will change RESET#/OE functionality to RESET/OE# (the default condition).

Using A Programmed Device as the Data Source

If a programmed (master) device is to be used as the source for the data to be programmed into some new devices, then the programmer can read the data from the master. This can be done without any difficulty for the AT34CXXX; however the polarity of the RESET/OE# must be known before this can be done successfully for the AT17CXXX. Depending on the capabilities of the programming device, one of the following algorithms can be used to read the data and polarity of the RESET/OE# pin.

1. If the programmer is able to sense s tri-state condition:

Switch the power on with

RESET/OE#=0V

CE#=0V

A2 (CEO#)=Input to programmer (High Z)

SER_EN#=5±0.25ς

CLOCK=0

DATA=Input to programmer

In this condition, if the SDA pin is tri-stated, then the RESET/OE# fuse is PROGRAMMED; if the SDA pin reads a "0" or a "1", then the RESET/OE# fuse is ERASED.

2. If the programmer is NOT able to sense a tri-state condition:

Switch the power on with

RESET/OE#=5±0.25ς

CE#=0V

A2 (CEO#)=Input to programmer

SER_EN#=5±0.25ς

CLOCK=0

DATA=Input to programmer

Hold this configuration for 10 seconds after Vcc reaches 5V. Then set RESET/OE# to low and pulse the clock 131,072 (128K) times reading the data provided at each clock pulse. After the last clock has been issued CEO# should drop from high to low. If it does so then the polarity is RESET/OE#. If CEO# remains high, then the polarity is RESET#/OE. In this latter case, none of the data read is reliable and it should be discarded. The procedure should be redone with RESET/OE# = 0V on power up and switched to 5±0.25V before starting the clock. The data read is now good data.

D.C. Characteristics

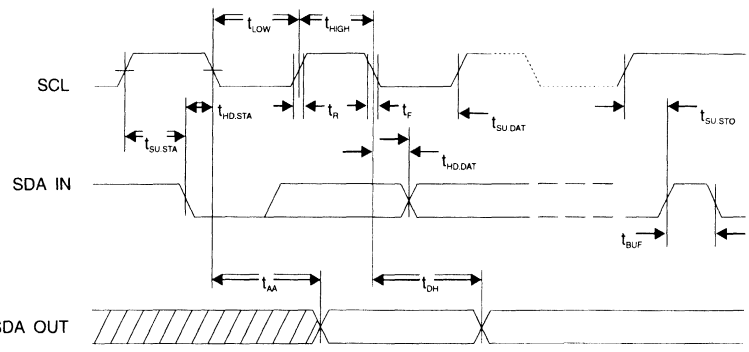
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	V_{CC} = 5V		2.0	3.0	mA
I_{LL}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	A
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	A
V_{IH}			V_{CC} x 0.7		V_{CC} ± 0.5	V
V_{IL}			-1.0		V_{CC} x 0.3	V

3

A.C. Characteristics

Symbol	Parameter	?		Units
		Min	Max	
f_{CLOCK}	Clock Frequency, Clock		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		s
t_{HIGH}	Clock Pulse Width High	0.6		s
t_{AA}	Clock Low to Data Out Valid	5		s
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		s
$t_{HD;STA}$	Start Hold Time	0.6		s
$t_{SU;STA}$	Start Set-Up Time	0.6		s
$t_{HD\ DAT}$	Data In Set-up Time	0		s
$t_{SU\ DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time		0.3	s
t_F	Inputs Fall Time		300	ns
$t_{SU\ STO}$	Stop Set-up Time	0.6		s
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		10	ns

Serial Data Timing Diagram



Contents

PLD Software Tools Overview

Atmel's philosophy is that you should be able to use standard tools you already have to design with our programmable logic devices. For those users that do not currently have such a tool, or who wish to augment tools they already own, we have Atmel-specific versions of standard tools available at very reasonable costs.

With the tools Atmel has available, we can serve the needs of beginning users as well as more experienced users. Based on the background of the user, we can make recommendations on the most cost effective solution (see Table 1). If you have any questions regarding which package is best suited to a particular set of needs, please contact the Atmel PLD Technical Support Hotline at (408) 436-4333.

General

Atmel offers versions of standard third-party PLD design tools that are limited to only Atmel PLD devices at a reduced cost compared to the normal versions. These systems are based on software licensed from Data I/O Corporation and Viewlogic Systems, Inc.

Under the terms of our agreements with Data I/O and Viewlogic Systems, Atmel may sell these systems and their options only to users of these limited systems. If a customer already has the full function version from Data I/O and/or Viewlogic Systems, they can purchase upgrades or options from the original company, not from Atmel.

This document outlines general system configurations required to use the various systems, details each package including ordering information, and includes a section with suggested systems for various types of users.

Required System Configurations

At the present time, all of the PLD systems described are available only on PC386/486 platforms running DOS with the system requirements indicated in Table 2. Contact the Atmel PLD Hotline at (408) 436-4333 for further information on system configurations

Systems

Atmel offers several levels of systems to meet the various needs of our customers. The systems are described on the following pages, along with a brief description of their function. For further information, contact your local Atmel sales representative or the Atmel PLD Hotline at (408) 436-4333.

Table 1. PLD Software System Recommendations

User	Experience	Recommended System
New PLD User	No prior PLD experience. Wants basic support for PAL-type and V-Series devices and is willing to do manual pin assignment.	Atmel-CUPL ATDS1200PC (Atmel-ABEL)
PAL-type Device User	Knows Abel, Cupl, or PALASM, and is familiar with 22V10 design. Wants to move up in density, and wants automatic fitting to reduce need to learn detailed internals of each device.	ATDS1210PC (Atmel-ABEL V-Series Kit)
Complex PLD User or TTL Designer	Uses complex PLDs from Altera, AMD, or Lattice. Wants state-of-the-art tools for Atmel's V-Series to take advantage of their speed and density. Wants schematic capture, simulation, and multiple design entry modes. Does not need full timing simulation	ATDS1303PC (Atmel-ProPLD 3K Gate System. Includes one year of maintenance)
	If timing simulation and higher gate capacity is needed ...	ATDS1320PC (Atmel-ProPLD 20K Gate System)
Viewlogic-based FPGA User	Uses FPGAs from Xilinx, Actel, or others with Viewlogic CAE tools for schematic capture and simulation. Wants to add capability for Atmel's V-Series to take advantage of their speed and density for control and timing applications, at minimum cost.	ATDS1303PCI (Atmel-ProPLD 3K System Intermediate Upgrade)
	If timing simulation and higher gate capacity is needed ...	ATDS1320PCI (Atmel-ProPLD 20K Gate System Intermediate Upgrade)

Table 2. PLD System Configuration Requirements

		Atmel-Abel	Atmel-ProPLD
Platform:		PC386/486	PC386/486
Operating System:		DOS 3.0 or greater [1]	Windows 3.1
Display Adaptor:		CGA, EGA, Hercules, VGA or SVGA	EGA, Hercules, VGA, or SVGA
System Memory:		4 Mbytes total	8 Mbytes total min. 16 Mbytes total recommended
Hard Disk:	Space required: Space Recommended:	5 Mbytes 20 Mbytes	22 Mbytes 40 Mbytes
I/O Ports required:		1 parallel	1 parallel 1 serial (for mouse)
Mouse:		not required	3-button mouse required

Note: 1. Atmel-Abel can be run under the Microsoft Windows Environment.

PLD Software Tools Product Description List

Atmel-ABEL

Ordering Code: ATDS1200PC

Basic ABEL support for Atmel PAL-type and V-Series devices. Does not include any automatic device fitters, which are optional and priced separately or available in packages called Atmel-ABEL Kits. Current users of Atmel-ABEL-4.0x do not get an automatic upgrade to this version.

Atmel-ABEL V-Series Fitters

Ordering Code: ATDS1205PC

Automatic ATV750/ATV2500, ATV750B/ATV2500B, and ATV5000/ATV5100 device fitters for Atmel-ABEL. Requires Atmel-ABEL version 4.2 or greater in order to run.

Atmel-ABEL V-Series Kit.....

Ordering Code: ATDS1210PC

A package consisting of Atmel-ABEL together with fitters for the ATV750/ATV2500, ATV750B/ATV2500B, and ATV5000/ATV5100. A complete development package for the PAL-type devices and the V-Series with fitters, that offers a savings to the user over the components purchased separately.

Atmel-ProPLD 20K Gate System .....

Ordering Code: ATDS1320PC

A complete stand-alone ProPLD system with all ABEL functions plus Viewlogic schematic capture, simulation (unit delay and timing) as well as modeling function plus utilities. Includes all fitters. Price includes one year of maintenance/updates. Maintenance is optional after the first year.

Atmel-ProPLD 3K Gate System

Ordering Code: ATDS1303PC

A complete stand-alone ProPLD system with all ABEL functions plus Viewlogic schematic capture, simulation (unit delay). Includes all fitters. Price includes one year of maintenance/updates. Maintenance is optional after the first year.

Atmel-ProPLD Maintenance

Ordering Code: ATDM1303PC (3K)-ATDM1320PC (20K)

One year of updates and maintenance for the ProPLD software. Maintenance for one year is included with the purchase of Atmel-ProPLD, and it is optional after the first year. Maintenance is not required for the purchase of an Atmel-ProPLD Intermediate Upgrade, but is available if the user wishes to purchase their updates from Atmel.

Atmel-ProPLD Intermediate Upgrade

Ordering Code: ATDS1303PCI (3K)ATDS1320PCI (20K)

A ProPLD system sold as an add-on for users with an existing vendor-specific (SDA) Viewlogic seat. Examples of SDA seats are Viewlogic front-end systems sold by Xilinx and Actel for use with their place-and-route tools. Adds Atmel PLDs to the system. Includes all Atmel-ABEL files and fitters plus access to the appropriate Viewlogic libraries. May not be sold to a user with a full Viewlogic seat purchased from Viewlogic. Those users must purchase ProPLD directly from Viewlogic.

Ordering Information

Ordering Code	Description
ATDS1200PC	Atmel-ABEL High-Level Design Tool for Atmel Programmable Logic Devices: PAL-type devices, ATV750, ATV750B, ATV2500, ATV2500B, ATV5000, and ATV5100
ATDS1205PC	Atmel-ABEL Custom Logic Fitter Package for V-Series CPLDs
ATDS1210PC	Atmel-ABEL Kit with all V-Series Fitters
ATDS1303PC	Atmel-ProPLD 3K Gate System with Functional Simulation for PCs (Includes One Year Maintenance)
ATDS1303PCI	Atmel-ProPLD 3K Gate Intermediate Upgrade System with Functional Simulation
ATDM1303PC	Atmel-ProPLD 3K Gate System Maintenance (One Year)
ATDS1320PC	Atmel-ProPLD 20K Gate System with Timing Simulation for PCs (Includes One Year Maintenance)
ATDS1320PCI	Atmel-ProPLD 20K Gate Intermediate Upgrade System with Timing Simulation
ATDM1320PC	Atmel-ProPLD 20K Gate System Maintenance (One Year)

Features

- **Supports Various Atmel Devices: 16V8, 20V8, 22V10, 750, 750B, 2500, 2500B**
- **Full CUPL Hardware Description Language Using "C"-like Syntax**
- **Design entry includes: Boolean Equations, State Machines, and Truth Tables.**
- **Macros allow library development, and macro reusability.**
- **Five-level logic minimization algorithm.**
- **Functional unit delay behavioral simulator.**
- **Menu driven operation.**

Atmel-CUPL High-Level Design Tool for Atmel Programmable Logic Devices:

PAL-type

ATV750/B

ATV2500/B

Description

Atmel-CUPL is an entry level PLD design system. It offers full design entry, simulation, and JEDEC file generation of Atmel PLDs. Atmel-CUPL offers the basic features of Logical Devices' CUPL PLD design environment. It is well suited for small PLD design and verification. The package is specifically designed to support development with Atmel Programmable Logic Devices. Atmel-CUPL supports: 16V8, 20V8, 22V10, 750, 750B, 1500, 2500, 2500B devices. Support for other manufacturer's PLDs can be added directly from Logical Devices.

Atmel-CUPL supports multiple design entry methods. State machine, truth tables and high level Boolean equation can be used. Atmel-CUPL also accepts inputs from schematic entry tools and other HDLs.

Multiple logic minimization algorithm are available. Different algorithms will provide different results for each design. Therefore, a user benefits from the availability of multiple algorithms.

A unit delay simulator allows quick design verification. Simulation is the simplest way of checking a design's functionality. An integrated simulator allows quick design iteration.

Once a design is completed, Atmel-CUPL generates standard JEDEC files. Device programming is done with these files.

System Requirements

- **386/486 based PC**
- **640 KB system memory, 1MB expanded memory**
- **3.6 MB hard disk space**
- **DOS 3.3 or higher**

0434A

Atmel-ABEL High-Level Design Tool for Atmel Programmable Logic Devices:

PAL-type

ATV750/B

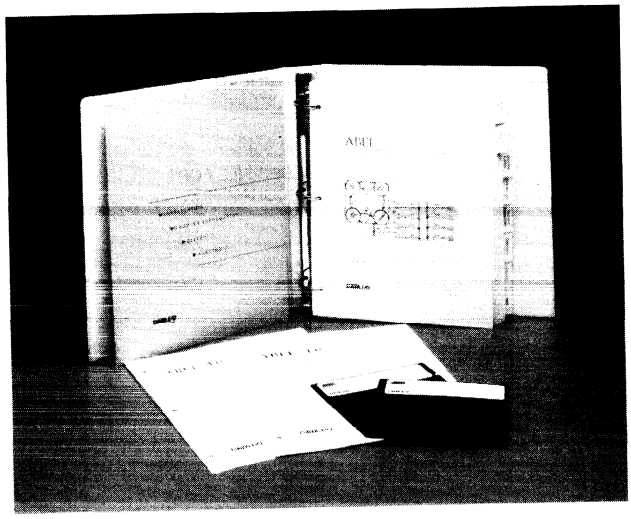
ATV2500/B

ATV5000

ATV5100

Features

- Atmel-ABEL Uses the Industry-Standard ABEL Hardware Description Language
- Multiple Input Methods :
  - Boolean Equations, Truth Tables and State Diagrams
  - Optional Schematic Entry Available
- Automatic Logic Reduction, Simulation, Error Checking, and Generation of Design Documentation
- Optional Device Fitters Perform Automatic Pin/Node Assignment and Logic Synthesis
- Automatically Takes Advantage of Atmel's PLD Architecture, Joining Sum Terms When Extra Product Terms are Needed
- Runs on MS-DOS™ Compatible Personal Computers
- This Inexpensive Package Includes:
  - Atmel-ABEL Software which Supports Atmel PAL-type Devices, ATV750, ATV750B, ATV2500, ATV2500B, ATV5000, and ATV5100
  - Complete ABEL Manual
  - Design Examples
- Upgradable to Full Version of ABEL Through Data I/O



Description

Atmel Programmable Logic Devices (PLDs) offer powerful solutions for logic design. Atmel-ABEL, developed by Data I/O Corporation, is a software package specifically designed to support development with Atmel Programmable Logic Devices.

Atmel-ABEL offers all of the function and features of Data I/O's standard ABEL software package while supporting Atmel's PLDs including all Atmel PAL-type devices as well as the ATV750, ATV750B, ATV2500, ATV2500B, ATV5000, and ATV5100. Support for other manufacturer's PLDs is not provided.

Atmel-ABEL automatically takes advantage of Atmel's innovative multiple sum term PLD architecture. When your reduced equations require more product terms than anticipated, the software automatically allocates the next available block of product terms to your equation.

(continued)

0430A

Description (Continued)

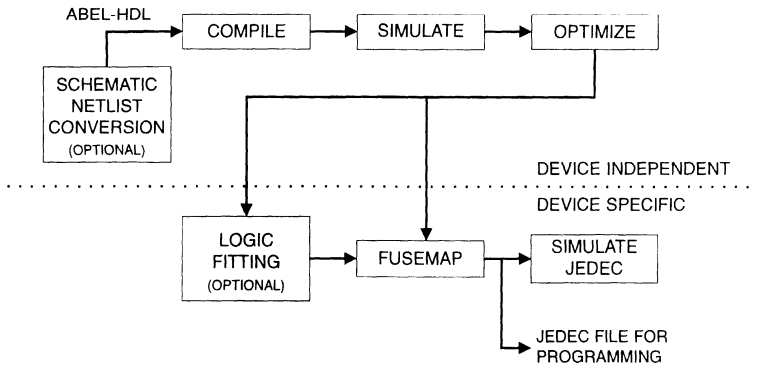
Atmel-ABEL automatically reduces your logic equations to near minimal form. Depending on your requirements, you can choose among several reduction algorithms. The result is a more efficient, cost-effective design.

Behavioral simulation is an integral part of the Atmel-ABEL design package. Simulation may be performed on either the design equations as entered, or after device selection, pin and node assignment, and option selection. This way you can verify that the completed design matches your design input.

Atmel-ABEL uses the Open ABEL format which allows the use of optional logic fitters. These logic fitters perform automatic device pin and node assignment and macrocell option selection to make maximum use of device resources, speeding up the design process.

Once your design is ready, Atmel-ABEL generates standard JEDEC files which can be downloaded to your programmer with the terminal emulation software included with the package.

Design Flow Diagram



General Support Requirements

- 386/486 Computer
- 3 1/2" 1.44 MB/HD Floppy Disk Drive
- DOS 3.0 or higher (can be run under Microsoft Windows Environment)
- 4 MB Total RAM

Ordering Information

Ordering Code	Description
ATDS1200PC	Atmel-ABEL High-Level Design Tool for Atmel Programmable Logic Devices: PAL-type Devices, ATV750/B, ATV2500/B, ATV5000, and ATV5100
ATDS1210PC	Atmel-ABEL Kit with all V-Series Fitters

Features

- **Works with Atmel-ABEL PLD Design System**
- **Allows Device-Independent Design**
- **Optimizes Resource Utilization**
- **Assigns Signals to Pins and Nodes**
- **Utilizes Atmel's Unique Product Term Joining/Sharing**
- **Performs Logic Synthesis**

Description

This custom logic fitter package for the Atmel-ABEL PLD design system supports all Atmel V-Series CPLDs. It was written by Data I/O with Atmel's cooperation and approval. This fitter package will work only with Atmel-ABEL, the special version of ABEL available from Atmel which supports Atmel's low and high density PLDs.

The fitters perform pin/node signal assignment, perform macrocell option selection, take advantage of Atmel's shared product term architecture where possible, and maximize resource utilization. This allows a user to do device-independent design and still get maximum utilization for Atmel's V-Series PLDs without needing to know all internal details of the devices.

Pin/node assignments may be made by the user, assigned by the fitter, or a combination of both. Optionally, all pin/node assignments can be ignored and the fitter will attempt to fit the design into the target device automatically.

Requirements

- The V-Series fitters require Atmel-ABEL version 4.2 or higher running under MS-DOS, version 3.00 or higher, with extended memory support (3 Mbyte minimum).

Atmel-ABEL V-Series Custom Logic Fitters:

ATV750

ATV750B

ATV2500

ATV2500B

ATV5000

ATV5100

4

Ordering Information

Ordering Code	Description
ATDS1205PC	Atmel-ABEL Custom Logic Fitter Package for V-Series CPLDs

ABEL™ and MS-DOS™ may be trademarks of others.

0431A

Atmel-ProPLD Integrated Programmable Logic Design System

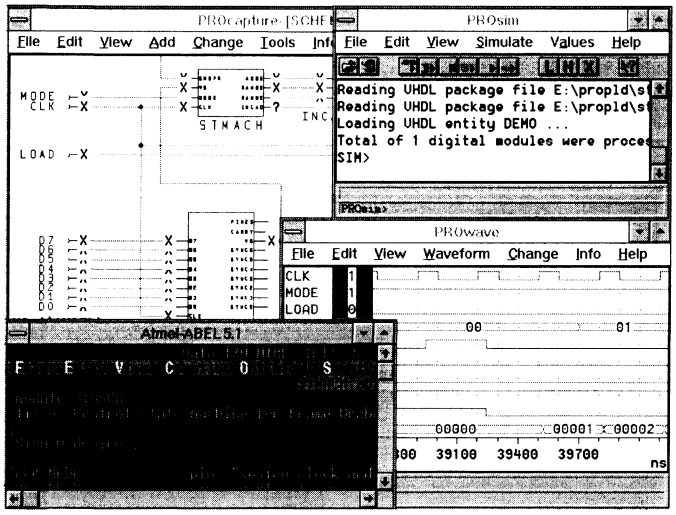
4

Reduce your time to market with the fastest, easiest to use, most complete set of tools for programmable logic design available: Atmel-ProPLD.
This fully integrated system supports Atmel's PLD devices and V-Series of complex PLDs.

Benefits

- **Allows design specification with schematic entry or the Abel hardware description language and accepts existing designs with JEDEC files and TTL logic in any arbitrary design hierarchy.**
- **Allows the retargeting of older designs into new technologies, and new functions can be easily merged and enhanced.**
- **Utilizes intelligent device fitters for automatic logic synthesis and device resource assignment.**
- **Saves design iterations by generating full VHDL timing models for simulating and debugging PLD designs in the system context.**
- **Optimizes designs requiring multiple devices with automatic user-guided partitioning and device fitting.**
- **Can combine multiple PLDs into larger CPLDs**
- **Runs under Microsoft Windows™ 3.1**

ProPLD Sample Screen



Atmel-ProPLD is a Complete Set of Tools for Programmable Logic Design

Through a partnership with Data I/O and Viewlogic Systems, Atmel has developed Atmel-ProPLD, bringing together the best programmable device knowledge and fitting capabilities with the best engineering environment for schematic entry and verification. Atmel-ProPLD is a complete set of tools for PLD design which will get you from concept to finished product faster than you ever thought possible. Atmel-ProPLD contains every tool you will ever need, from schematic entry and device fitting to waveform analysis and full timing simulation.

Atmel-ProPLD is available either as an add-on product to users with other vendor-specific Viewlogic front-end systems (intermediate upgrade), or as a stand-alone product offering unmatched capabilities and value in PLD design.

0432A

ProPLD Works From Multiple Input Formats/Sources

All of Atmel-ProPLD's capabilities operate from a design database which is created from several sources which can be freely intermixed. The Abel language can be used to easily specify Boolean operations, truth tables, and state machines. Schematics can be created using basic logic functions or TTL macro functions, and existing PLD designs in JEDEC format can be used as well. Once the design database is created, Atmel-ProPLD can automatically produce a schematic of the design for use in system schematics for functional simulation before any implementation is started.

Design Flow

Figure 1 shows the basic design flow for Atmel-ProPLD. Abel source files can be processed directly using the basic technology supplied by Data I/O, or Viewlogic's ProCapture tool may be used to enter hierarchical designs. These designs may have blocks that originate as Abel files, JEDEC files, or schematic input using either logic primitives or any of the comprehensive set of TTL macro functions included with Atmel-ProPLD.

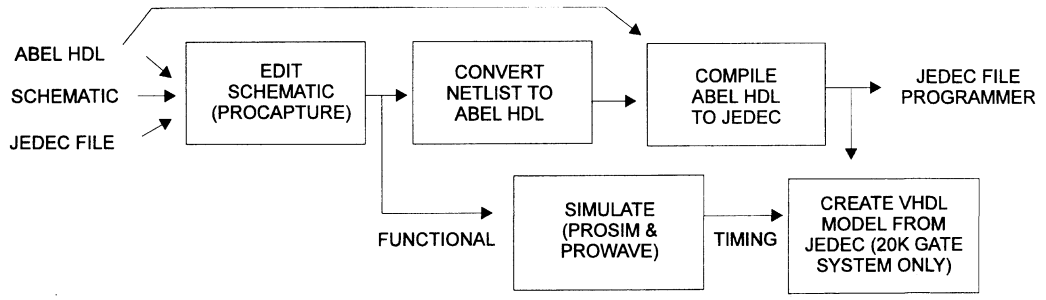
Comprehensive Device Support

Atmel-ProPLD offers complete support for Atmel's families of PLDs, including 16V8, 20V8, and 22V10 devices and the V-Series CPLDs. The V-Series CPLDs, designed for high density timing and control applications, includes the ATV750/L, ATV750B/BL, ATV2500H/L, ATV2500B/BL, ATV5000/L and ATV5100/L. For each PLD, Atmel-ProPLD automatically produces optimized JEDEC files that are ready to be downloaded to device programmers.

Although JEDEC file generation and timing modeling is limited to the Atmel devices, JEDEC file design input into the design database is accepted for most PLD devices supported by Abel, including all PAL and GAL devices.

Atmel-ProPLD includes device fitters for the V-Series CPLD devices. These fitters, developed by Data I/O with Atmel's support and cooperation, perform logic synthesis and device resource assignment automatically, allowing efficient designs to be created with minimum effort.

Figure 1. Atmel-ProPLD Design Flow Diagram



VHDL Models Automatically Generate Simulation Models

Once the design has been fitted into the PLD(s), Atmel-ProPLD generates simulation models for each PLD in VHDL for design verification. These models can be used with the automatically generated schematic interconnecting the PLD(s) to perform full timing simulation at the system level using ViewSim and ViewWave (Viewlogic's full function simulator and graphic waveform analyzer). ProSim and ProWave are included as a part of Atmel-ProPLD.

Functional VHDL models can also be produced for use in migrating a design to ASIC technology using the optional ProSynthesis and ProRetargeter tools.

Ordering Information

Ordering Code	Description
ATDS1303PC	Atmel-ProPLD 3K Gate System with Functional Simulation for PCs (Includes One Year Maintenance)
ATDS1303PCI	Atmel-ProPLD 3K Gate Intermediate Upgrade System with Functional Simulation
ATDM1303PC	Atmel-ProPLD 3K Gate System Maintenance (One Year)
ATDS1320PC	Atmel-ProPLD 20K Gate System with Timing Simulation for PCs (Includes One Year Maintenance)
ATDS1320PCI	Atmel-ProPLD 20K Gate Intermediate Upgrade System with Timing Simulation
ATDM1320PC	Atmel-ProPLD 20K Gate System Maintenance (One Year)

Software Support Information

	Software									
	Atmel ABEL	Atmel ViewPLD	Atmel CUPL	Data I/O ABEL	Logical Devices CUPL	Minc PLDesigner -XL	Viewlogic View-PLD	Viewlogic Power-View	Micro-Sim PLSyn	ISDATA LOG/iC
22V10 [1]	4.4	4.42	4.4c	1.3	2.0	3.0	1.2	5.2	6.0a	2.3
ATF16V8B	4.41	4.42	4.4c	2.0	2.0	3.0	1.2	5.2	6.0a	2.3
ATF20V8B	4.41	4.42	4.4c	2.0	2.0	3.0	1.2	5.2	6.0a	2.3
ATV750B	4.41	4.42	4.4c	5.1	4.4c	3.2	—	5.2	6.0a	4.0
ATV2500B	4.42	4.42	4.4c	5.1	4.4c	3.2	—	5.2	6.0a	4.0
ATV750	4.2	4.2	4.4c	3.0	2.15b	3.0	1.2	5.2	6.0a	3.0
ATV2500	4.2	4.2	4.4c	3.2	3.2A	3.0	1.2	5.2	6.0a	3.4
ATV5000	4.2	4.2	(4)	4.02	4.3	3.3	1.2	5.2	6.0a	(3)
ATV5100	4.2	4.2	(4)	4.3	(2)	(2)	1.2	5.2	6.0a	(2)

Notes: 1. Includes AT22V10, AT22V10B, AT22LV10, ATF22V10B.
2. Call PLD software vendor for more information.
3. Qualification in progress. Please call Atmel for update information.
4. Contact Logical Devices for support.

PLD Software Companies

Cadence Design Systems
555 River Oaks Parkway
San Jose, CA 95134
(408) 943-1234

Data I/O Corporation (ABEL™)
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 426-1045

ISDATA Gmbh (LOG/iC)
Daimlerstr 51
W-7500 Karlsruhe 21
Germany
US: (510) 531-8553

Logical Devices (CUPL™)
130 Capital Drive
Suite A
Golden, CO 80401
(800) 315-7766
(303) 279-6868

Mentor Graphics Corporation
8005 S.W. Boeckman Rd.
Wilsonville, OR 97070-7777
(503) 685-7000

Minc, Inc.
6755 Earl Drive
Colorado Springs, CO 80918
(719) 590-1155

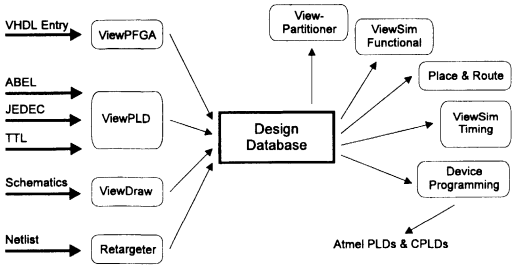
Viewlogic Systems, Inc.
293 Boston Road West
Marlboro, MA 01752
(508) 480-0881

MicroSim Corp.
20 Fairbanks
Irvine, CA 92718
(714) 770-3022

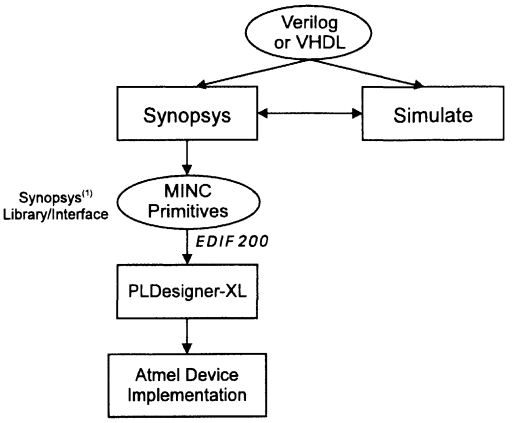
0433A

CAE Environments

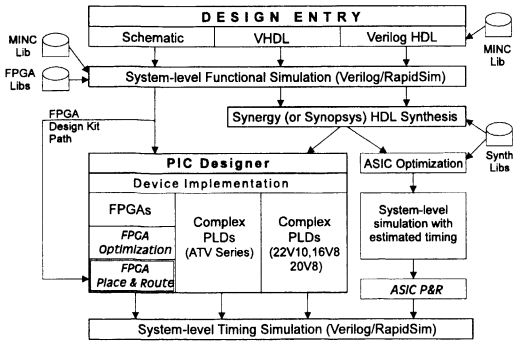
Viewlogic Environment



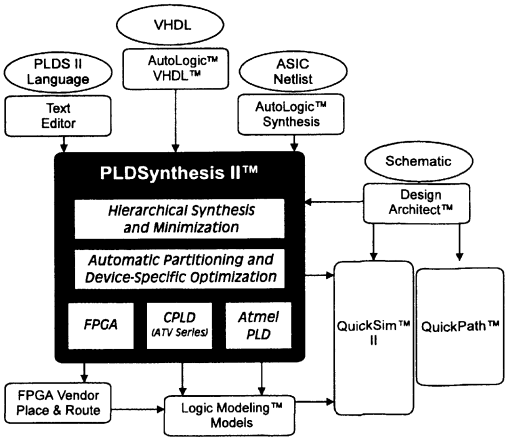
Synopsys Environment



Cadence Environment



Mentor Environment



New Programmer Support Information

The following is a partial listing of the ever-growing group of programmers that are evaluated and approved by Atmel.

A list of specific product and programmer firmware/software revisions that support each product is published periodically by Atmel and is also available from the Atmel BBS (408) 436-4309.

Information regarding specific product support information may be obtainable through your local Atmel representative or directly from the programmer vendors.

Company	Model			
Advantech Instruments	PC-UPROG	LABTOOL-48		
Advin Systems	Sailor-PAL	Pilot-U40	Pilot-U84	Pilot-U32
BP Microsystems	PLD1100	BP-1200	CP-1128	PLD1128
CEIBO	MP-51			
Data I/O	Unisite 48	3900/ Autosite	2900	
Hi-Lo System/ TRIBAL Microsystems	All-03A/ TUP400	All-07/ Flex700		
Logical Devices	AllPro40	AllPro88	AllPro88-XR	
Microprоss	ROM 3000U			
Needham Elec.	EMP20			
SMS	Sprint Plus	Sprint Expert		
Stag	ZL30A	ZL30B		
System General	TURPRO-1	TURPRO-1/FX		
XELTEK	SUPERPRO II			

4

Programming Hardware Companies

Advantech Instruments
Fl. 4, No. 108-3, Ming Chuan Rd.
Shing-Tien City, Taipei, Taiwan
886-2-218-4567
US: (408)245-6678

Advin Systems, Inc.
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 243-7000

BP Microsystems
1000 N. Post Oak Road
Suite 225
Houston, TX 77055
(713) 688-4600

CEIBO
Merkazim Building
1 Maskit Street
P.O. Box 2106
Herzelia 46120
Israel
(972) 52-555387
US: (617) 863-9927

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(206) 881-6444
(800) 247-5700

HI-LO System/TRIBAL Microsystems
44388 Grimmer Blvd.
Fremont, CA 94538
(510) 623-8859

Logical Devices
130 Capital Dr.
Suite A
Golden, CO 80401
(800) 315-7766
(303) 279-6868

Microprocess
5 Rue Denis Papin
59650 Villeneuve D'Ascq
France
(011) 33204-79040

Needham Electronics
4630 Beliot Dr., Suite #20
Sacramento, CA 95838
(916) 924-8037

SMS GmbH
Im Grund 15
D-88239 Wangen im Allgau
Germany: (07)522-9728-21
US: (800) 632-2776

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118
Europe: (44) 707-332148

System General
510 S. Park Victoria Drive
Milipitas, CA 95035
(408) 263-6667
Taiwan: (886) 2-9173005

XELTEK
757 North Pastoria Ave.
Sunnyvale, CA 94086
(408)524-1932

AT6000 FPGA Integrated Development System Overview

Features

- **Support for Industry Standard PC and Workstation CAE tools**
- **Combination Schematic, VHLD, PLD design entry**
- **Macro Library of Over 200 Hard/Soft Functions**
- **Automatic Macro Generators Generate Physical Layout**
- **Floor Planning Capability**
- **Automatic Place and Route**
- **Interactive Layout Editing**
- **Advanced Timing Analysis**
  - **100% logical path coverage**
  - **No user-vector generation**
  - **Displays set-up/hold violations & speed critical paths**
- **Full Back-Annotation for Functional & Timing Simulation**
- **Graphical User Interface**
- **Unified Design Database**

Description

Atmel's Integrated Development System lets designers create fast, predictable designs with AT6000 Series FPGAs.

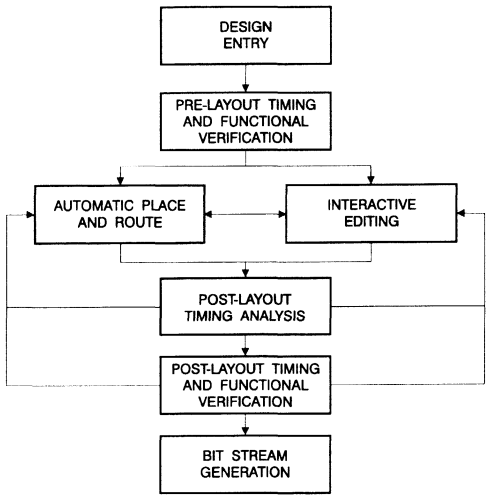
Available for use on 486/Pentium or Sun Sparc workstation-based computers, the Integrated Development System combines industry-standard software for design entry and simulation with Atmel's proprietary software for component generation, automatic and interactive placement and routing, timing analysis, and bit stream generation.

The Integrated Development System design flow is shown below. Pre-layout modules verify design logic, place and route modules implement the design, and post-layout modules reflect the design as it actually appears in silicon.

A Design Manager provides push-button access to each step in the flow. The Design Manager's simple user interface streamlines the design flow as it creates a seamless design environment. Design data is stored in a unified database that eliminates the need for data re-entry and translation.

The Integrated Development System Physical Design System includes a prototype kit and Viewlogic PRO Series (PC) or PowerView (Sun) macro libraries. Viewlogic timing and functional simulation is optional. Mentor, Verilog, Synopsys, Cadence, and Exemplar library/interface packages are also available.

Integrated Development System



0438A

AT6000 FPGA System Summary

The following is a summary of Integrated Development System software, hardware, and annual maintenance agreements. Detailed technical information is contained in the individual product data sheets.

Atmel offers specially-priced University systems for selected PC and Sun packages.

FPGA Physical Design System (ATDS2100PC/ATDS2100SN)

The AT6000 Physical Design System includes the Atmel Design Manager with PLD interface and macro libraries for Viewlogic schematic capture synthesis and functional simulation. Tools are included for macro generation, interactive editing, design rule checking, automatic placement and routing, timing analysis, bitstream generation, and PROM file generation.

Base PC and Sun system requirements for the Physical Design System are listed on the next page.

Physical Design System/Viewlogic standalone packages.

Several AT6000 Series design tool packages combine the Physical Design System with Viewlogic schematic capture and functional simulation options.

PC-based packages

Viewlogic's PRO series for the PC includes PROcapture (schematic entry), PROsim (gate simulation), and PROsynthesis (text-based entry).

Atmel offers the following PRO series packages:

- **ATDS2101PC.** AT6000 Series Physical Design System with PROcapture Schematic Entry
- **ATDS2110PC.** AT6000 Series Physical Design System with PROcapture and PROSim Gate Simulation (10K gates)
- **ATDS2120PC**. AT6000 Series Physical Design System with PROcapture and PROSim Gate Simulation (20K gates)

Customers with Viewlogic restricted licenses may purchase an Atmel 10K or 20K AT6000 Series Design System & Viewlogic restricted license upgrade.

A University system without a prototype kit is available for the ATDS2100PC and ATDS2110PC.

- **ATDS2130PC**. Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface for AT6000 Series Design System

Sun-based packages

Viewlogic's design tool family for Sun workstations is called Powerview, and the schematic entry, gate simulation, and text-based entry options are called ViewDraw, ViewSim, and ViewSynthesis.

Atmel offers the following Powerview packages:

- **ATDS2120SN**. AT6000 Physical Design System with Powerview Schematic Entry and Viewlogic Simulator (20K gates)
- **ATDS2130SN**. Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 Series Design System

A University system is available for the ATDS2120SN.

Library and Interface packages

Atmel offers several library and interface packages for customers who wish to use the AT6000 Series Physical Design System with third-party software from other companies:

PC-based library/interface package

ATDS2140PC. Exemplar Library & Interface for AT6000 Series Design System

Sun-based library/interface packages

ATDS2140SN. Exemplar Library & Interface for AT6000 Series Design System

ATDS2150SN. Mentor Library & Interface for AT6000 Series Design System

ATDS2160SN. Synopsys Library & Interface for AT6000 Series Design System

ATDS2170SN. Cadence Verilog/Concept Library & Interface for AT6000 Series Design System

Annual Maintenance Agreements

Annual Maintenance Agreements are available for each package and option in the Integrated Development System. The first year of maintenance is included in the purchase price; renewal is optional. Maintenance Agreements give users direct access to Atmel's experienced technical support staff and cover software upgrades that keep engineers on the leading edge of Atmel's design tools. See the individual product data sheets for ordering and pricing information.

Extended maintenance agreements are not available for University systems.

Prototype Kit

A Prototyping Kit is included in all PC Physical Design System packages, except University systems. Additional Prototype Kits can be ordered separately. Each kit includes a cable for downloading configuration data to a device and an AT-style board for prototyping designs.

Atmel now offers both 84-pin and 132-pin download boards for use with the Prototype Kit or the designer's target system. The boards can be attached to a host PC running the AT6000 series software.

Automatic Macro Generators

The AT6000 Physical Design System includes an innovative tool that allows users to create from a large number of datapath functions (multipliers, adders, accumulators).

The user specifies the parameters and the software quickly generates a physical layout and schematic, and reports worst case speed, area, and power consumption. These functions are layout-independent and resusable.

System Requirements

PC-based systems:

- Fully Compatible486/Pentium-Based Computer
- MS-DOS version 5.0 or greater
- Windows version 3.1
- Minimum 30 MB fixed disk space (for base system)
- CD-ROM player
- VGA graphics board and monitor
- Windows-Compatible Mouse
- One parallel port
- 32 MB of RAM

Sun-based systems:

- Sun Sparc workstation runnung SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- Minimum 40 MB fixed disk space (for base system)
- CD-ROM player
- X-Windows or Open Windows support
- 32 MB of RAM

PC-based Tools

Ordering Code	Description
ATDS2100PC	AT6000 Series Physical Design System
ATDS2101PC	AT6000 Series Physical Design System with PROcapture Schematic Entry
ATDS2110PC	AT6000 Series Physical Design System with PROcapture and PROSim Gate Simulation (10K)
ATDS2110PCI	AT6000 Series Design System & Viewlogic restricted license 10K upgrade
ATDS2120PC	AT6000 Physical Design System with PROcapture and ProSim (20K)
ATDS2120PCI	AT6000 Series Design System & Viewlogic restricted license 20K upgrade
ATDS2130PC	Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface for AT6000 Series Design System
ATDS2140PC	Exemplar Libraries & Interface for AT6000 Series Design System
Maintenance Agreements	
ATDM2100PC	Maintenance for AT6000 Series Physical Design System
ATDM2101PC	Maintenance for AT6000 Series Physical Design System with PROcapture
ATDM2110PC	Maintenance for AT6000 Series Physical Design System with PROcapture and PROSim (10K)
ATDM2110PCI	Maintenance for AT6000 Series Design System & Viewlogic restricted license 10K upgrade
ATDM2120PC	Maintenance for AT6000 Physical Design System with PROcapture and ProSim (20K)
ATDM2120PCI	Maintenance for AT6000 Series Design System & Viewlogic restricted license 20K upgrade
ATDM2130PC	Maintenance for Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface for AT6000 Series Design System
ATDM2140PC	Maintenance for Exemplar Library & Interface for AT6000 Series Design System
University PC-based Tools (do not include Prototyping Kit)	
ATDS2100PCU	University AT6000 Series Physical Design System
ATDS2110PCU	University AT6000 Series Physical Design System with PROcapture and ProSim (10K)
PC Design Hardware	
ATDH2000	AT6000 Series FPGAs Demonstration Board

Sun-based Tools

Ordering Code	Description
ATDS2100SN	AT6000 Series Physical Design System
ATDS2120SN	AT6000 Physical Design System with Powerview Schematic Entry and Viewlogic Simulator (20K)
ATDS2130SN	Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 Series Design System
ATDS2140SN	Exemplar Libraries & Interface for AT6000 Series Design System
ATDS2150SN	Mentor Libraries & Interface for AT6000 Series Design System
ATDS2160SN	Synopsys Libraries & Interface for AT6000 Series Design System
ATDS2170SN	Cadence Verilog/Concept Libraries & Interface for AT6000 Series Design System
Maintenance Agreements	
ATDM2100SN	Maintenance for AT6000 Series Physical Design System
ATDM2120SN	AT6000 Physical Design System with Powerview Schematic Entry and Viewlogic Simulator Maintenance for (20K)
ATDM2130SN	Maintenance for Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 Series Design System
ATDM2140SN	Maintenance for Exemplar Libraries & Interface for AT6000 Series Design System
ATDM2150SN	Maintenance for Mentor Libraries & Interface for AT6000 Series Design System
ATDM2160SN	Maintenance for Synopsys Libraries & Interface for AT6000 Series Design System
ATDM2170SN	Maintenance for Cadence Verilog/Concept Libraries & Interface for AT6000 Series Design System
University Sun-based Tools	
ATDS2100SNU	University AT6000 Series Physical Design System
ATDS2120SNU	University AT6000 Series Physical Design System with Powerview Schematic Entry and Viewlogic Simulator (20K)

Features

- Atmel Design Manager
- AT6000 Macro Libraries for PROcapture & PROsim
- AT6000 Macro Libraries for PROsynthesis
- Automatic Macro Generators
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Design Rule Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator and Utilities
- AT6000 Prototype Kit (not included in University system)

Applications Support

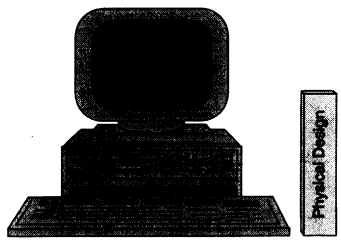
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

Base System Requirements

- Fully compatible 486/Pentium
- MS-DOS version 5.0 or greater
- Windows version 3.1
- Minimum 30 MB hard disk space
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM



ATDS2100PC
AT6000 Physical Design System

AT6000 FPGA Physical Design System (PC)

0439A

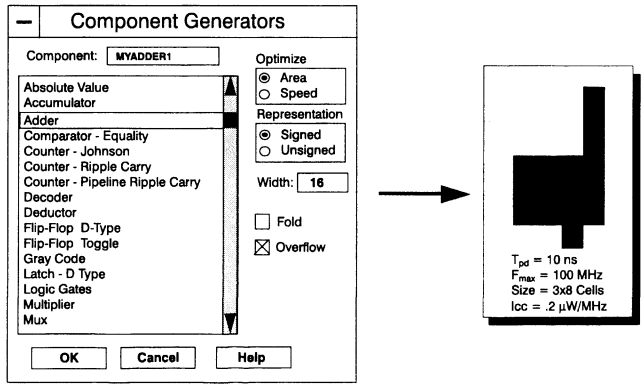
ATDS2100PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System	ATDS2100PC
Physical Design System Maintenance	ATDM2100PC
University Physical Design System (does not include Prototype Kit)	ATDS2100PCU
AT6000 Demonstration Board	ATDH2000PC
AT6000 Prototype Kit	ATDH2080PC

AT6000 Automatic Component Generators



AT6000 FPGA Physical Design System (PC) /w PROcapture Schematic Entry

Features

- Viewlogic PROcapture Schematic Entry
- Atmel Design Manager
- AT6000 Macro Libraries for PROcapture & PROsim
- AT6000 Macro Libraries for PROsynthesis
- Automatic Macro Generators
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Design Rule Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator and Utilities
- AT6000 Prototype Kit

Applications Support

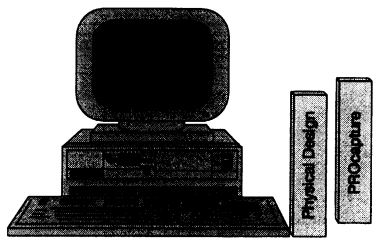
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Fully compatible 486/Pentium
- MS-DOS version 5.0 or greater
- Windows version 3.1
- 30 MB hard disk space for base system
- 25 MB hard disk space for Viewlogic
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM



ATDS2101PC
AT6000 Physical Design System
w/ PROcapture

0440A

ATDS2101PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System w/PROcapture	ATDS2101PC
Physical Design System w/PROcapture Maintenance	ATDM2101PC

AT6000 FPGA Physical Design System (PC) /w PROcapture Schematic Entry & PROsim Simulator (10K Gates)

Features

- Viewlogic PROcapture Schematic Entry
- Viewlogic PROsim Simulator (10K gates)
- Atmel Design Manager
- AT6000 Macro Libraries for PROcapture & PROsim
- AT6000 Macro Libraries for PROsynthesis
- Automatic Macro Generators
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Design Rule Checker
- Layout vs. Schematic Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator and Utilities
- AT6000 Prototype Kit (not included in University system)

Applications Support

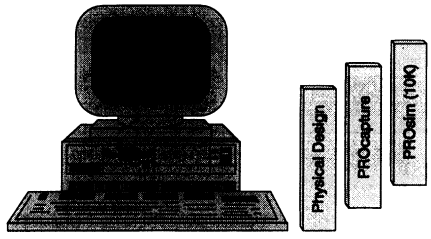
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Fully compatible 486/Pentium
- MS-DOS version 5.0 or greater
- Windows version 3.1
- 30 MB hard disk space for base system
- 25 MB hard disk space for Viewlogic
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM



ATDS2110PC
AT6000 Physical Design System
w/ PROcapture & PROsim (10K)

0441A

ATDS2110PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System w/PROcapture & PROsim (10K)	ATDS2110PC
Physical Design System w/PROcapture & PROsim (10K) Maintenance	ATDM2110PC
University Physical Design System w/PROcapture & PROsim (10K) (does not include Prototype Kit)	ATDS2110PCU
AT6000 Series Design System & Viewlogic restricted license upgrade	ATDS2110PCI
AT6000 Series Design System & Viewlogic restricted license upgrade Maintenance	ATDM2110PCI

AT6000 FPGA Physical Design System (PC) /w PROcapture Schematic Entry & PROsim Simulator (20K Gates)

Features

- Viewlogic PROcapture Schematic Entry
- Viewlogic PROsim Simulator (20K gates)
- Atmel Design Manager
- AT6000 Macro Libraries for PROcapture & PROsim
- AT6000 Macro Libraries for PROsynthesis
- Automatic Macro Generators
- Netlist Generator
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Pre-Layout Timing Estimator
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Timing to Layout Back Annotator
- Design Rule Checker
- Layout vs. Schematic Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator
- AT6000 Prototype Kit

Applications Support

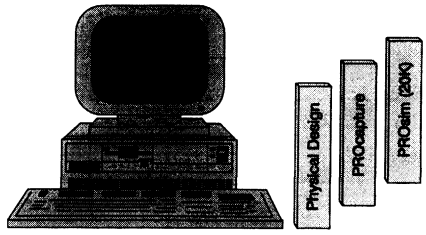
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Fully compatible 486/Pentium
- MS-DOS version 5.0 or greater
- Windows version 3.1
- 30 MB hard disk space for base system
- 25 MB hard disk space for Viewlogic
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM



ATDS2120PC
AT6000 Physical Design System
w/ PROcapture & PROsim (20K)

0442A

ATDS2120PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System w/PROcapture & PROsim (20K)	ATDS2120PC
Physical Design System w/PROcapture & PROsim (20K) Maintenance	ATDM2120PC
AT6000 Series Design System & Viewlogic restricted license upgrade	ATDS2120PCI
AT6000 Series Design System & Viewlogic restricted license upgrade Maintenance	ATDM2120PCI

Features

- AT6000 Synthesis Libraries for Viewlogic PROsynthesis
- Viewlogic PROsynthesis compiler
- Viewlogic PROsynthesis Interface to AT6000 Series Physical Design System

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

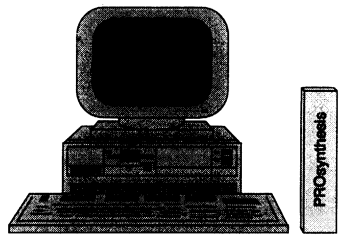
- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Fully compatible PC386/486/Pentium
- MS-DOS version 5.0 or greater
- Windows version 3.1
- 30 MB hard disk space for base system
- 15 MB hard disk space for Synthesis
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM

AT6000 FPGA Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface

4



ATDS2130PC
Viewlogic PROsynthesis,
PROsim/VDHL Libraries & Interface
for AT6000 FPGAs

0443A

ATDS2130PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface for AT6000 Series FPGAs	ATDS2130PC
Viewlogic PROsynthesis, PROsim-VDHL Libraries & Interface for AT6000 Series FPGAs Maintenance	ATDM2130PC

Features

- AT6000 Synthesis Libraries for Exemplar Design Compiler
- Exemplar Interface to AT6000 Series Physical Design System

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

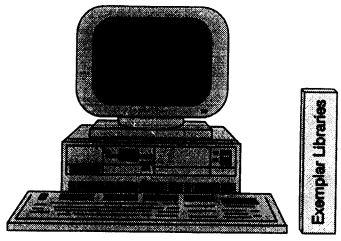
Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Fully compatible 486/Pentium
- MS-DOS version 5.0 or greater
- Windows 3.1
- 30 MB hard disk space for base system
- 2 MB hard disk space for Exemplar Libraries
- CD-ROM player
- VGA graphics board and monitor
- Windows compatible mouse
- One parallel port
- 32 MB of RAM

AT6000 FPGA Exemplar Synthesis Libraries & Interface



ATDS2140PC
Exemplar Synthesis Libraries
& Interface for AT6000 FPGAs

0444A

ATDS2140PC Features

PC-based Tools Feature	2100	2101	2110	2120	2130	2140
AT6000 FPGA Family Support	x	x	x	x	x	x
AT6000 Physical Design System	x	x	x	x		
Schematic Libraries & Interface	x	x	x	x		
Simulation Libraries & Interface	x	x	x	x	x	
Synthesis Libraries & Interface	x	x	x	x	x	x
Schematic Capture		x	x	x		
Synthesis Compiler					x	
Simulator (10K gates)			x			
Simulator (20K gates)				x		
Automatic Component Generators	x	x	x	x		
Prototype Kit	x	x	x	x		
Applications Hotline Support	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x

Ordering Information

Description	Part Number
Exemplar Libraries & Interface for AT6000 Series FPGAs	ATDS2140PC
Exemplar Libraries & Interface for AT6000 Series FPGAs Maintenance	ATDM2140PC

Features

- Atmel Design Manager
- AT6000 Macro Libraries for Powerview Schematic Entry and Simulation
- AT6000 Macro Libraries for ViewSynthesis
- Automatic Macro Generators
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Design Rule Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator and Utilities

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

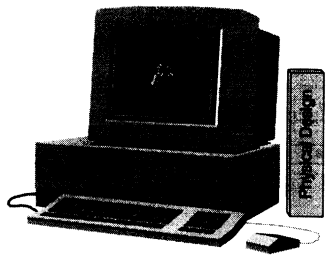
- Software Support and Updates for One Year included
- Extended Support is available

Base System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space
- 32 MB of RAM

AT6000 FPGA Physical Design System (Sun)

4



ATDS2100SN
AT6000 Physical Design System

0445A

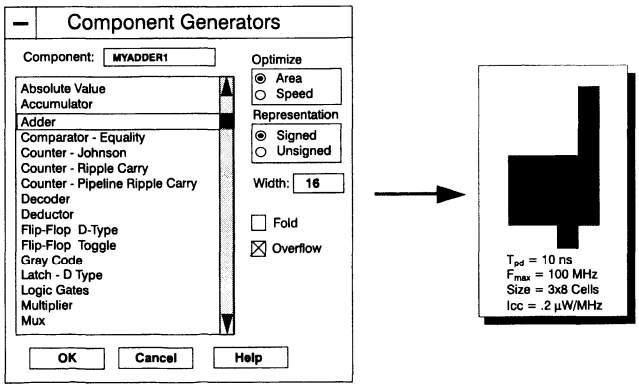
ATDS2100SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System	ATDS2100SN
Physical Design System Maintenance	ATDM2100SN
University Physical Design System	ATDS2100SNU

AT6000 Automatic Component Generators



AT6000 FPGA Physical Design System (Sun) /w Powerview Schematic Entry & Viewlogic Simulator (20K Gates)

Features

- Viewlogic ViewDraw Schematic Entry
- Viewlogic ViewSim (20K gates)
- Atmel Design Manager
- AT6000 Macro Libraries for Powerview Schematic Entry and Simulation
- AT6000 Macro Libraries for ViewSynthesis
- Automatic Macro Generators
- Automatic Place and Route
- Interactive Layout Editor (Floor Planning Tool)
- Static Timing Analyzer
- Post-Layout Timing Analyzer
- Timing to Simulation Back Annotator
- Design Rule Checker
- Plotting Utilities
- System Utilities
- Bit Stream Generator and Utilities

Applications Support

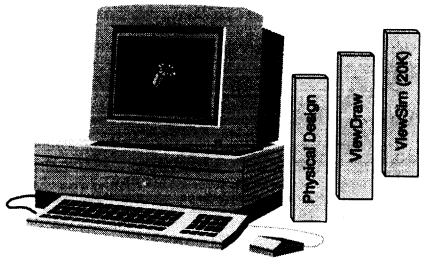
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 60 MB hard disk space for Viewlogic
- 120 MB of hard disk space for ViewDoc
- 32 MB of RAM



ATDS2120SN
AT6000 Physical Design System /w
Powerview Schematic Entry &
Viewlogic Simulator (20K Gates)

0446A

ATDS2120SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
AT6000 Series Physical Design System /w Powerview Schematic Entry & Viewlogic Simulator (20K)	ATDS2120SN
Physical Design System /w Powerview Schematic Entry & Viewlogic Simulator (20K) Maintenance	ATDM2120SN
University Physical Design System /w Powerview Schematic Entry & Viewlogic Simulator (20K)	ATDS2120SNU

Features

- AT6000 Synthesis Libraries for Viewlogic ViewSynthesis
- Viewlogic ViewSynthesis compiler
- Viewlogic ViewSynthesis Interface to AT6000 Series Physical Design System

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

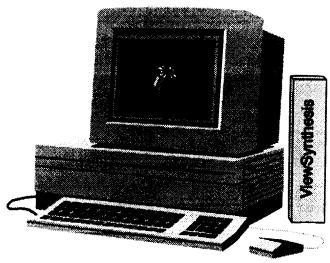
Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 60 MB hard disk space for Synthesis
- 32 MB of RAM

AT6000 FPGA Viewlogic ViewSynthesis, ViewSim-VDHL Libraries & Interface



ATDS2130SN
Physical Design System Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 FPGAs

0447A

ATDS2130SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 Series FPGAs	ATDS2130SN
Viewlogic Viewsynthesis, ViewSim-VDHL Libraries & Interface for AT6000 Series FPGAs Maintenance	ATDM2130SN

Features

- AT6000 Synthesis Libraries for Exemplar Design Compiler
- Exemplar Interface to AT6000 Series Physical Design System

Applications Support

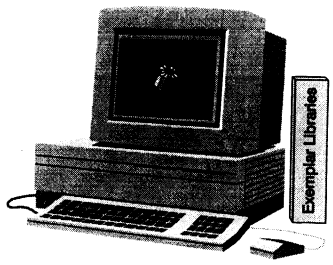
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 2 MB hard disk space for Exemplar Libraries
- 32 MB of RAM



ATDS2140SN
Exemplar Synthesis Libraries
& Interface for AT6000 FPGAs

AT6000 FPGA Exemplar Synthesis Libraries & Interface

4

0448A

ATDS2140SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
Exemplar Library & Interface for AT6000 Series FPGAs	ATDS2140SN
Exemplar Library & Interface for AT6000 Series FPGAs Maintenance	ATDM2140SN

Features

- AT6000 Schematic and Synthesis Libraries for Mentor Design Tools
- Mentor Interface to AT6000 Series Physical Design System

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

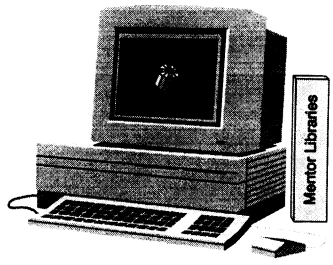
Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 9 MB hard disk space for Mentor Libraries
- 32 MB of RAM

AT6000 FPGA Mentor Libraries & Interface



ATDS2150SN
Mentor Libraries & Interface for AT6000 FPGAs

ATDS2150SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
Mentor Library & Interface for AT6000 Series FPGAs	ATDS2150SN
Mentor Library & Interface for AT6000 Series FPGAs Maintenance	ATDM2150SN

Features

- AT6000 Synthesis Libraries for Synopsys Design Compiler
- Synopsys Interface to AT6000 Series Physical Design System

Applications Support

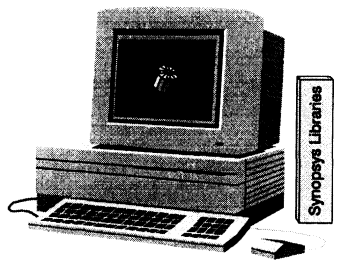
- FPGA Applications Hotline
- Access to Atmel Bulletin Board

Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 4 MB hard disk space for Synopsys Libraries
- 32 MB of RAM



ATDS2160SN
Synopsys Synthesis Libraries
& Interface for AT6000 FPGAs

AT6000 FPGA Synopsys Synthesis Libraries & Interface

0450A

ATDS2160SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
Synopsys Library & Interface for AT6000 Series FPGAs	ATDS2160SN
Synopsys Library & Interface for AT6000 Series FPGAs Maintenance (after first year)	ATDM2160SN

Features

- AT6000 Schematic and Synthesis Libraries for Cadence Design Tools
- Cadence Verilog/Concept Interface to AT6000 Series Physical Design System

Applications Support

- FPGA Applications Hotline
- Access to Atmel Bulletin Board

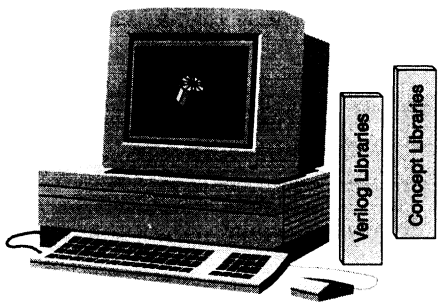
Maintenance

- Software Support and Updates for One Year included
- Extended Support is available

System Requirements

- Sun Sparc workstation running SUN OS 4.1.2 or greater
- Graphical monitor (color recommended)
- CD-ROM player
- X-Windows or Open Windows support
- 40 MB hard disk space for base system
- 4 MB hard disk space for Cadence Libraries
- 32 MB of RAM

AT6000 FPGA Cadence Synthesis Libraries & Interface



ATDS2170SN
Cadence Synthesis Libraries
& Interface for AT6000 FPGAs

0451A

ATDS2170SN Features

Sun Sparc-based Tools Feature	2100	2120	2130	2140	2150	2160	2170
AT6000 FPGA Family Support	x	x	x	x	x	x	x
AT6000 Physical Design System	x	x					
Schematic Libraries & Interface	x	x			x		x
Simulation Libraries & Interface	x	x	x		x		x
Synthesis Libraries & Interface	x	x	x	x	x	x	x
Schematic Capture		x					
Synthesis Compiler			x				
Simulator (20K gates)		x					
Automatic Component Generators	x	x					
Applications Hotline Support	x	x	x	x	x	x	x
Maintenance for 1 year	x	x	x	x	x	x	x

Ordering Information

Description	Part Number
Cadence Library & Interface for AT6000 Series FPGAs	ATDS2170SN
Cadence Library & Interface for AT6000 Series FPGAs Maintenance	ATDM2170SN

FPGA Integrated Development System Prototype Kit

Features

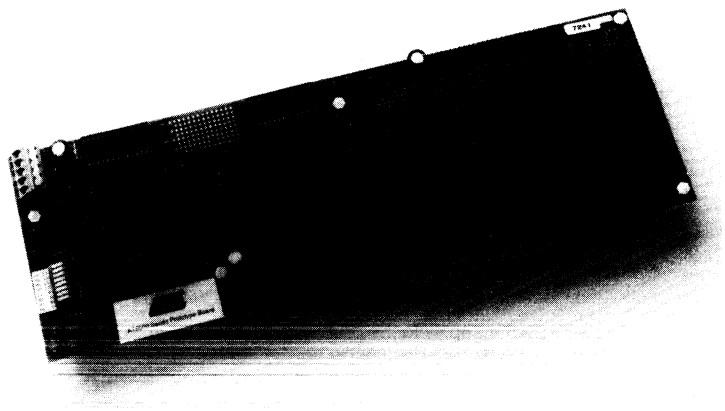
- **Prototype Board**
  - **PC/AT-Compatible Expansion Board Edge Connector**
  - **84-Pin PLCC High-Pressure Tin Socket with Solder Tails**
  - **132-Pin PQFP Micro-Pitch Socket**
  - **Over 16 Square Inches of Wire-Wrap Area**
  - **Test-Point Headers for Easy Access to V_{CC}, GND, and FPGA I/O Signals**
  - **Pre-Wired Header for Download Cable Connection**
  - **Pre-Wired Sockets for Serial E^2PROMor Parallel Configuration EPROMs**
- **Materials for Device Configuration via PC Parallel Port**
  - **Cable Adapter Nodule**
  - **DB25-Male-to-DB25-Female Cable**
  - **Ten-Conductor Ribbon Cable**

Description

Atmel's Prototype Kit lets engineers try out an FPGA design in silicon and analyze its operation in a systems environment. The Kit includes a PCB assembly with sockets for two FPGAs and space for adding active components. The board can be set up to run in at least three ways:

- Attached to a host PC running the AT6000 series design software. The Design Manager control panel is used to send configuration data to the board via the download cable supplied with the Integrated Development System.
- Attached to a PC that isn't running the Atmel Integrated Development System. The Integrated Development System generates download files that can be used on any DOS-based PC to send configuration data to the board.
- Not attached to a host PC (stand-alone). Sockets on the board are used to hold E^2PROMs programmed with configuration data. Power is supplied to the board from an external source.

AT6000 Series Prototype Board



0452A

Board Contents (in alphabetical order)

Symbol	Name	Description
C1-C12	Bypass Capacitors	Used to stabilize the V_{CC} and GND lines and filter out unwanted frequency components. Capacitors are placed near each FPGA to minimize any transient currents arising from device switching and magnetic coupling. Bulk capacitors placed near power supply connections accommodate the continually changing I_{CC} requirements of the total power system.
D1	Power LED	Lights up when power is applied to the board.
E1, E3	AT27C010 Parallel EPROM Socket	Holds standard 128K x 8 parallel EPROMs (e.g., Atmel AT27C010), which can be used with configuration modes 1, 2, or 5. Table 2 lists recommended EPROMs. The configuration application note (included with the Integrated Development System) has more on configuration modes.
E2, E4	Serial E^2PROM Socket	Holds standard serial E^2PROMs (e.g., Atmel AT17128), which can be used with configuration modes 3 or 4. Table 2 lists recommended E^2PROMs. The configuration application note (included with the Integrated Development System) has more on configuration modes.
F1	Power Supply Fuse (optional)	The board is wired with a zero-ohm resistor which can be replaced with a solid-state fuse or current-limiting device when such protection is desired.
J1	84-Pin PLCC FPGA Download Cable Connector	Attaches the download cable to the board so a PC can be used to configure an 84-pin device using mode 3.
J2	132-Pin PQFP FPGA Download Cable Connector	Attaches the download cable to the board so a PC can be used to configure a 132-pin device using mode 3.
J3, J4, J5, J6	84-Pin PLCC FPGA Pin Access Headers	Provides access to all pins on an 84-pin PLCC FPGA. Pin access headers can be used for wire-wrapping prototype circuits or for connecting the FPGA to a logic analyzer or oscilloscope. An access header post is provided for each device pin, including power pins (refer to the AT6000 Series data sheet for device pin descriptions). The number next to each header post indicates the header's corresponding package pin.
J7, J8, J9, J10	132-Pin PQFP FPGA Pin Access Headers	Provides access to all pins on a 132-pin PQFP FPGA. Pin access headers can be used for wire-wrapping prototype circuits or for connecting the FPGA to a logic analyzer or oscilloscope. An access header post is provided for each device pin, including power pins (refer to the AT6000 Series data sheet for device pin descriptions). The number next to each header post indicates the header's corresponding package pin.
J11, J12	Power Supply Access Headers	Provides access to power and ground for wire wrapping circuits. Each power supply access header shares a column of +5 V pins, which in turn share power and ground with the FPGA, EPROMs, configuration headers, and AT Bus edge connectors.
J13, J14	AT Bus Access Headers	Provides access to the AT edge connector signals. Each AT bus access header is connected to a finger. The power labels correspond to the bus standard. The GND and +5 V edge connector headers are already wired to the GND and +5 V power planes on the prototype board.
J15	Power Supply Connector	Connects a +5 V supply to the prototype board when power is not supplied by a host PC. Two connections are used for +5 V, and two are used for GND. The fifth connection goes to an unused board trace and can be wired for different applications. To attach a wire, depress the lever, insert the wire into the hole, and release the lever to make solid contact with the wire. Most gauges of stripped wire will work.

Board Contents (continued)

Symbol	Name	Description
L0-L15	Ground Loops	Connects a logic analyzer or oscilloscope to the ground plane for cleaner, simpler test setup.
SW1-8	Mode Select Switches SW8 M0 84-pin PLCC SW7 M1 84-pin PLCC SW6 M2 84-pin PLCC SW5 CS 84-pin PLCC SW4 M0 132-pin PQFP SW3 M1 132-pin PQFP SW2 M2 132-pin PQFP SW1 CS 132-pin PQFP	Selects the configuration mode. Each switch is connected to one of the configuration control pins (M0, M1, M2, or CS). When the switch is open, it drives the input with a logic "1." When closed, it drives the input with a logic "0." The logical "1" and "0" positions are noted on the board silkscreen.
U1	84 Pin PLCC Socket AMP Socket # 821573-1 AMP Tool # 821590-1	Holds any AT6000 Series device housed in an 84-pin PLCC package. The location of power, ground, and configuration pins is constant throughout the family, making the socket compatible with any AT6000 Series device in this package. The arrow on the socket indicates Pin 1. The 84-pin PLCC can be inserted by hand, but an extraction tool from AMP Incorporated (84 PLCC #821590-1) can make removal easier.
U2	132 pin PQFP Socket AMP Socket # 821949-5 AMP Cover # 821942-1 AMP Tool # 821958-2 AMP Sheet # 15-9516	Holds any AT6000 Series device housed in a 132-pin PLCC package. The location of power, ground, and configuration pins is constant throughout the family, making the socket compatible with any AT6000 Series device in this package. The arrow on the socket indicates Pin 1. An insertion and extraction tool from AMP Incorporated (132 PQFP #821958-2) is recommended for inserting and removing the PQFP.

Board Setup and Configuration Requirements

Attaching to a PC Running the Integrated Development System

This setup lets the engineer configure devices from within the Design Manager environment. There engineer doesn't have to pull the FPGA out of the board or reprogram EPROMs for each design iteration.

Board Setup

To link the board to a host PC, use the DB25-male-to-DB25-female cable to connect the PC parallel or printer port (LPT1: or LPT2:) to the cable adapter module. Use the ten-conductor ribbon cable to connect the cable adapter module to the configuration headers J1 and J2. Figures 1 and 2 show how to connect the cable adapter module to the 84-pin and 132-pin sockets respectively.

Bit streams sent over the PC parallel port use mode 3 (bit-sequential, external CCLK—see the AT6000 Series configuration application note for more information about configuration modes). Make sure the FPGA is set up for mode 3 before applying power to the board.

To configure a device in the 84-pin socket, set mode switch SW6 to 0, SW7 to 1, and SW8 to 1. This selects the correct settings for mode 3 configuration: M2=0, M1=1, and M0=1. Close the $\overline{CS}$ switch SW5 to supply a logical "0" to the $\overline{CS}$ input.

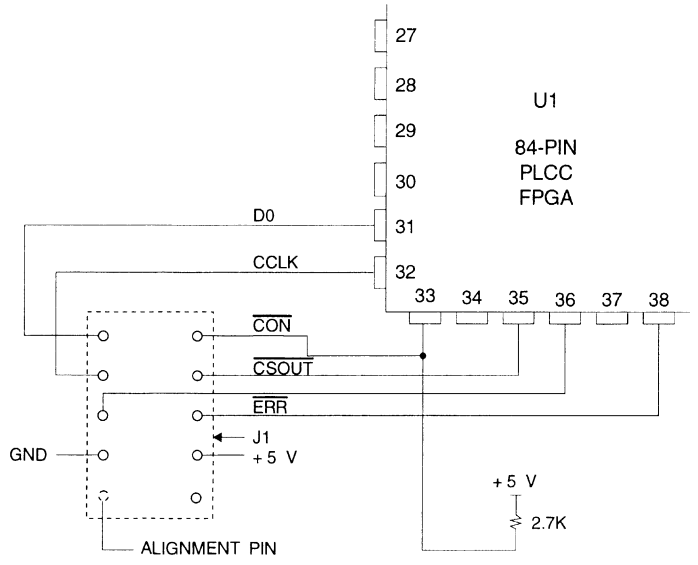
To configure a device in the 132-pin socket, set mode switch SW2 to 0, SW3 to 1, and SW4 to 1. This selects the correct settings for the mode 3 configuration: M2=0, M1=1, and M0=1. Close $\overline{CS}$ switch SW1 to supply a logical "0" to the $\overline{CS}$ input.

It is very important that the PC and the prototype board power supply be capable of sharing a common ground. The download cable connects the PC parallel port ground to the prototype board ground. The Schmitt trigger module gets its power (~5mA) from the prototype board. The user is responsible for solving any ground contention problems between the PC and the user power supply. *Atmel is not responsible for damage to the PC or power supply caused by improper grounding of the lab setup.*

Once the board is properly connected to the PC and the mode switches are in their proper position, a power supply of between 4.75 and 5.25 volts can be applied to jumper J15. It is recommended that the supply be a minimum of 1 ampere to accommodate any current spikes generated by high-speed, simultaneously switching outputs. If the power LED does not light once power is supplied, immediately disconnect power and check the polarity of hand-wired circuits and the power supply fuse for possible problems.

The prototype board can be treated like an add-in board and put inside the PC chassis. Place the board inside the PC and attach it to the PC/AT-compatible bus slot. Turn the PC power supply off and *do not* use the power supply connector J1 with this setup. The download cable should still be connected to the parallel port and the prototype board in the PC. Power is supplied from the PC bus.

Figure 1. Ribbon Cable Header Connecting 84-Pin Socket



Initiating Configuration

Instructions for using the Design Manager to generate the bit stream appear in the Integrated Development System User's Guide. When generating the bit stream, make sure of four things:

1. The bit stream is generated using mode 3.
2. Disable Data Check (B3) is not set or the $\overline{\text{CHECK}}$ pin is tied high on the prototype board.
3. The $\overline{\text{ERR}}$ pin is operating without interference so it can verify the download process.
4. LPT1: is the default printer port. To use LPT2:, change the default setting in the System Setup/User Settings/Miscellaneous panel.

Attaching to a PC that Isn't Running the Integrated Development System

A security block restricts the Integrated Development System to a single PC, but an executable download program (provided with the Integrated Development System) makes configuration more portable. Two files are used to download configurations to the prototype board from any PC/AT:

- downld.exe
- <design name>.bst

This setup is particularly useful if the test equipment needed to analyze the design is in a different room or if design work is divided among many engineers.

Board Setup

The prototype board connects to the host PC in the same way as described in the previous section.

PC Setup

The following Integrated Development System files are use to download a bit stream from the host PC:

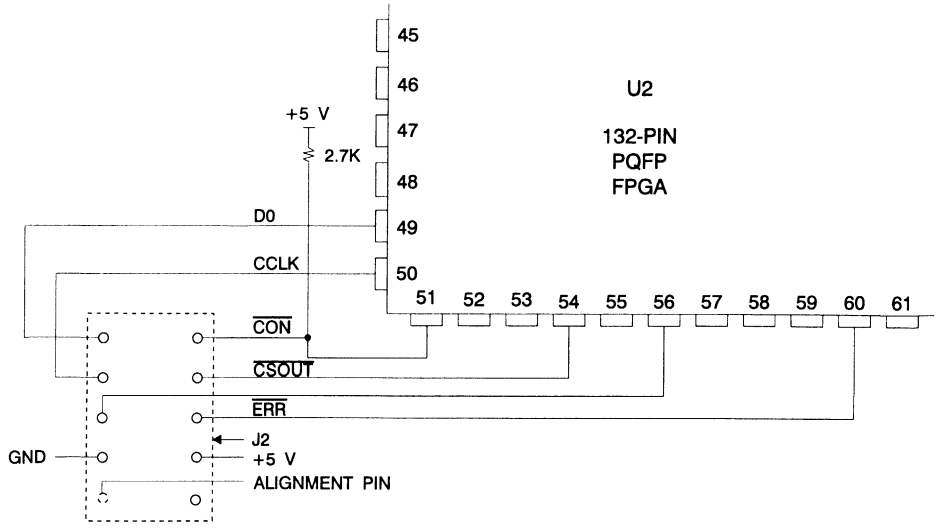
- downld.exe
- Downld.exe transfers the .bst file from the PC to the prototype board. It is stored with the other executables in the \atmel\bin\ directory. It is the only executable file needed by the host PC.
- It uses the dual-function $\overline{\text{ERR}}$ pin to detect errors in downloading the configuration file. If $\overline{\text{ERR}}$ goes low, an error has occurred. The error is displayed on the screen. To prevent false errors, make sure the $\overline{\text{ERR}}$ pin operates without interference during the download process. Refer to the AT6000 Series configuration application note for more on dual-function pins.
- <design name>.bst
- Contains the bit stream used to configure the device. The Integrated Development System User's Guide describes how to generate a <design name>.bst file.
- Follow these steps to set up the host PC for downloading configuration. Refer to the Integrated Development System User's Guide for more details.

1. Load the downld.exe file onto the PC.
2. Load the <design name>.bst file onto the PC.
3. Place the design.cfg file, edited to specify the parallel port to be used (LPT1: is the default), in the project sub-directory.

Initiating Configuration

Table 1 lists commands used to invoke the downld.exe files. Port can be either of the parallel printer ports LPT1 or LPT2. LPT1 is the default. The port argument is case-sensitive.

Figure 2. Ribbon Cable Header Connecting 132-Pin Socket



Configuring as a Stand-Alone (Not Attached to a Host PC)

It is possible to use the prototype board without the download cable. The prototype board is supplied with sockets for serial E^2PROMs and parallel configuration EPROMs. Stand-alone operation can be used to test and verify memory devices before production. It can also help in the verification of a prototype system using auto configuration. Mode 4 loads configuration data from the E^2PROM right after the application of power. Mode 5 does not automatically generate a $\overline{CON}$ signal after the power-up boot sequence. Configuration is initiated by driving $\overline{CON}$ low. Serial E^2PROMs are best suited for mode 4 configuration, parallel EPROMs for mode 5.

Board Setup

Sockets E1 and E3 hold standard 128K-x-8 parallel EPROMs (e.g., AT 27C010), which can be used with configuration modes 1, 2, or 5. Figure 3 shows how the socket is wired to the FPGA.

Sockets E2 and E4 hold standard serial E^2PROMs (e.g., AT17128), which can be used with configuration modes 3 or 4. Figure 4 shows how the socket is wired to the FPGA.

The AT6000 Series configuration application note gives more detailed configuration requirements. When setting up the board for auto-configuration, make sure of three things:

1. The configuration mode select switches are set to the proper value before power is applied to the board.
2. The $\overline{CS}$ switch for the device being used is closed.
3. If a mode other than 4 or 5 is to be used, a configuration clock must be supplied by the user. Configuration is initiated by pulsing the $\overline{CON}$ pin low.

In this setup, power is applied through the J15 jumper, or the board is installed into a PC bus. Make sure the mode switches are set and the programmed memory device is properly installed before applying power to the host PC.

Table 1. Commands Used to Invoke Download.exe Files

DOWNLD <design name>
DOWNLD/PLPT2<design name>.bst

Figure 3. Parallel EPROM and Mode 5 Configuration

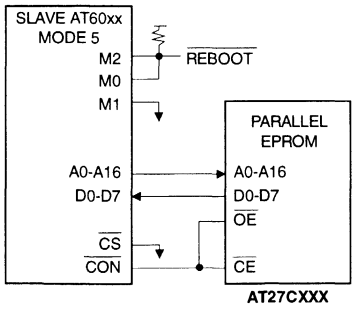
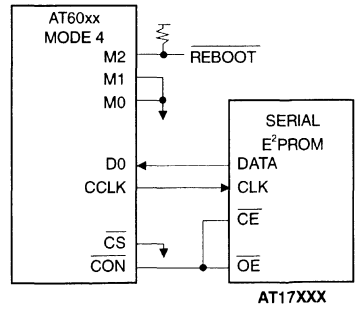


Figure 4. Serial E^2PROM and Mode 4 Configuration



E²PROM Setup

The Integrated Development System can generate a bit stream in the Intel HEX format, accepted by most programmers. To generate a bit stream in HEX format, run the Bit Stream or Cascade program with the Intel Hex Format box checked in the Device Programming/Build Bit Stream panel or the Device Programming/Bit Stream Utilities/Cascade Bit Stream panel, as appropriate.

See the Integrated Development System User's Guide for more information.

A Note About EPROMs and E²PROMs

Virtually any EPROM with an access time faster than 500 ns and an active-low output enable control is suitable for storing configuration data. FPGA density and required configuration speed determine which EPROM is most appropriate.

The amount of memory needed to hold configuration data increases as the FPGA gets larger. The AT6002 needs 2,676 bytes (21,408 bits) of storage capacity for full configuration; the AT6005 needs 8,077 bytes (64,616 bits). Compressed and partial-configuration bit streams use fewer bits and require less space.

Atmel and other vendors carry suitable parallel EPROMs. Atmel offers serial E²PROMs large enough for the AT6000 series. The ones from Atmel are reprogrammable. All these memory devices are available in "through-hole" DIPs and surface-mount packages. They can be programmed using industry-standard programmers, like those from DATA I/O Corporation.

Table 2. Recommended Memory Devices

	Part Number	Size
Parallel E²PROMs		
Atmel	AT27C64	8K x 8
	AT27C256	32K x 8
	AT27C010	128K x 8
Serial E²PROMs		
Atmel	AT17C65	64K x 1
	AT17C128	128K x 1
	AT17C256	256K x 1

Contents

Features

- 0.6µm Drawn Gate Length (0.5µm Leff) Sea-of-Gates Architecture With Triple Level Metal
- 5.0 Volt, 3.3 Volt, and 2.0 Volt Operation Including Mixed Voltages
- On Chip Phase Locked Loop Available to Synthesize Frequencies up to 150 MHz and Manage Chip-to-Chip Clock Skew
- Compiled (gate level) and Embedded (custom) SRAMs Available
- PCI, SCSI, and High Speed (200 MHz) Buffers Available
- Easy Alternative Sourcing of Existing ASIC, FPGA, and PLD Designs
- Design-for-Test methods — Including JTAG, Serial and Boundary Scan, and ATPG
- High Output Drive Capability: up to 48 mA with Slew Rate Control

Description

Atmel's next generation ATL60 Series CMOS Gate Arrays are fabricated using a 0.6µm drawn gate, oxide isolated, triple level metal process. Extensive cell libraries are available and support the major CAD software tools. As with all Atmel gate array families, customer involvement and satisfaction is integral to all steps of the design flow. A variety of Design for Testability techniques are supported by the libraries, and a wide range of packaging options are available.

ATL60 Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate[1] Speed
ATL60/4	4,000	3,000	44	36	200 ps
ATL60/15	15,000	10,000	68	60	200 ps
ATL60/25	25,000	16,900	84	76	200 ps
ATL60/40	38,000	25,400	100	92	200 ps
ATL60/60	58,000	34,600	120	112	200 ps
ATL60/85	86,000	51,900	144	136	200 ps
ATL60/110	110,000	65,900	160	152	200 ps
ATL60/150	149,000	89,300	184	176	200 ps
ATL60/200	195,000	116,900	208	200	200 ps
ATL60/235	232,000	139,500	226	218	200 ps
ATL60/300	301,000	181,000	256	248	200 ps
ATL60/435	430,000	260,000	304	296	200 ps
ATL60/550	545,000	288,000	340	332	200 ps
ATL60/700	693,000	363,000	380	372	200 ps
ATL60/870	870,000	456,000	424	416	200 ps
ATL60/1100	1,119,000	590,000	480	472	200 ps

Note: 1. Nominal 2 Input NAND Gate with a Fan Out of 2

ATL60 Series Gate Arrays

ATL60/4
ATL60/15
ATL60/25
ATL60/40
ATL60/60
ATL60/85
ATL60/110
ATL60/150
ATL60/200
ATL60/235
ATL60/300
ATL60/435
ATL60/550
ATL60/700
ATL60/870
ATL60/1100

Preliminary

5

0388B

Design

Design Systems Supported

Atmel supports four major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and accurate pre-route delay simulations. Verilog-XL is Atmel's golden simulator. The following design systems are supported:

Cadence/Composer	Viewlogic
Synopsys	Mentor 8.X

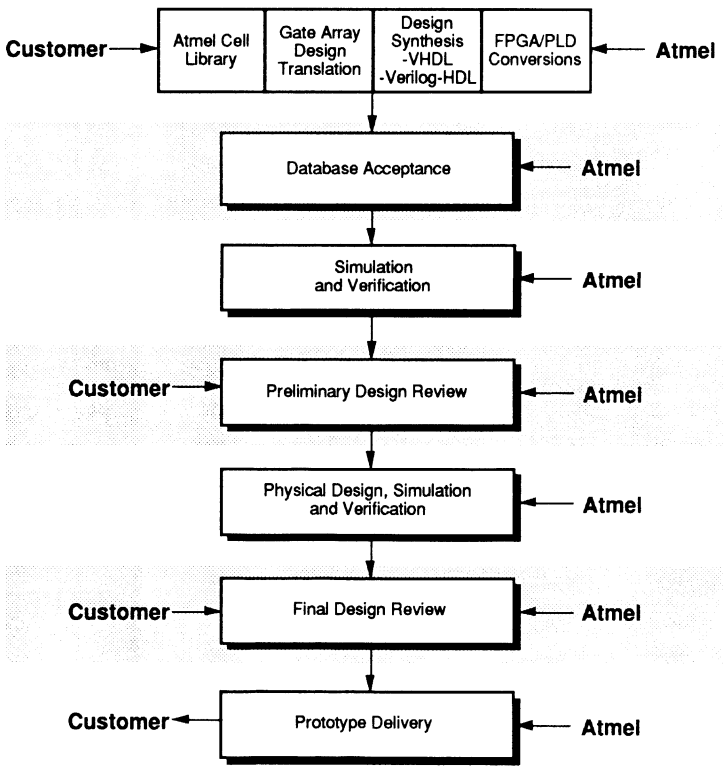
Design Flow

Atmel provides four methods for implementing a gate array design, while maintaining the same basic design flow for each of them. This flow involves both the Customer and Atmel at all critical review and acceptance steps, as can be seen from the chart below. Data Base Acceptance occurs when Atmel receives and accepts the complete design data base. The Preliminary Design Review follows Cadence simulation and verification by Atmel. This includes functional as well as timing performance evaluation. Upon completion of this critical step, Atmel performs physical place-and-route. Additional simulations are performed, based on the physical design, including the generation of a back annotation report to provide the customer with the most accurate timing information available. Final Design Review is the last step of the design flow prior to generation of masks. After this acceptance step is completed, masks are generated and released, and prototype parts, in ceramic packages, are delivered.

Pin Definition Requirements

Within the Physical Design Step (ie. layout) certain restrictions apply during pin definition. The corner pins on each die are reserved and programmable for Power and Ground only. All other buffer pins are fully programmable as Input, Output, Bi-directional, Clock-into-Array, Power, or Ground.

ATL60 Gate Array Design Flow



Design Options

Schematic Capture

The schematic capture method of design is performed by the customer using an Atmel provided macro cell library. A complete netlist and vector set must then be provided to Atmel. Upon acceptance of this data set, Atmel continues with the standard design flow.

VHDL/Verilog-HDL

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. VHDL or Verilog-HDL is Atmel's preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic, Motorola, SMOS, Oki, NEC, Fujitsu, AMI and others) into our gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx, Actel Altera, AMD and Atmel) into our gate arrays. There are four primary reasons to convert from an FPGA/PLD to a gate array. Conversion of high volume devices (over 10,000 units) for a single or combined design is cost effective. Performance can often be optimized for speed or power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

ATL60 Series Cell Library

Atmel's ATL60 Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The ATL60 Series PLL operates at frequencies of up to 150 Mhz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization. Output buffers are programmable to meet the voltage and current requirements of both PCI and SCSI.

These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the military temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Cell Index

Signal Name	Description	Site Count(1)
ADD3X	1 bit full adder with buffered outputs	10
AND2	2 input AND	2
AND2H	2 input AND - high drive	3
AND3	3 input AND	3
AND3H	3 input AND - high drive	4
AND4	4 input AND	3
AND4H	4 input AND - high drive	4
AND5	5 input AND	5
AOI22	2 input AND into 2 input NOR	2
AOI22H	2 input AND into 2 input NOR - high drive	4
AOI222	Two, 2 input ANDs into 2 input NOR	4
AOI222H	Two, 2 input ANDs into 2 input NOR - high drive	8
AOI2223	Three, 2 input ANDs into 3 input NOR	4
AOI2223H	Three, 2 input ANDs into 3 input NOR - high drive	7
AOI23	2 input AND into 3 input NOR	2
BUF1	1x buffer	2
BUF2	2x buffer	2
BUF2T	2x Tri State bus driver with active high enable	4
BUF2Z	2x Tri State bus driver with active low enable	4
BUF3	3x buffer	3
BUF4	4x buffer	3
BUF8	8x buffer	5
BUF12	12x buffer	8
BUF16	16x buffer	10
CLA7X	7 input carry lookahead	5
DEC4	2:4 decoder	7
DEC4N	2:4 decoder with active low enable	9
DEC8N	3:8 decoder with active low enable	24

Note: 1. A single ATL60 routing site contains 4 transistors, two N-channel and two P-channel, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%, with more accurate utilization figures generated by the netlist checker software(v3).

Cell Index

Signal Name	Description	Site Count(1)
DFF	D flip-flop	8
DFFBCPX	D flip-flop with asynchronous clear and preset with complementary outputs	16
DFFBSRX	D flip-flop with asynchronous set and reset with complementary outputs	16
DFFC	D flip flop with asynchronous clear	9
DFFR	D flip-flop with asynchronous reset	11
DFFS	D flip-flop with asynchronous set	9
DFFSR	D flip-flop with asynchronous set and reset	12
DLY1500	Delay buffer 1.5 ns	6
DLY2000	Delay buffer 2.1 ns	10
DLY6000	Delay buffer 6.0 ns	24
DSS	Set scan flip-flop	11
DSSBCPY	Set scan flip-flop with clear and preset	16
DSSBR	Set scan flip-flop with reset	13
DSSBS	Set scan flip-flop with set	13
DSSR	Set scan D flip-flop with reset	13
DSSS	Set scan D flip-flop with set	12
DSSSR	Set scan D flip-flop with set and reset	14
INV1	1x inverter	1
INV1D	Dual 1x inverters	2
INV1Q	Quad 1x inverters	4
INV1TQ	Quad Tri State inverter	7
INV2	2x inverter	2
INV2T	2x Tri State inverter with active high enable	3
INV3	3x inverter	2
INV4	4x inverter	2
INV8	8x inverter	4
INV10	10x inverter	8
JKF	JK flip-flop	10
JKFBCPX	Clear preset JK flip-flop with asynchronous clear and preset and complementary outputs	16
JKFC	JK flip-flop with asynchronous clear	12
LAT	LATCH	4
LATBG	LATCH with complementary outputs and inverted gate signal	6
LATBH	LATCH with high drive complementary outputs	7

Note: 1. A single ATL60 routing site contains 4 transistors, two N-channel and two P-channel, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%,with more accurate utilization figures generated by the netlist checker software(v3).

Cell Index

Signal Name	Description	Site Count(1)
LATR	LATCH with reset	4
LATS	LATCH with set	6
LATSR	LATCH with set and reset	8
LSCC	Voltage level shifter	4
LSISO	Voltage level shifter with power supply isolation function	12
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - high drive	5
MUX2I	2:1 MUX with inverted output	3
MUX2IH	2:1 MUX with inverted output - high drive	4
MUX2N	2:1 MUX with active low enable	4
MUX2NQ	Quad 2:1 MUX with active low enable	18
MUX2Q	Quad 2:1 MUX	14
MUX3I	3:1 MUX with inverted output	6
MUX3IH	3:1 MUX with inverted output - high drive	8
MUX4	4:1 MUX	9
MUX4X	4:1 MUX with transmission gate data inputs	10
MUX4XH	4:1 MUX with transmission gate data inputs - high drive	10
MUX5H	5:1 MUX - high drive	14
MUX8	8:1 MUX	18
MUX8N	8:1 MUX with active low enable	20
MUX8XH	8:1 MUX with transmission gate data inputs - high drive	18
NAN2	2 input NAND	2
NAN2D	Dual 2 input NAND	3
NAN2H	2 input NAND - high drive	2
NAN3	3 input NAND	2
NAN3H	3 input NAND - high drive	3
NAN4	4 input NAND	3
NAN4H	4 input NAND - high drive	4
NAN5	5 input NAND	5
NAN5H	5 input NAND - high drive	6
NAN6	6 input NAND	6
NAN6H	6 input NAND - high drive	7
NAN8	8 input NAND	7
NAN8H	8 input NAND - high drive	7
NOR2	2 input NOR	2

Note: 1. A single ATL60 routing site contains 4 transistors, two N-channel and two P-channel, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%,with more accurate utilization figures generated by the netlist checker software(v3).

Cell Index

Signal Name	Description	Site Count(1)
NOR2D	Dual 2 input NOR	3
NOR2H	2 input NOR - high drive	2
NOR3	3 input NOR	2
NOR3H	3 input NOR - high drive	3
NOR4	4 input NOR	3
NOR4H	4 input NOR - high drive	4
NOR5	5 input NOR	5
NOR8	8 input NOR	7
OAI22	2 input OR into 2 input NAND	2
OIA22H	2 input OR into 3 input NAND - high drive	4
OAI222	Two, 2 input ORs into 2 input NAND	2
OAI222H	Two, 2 input ORs into 2 input NAND - high drive	4
OAI22224	Four, 2 input ORs into 4 input NAND	6
OAI23	2 input OR into 3 input NAND	3
ORR2	2 input OR	2
ORR2H	2 input OR - high drive	3
ORR3	3 input OR	3
ORR3H	3 input OR - high drive	4
ORR4	4 input OR	3
ORR4H	4 input OR - high drive	4
ORR5	5 input OR	5
XNR2	2 input exclusive NOR	4
XNR2H	2 input exclusive NOR - high drive	4
XOR2	2 input exclusive OR	4
XOR2H	2 input exclusive OR - high drive	4

Note: 1. A single ATL60 routing site contains 4 transistors, two N-channel and two P-channel, aligned in columns. The number of sites used per gate varies according to the specific isolation and power requirements. Percent utilization varies from 50% to 70%,with more accurate utilization figures generated by the netlist checker software(v3).

I/O Buffer Cell Index

Signal Name	Description
PBD2C	4 mA bidi CMOS buffer
PBC3C	6 mA bidi CMOS buffer
PBD32TS	6 mA bidi TTL buffer with Schmitt Trigger
PBD5C	10 mA bidi TTL buffer with Schmitt Trigger
PBDSCSITS	48mA NMOS, SCSI buffer with TTL Schmitt Trigger
PBS1C	2 mA bidi CMOS buffer
PBS1CS	2 mA bidi CMOS buffer with Schmitt Trigger
PBS1TS	2 mA bidi TTL buffer with Schmitt Trigger
PBS2C	4 mA bidi CMOS input buffer
PBS2CS	4 mA bidi CMOS input buffer with Schmitt Trigger
PBS2T	4 mA bidi TTL buffer
PBS2TS	4 mA with Schmitt Trigger
PBS3C	6 mA bidi CMOS buffer
PBS3CS	6 mA with Schmitt Trigger
PBS31T	6 mA bidi TTL buffer
PBS3T	6 mA bidi TTL buffer
PBS3TS	6 mA bidi with Schmitt Trigger
PBS4C	8 mA bidi CMOS buffer
PBS4CS	8 mA bidi CMOS buffer with Schmitt Trigger
PBS4T	8 mA bidi TTL buffer
PBS4TS	8 mA bidi TTL buffer
PBS5C	10 mA bidi CMOS buffer
PBS5CS	10 mA bidi with Schmitt Trigger
PBS5T	10 mA bidi TTL buffer
PBS5TS	10 mA with Schmitt Trigger
PBS6C	12 mA bidi CMOS buffer
PBS6CS	12 mA bidi Schmitt Trigger
PBS6T	12 mA bidi TTL buffer
PBS6TS	12 mA bidi TTL buffer with Schmitt Trigger
PBS7C	14 mA bidi CMOS buffer
PBS7CS	14 mA bidi CMOS buffer with Schmitt Trigger
PBS7T	14 mA bidi TTL buffer
PBS7TS	14 mA bidi TTL buffer with Schmitt Trigger
PBS8C	16 mA bidi CMOS buffer
PBS8CS	16 mA bidi CMOS buffer with Schmitt Trigger
PBS8T	16 mA bidi TTL buffer
PBS8TS	16 mA bidi TTL buffer with Schmitt Trigger
PBS9C	18 mA bidi CMOS buffer

I/O Buffer Cell Index

Signal Name	Description
PBS9CS	18 mA bidi CMOS buffer with Schmitt Trigger
PBS9T	18 mA bidi TTL buffer
PBS9TS	18 mA bidi TTL buffer with Schmitt Trigger
PBSAC	20 mA bidi CMOS buffer
PBSACS	20 mA bidi CMOS buffer with Schmitt Trigger
PBSAT	20 mA bidi TTL buffer
PBSATS	20 mA bidi with Schmitt Trigger
PBSA6T	20 mA bidi TTL buffer
PBSBC	22 mA bidi CMOS buffer
PBSBCS	22 mA bidi CMOS buffer with Schmitt Trigger
PBSBT	22 mA bidi TTL buffer
PBSBTS	22 mA bidi TTL buffer with Schmitt Trigger
PBSCC	24 mA dibi CMOS buffer
PBSCCS	24 mA bidi CMOS buffer with Schmitt Trigger
PBSCT	24 mA bidi TTL buffer
PBSC1T	24 mA bidi TTL buffer
PBSCTS	24 mA bidi TTL buffer with Schmitt Trigger
PIC	CMOS input buffer
PICI	CMOS inverting input buffer
PICS	CMOS input buffer with Schmitt Trigger
PIT	TTL input buffer
PITS	TTL input buffer with Schmitt Trigger
PK8	16 mA clock driver
PKC	24 mA clock driver
PO1	2 mA output buffer
PO2	4 mA output buffer
PO2B	4 mA inverting output buffer
PO3	6 mA output buffer
PO4	8 mA output buffer
PO5	10 mA output buffer
PO6	12 mA output buffer
PO61	12 mA output buffer
PO7	14 mA output buffer
PO8	16 mA output buffer
POZ8B	16 mA open Crain inverting output buffer
PO9	18 mA output buffer
POA	20 mA output buffer
POB	22 mA output buffer

I/O Buffer Cell Index

Signal Name	Description
POC	24 mA output buffer
PTD2	4 mA Tri State output buffer
PTD3	6 mA Tri State output buffer
PTD32	6 mA Tri State output buffer
PTD5	10 mA Tri State output buffer
PTS1	2 mA Tri State output buffer
PTS2	4 mA Tri State output buffer
PTS3	6 mA Tri State output buffer
PTS31	6 mA Tri State output buffer
PTS33	6 mA Tri State output buffer
PTS4	8 mA Tri State output buffer
PTS41	8 mA Tri State output buffer
PTS5	10 mA Tri State output buffer
PTS6	12 mA Tri State output buffer
PTS63	12 mA Tri State output buffer
PTS7	14 mA Tri State output buffer
PTS8	16 mA Tri State output buffer
PTS81	16 mA Tri State output buffer
PTS9	18 mA Tri State output buffer
PTSA	20 mA Tri State output buffer
PTSA6	20 mA Tri State output buffer
PTSB	22 mA Tri State output buffer
PTSC	24 mA Tri State output buffer
PTSC1	24 mA Tri State output buffer
PTSC2	24 mA Tri State output buffer
PX2CL	4 mA crystal oscillator buffer (left side normalized input)
PX2CR	4 mA crystal oscillator buffer (right side normalized input)
PX4CL	8 mA crystal oscillator buffer (left side normalized input
PX4CR	8 mA crystal oscillator buffer (right side normalized input)

CMOS Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{DD}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V[1]
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN}=V_{DD}$, V_{DD}=5.5 V			10	µA
I_{IL}	Input Leakage Low (no pull-up) 40K pull-up	$V_{IN}=V_{SS}$, V_{DD}=5.5V $V_{IN}=V_{SS}$, V_{DD}=5.5V	-10 -100		 -15	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN}=V_{DD}$ or V_{SS}, V_{DD}=5.5V	-10		10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(1)	V_{DD}=5.5V, $V_{OUT}=V_{DD}$ V_{DD}=5.5V, $V_{OUT}=V_{SS}$		66 -66		mA mA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	TTL Switching Threshold CMOS Switching Threshold	V_{DD}=5.0 V, 25°C V_{DD}=5.0 V, 25°C		1.4 2.4		V V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2mA I_{OL} per stage	I_{OL}=as rated V_{DD}=4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2mA I_{OH} per stage	I_{OH}=as rated V_{DD}=4.5 V	0.7 x V_{DD}	4.2		V

Note: 1. This is the specification for the 3 x Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 2.7 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN}=V_{DD}$, V_{DD}=3.6 V			5	µA
I_{IL}	Input Leakage Low (no pull-up) Max R pull-up (U31)	$V_{IN}=V_{SS}$, V_{DD}=3.6V $V_{IN}=V_{SS}$, V_{DD}=3.6V	-5 -25		 -3	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN}=V_{DD}$ or V_{SS}, V_{DD}=3.6V	-5		5	µA
I_{OS}	Output Short Circuit Current (8 x Buffer)(1)	V_{DD}=3.6V, $V_{OUT}=V_{DD}$ V_{DD}=3.6V, $V_{OUT}=V_{SS}$		88 -88		mA mA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.7xV_{DD}			V
V_T	CMOS Switching Threshold	V_{DD}=3.0 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1mA I_{OL} per stage.	I_{OL}=as rated V_{DD}=2.7 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1mA I_{OH} per stage.	I_{OH}=as rated V_{DD}=2.7 V	0.7xV_{DD}	4.2		V

2.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -0°C to +70°C, V_{DD} = 1.8 V to 2.2 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN}=V_{DD}$, V_{DD}=2.2 V			5	µA
I_{IL}	Input Leakage Low (no pull-up) Max R pull-up (U31)	$V_{IN}=V_{SS}$, V_{DD}=2.2V $V_{IN}=V_{SS}$, V_{DD}=2.2V	-5 -15		 -2	µA µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN}=V_{DD}$ or V_{SS}, V_{DD}=2.2V	-5		5	µA
I_{OS}	Output Short Circuit Current (8 x Buffer)(1)	V_{DD}=2.2V, $V_{OUT}=V_{DD}$ V_{DD}=2.2V, $V_{OUT}=V_{SS}$		40 -40		mA mA
V_{IL}	CMOS Input Low Voltage				0.2xV_{DD}	V
V_{IH}	CMOS Input High Voltage		0.8xV_{DD}			V
V_T	CMOS Switching Threshold			0.5xV_{DD}		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 0.5mA I_{OL} per stage.	I_{OL}as rated V_{DD}=1.8 V			0.2xV_{DD}	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -0.5mA I_{OH} per stage.	I_{OH}as rated V_{DD}=1.8 V	0.8xV_{DD}			V

Note: 1. This is the specification for the 8 x Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance, Input Buffer (die)	5.0 V, 3.3 V, 2.0 V		2.4		pF
C_{OUT}	Capacitance, Output Buffer (die)	5.0 V, 3.3 V, 2.0 V		5.6		pF
$C_{I/O}$	Capacitance, Bi-Directional	5.0 V, 3.3 V, 2.0 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.0	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.8	1.0		V
	CMOS Negative Threshold	25°C, 5.0 V	1.5	2.0		V
ΔV	TTL Hysteresis	25°C, 5.0 V		0.8		V
	CMOS Hysteresis	25°C, 5.0 V		1.0		V
V+	CMOS Positive Threshold	25°C, 3.3 V		1.8	2.3	V
V-	CMOS Negative Threshold	25°C, 3.3 V	1.0	1.3		V
ΔV	CMOS Hysteresis	25°C, 3.3 V		0.5		V

Design for Testability

Atmel supports a wide range of Design for Testability techniques to improve the percentage of a design that can be fully tested. By achieving a high degree of testability, a designer can reduce design and prototype debug time, minimize production test time, and improve board and system level test and diagnostic capability.

Synopsys Test Compiler software is fully supported by Atmel. By use of this system during design, the computer will create and add a set of scan chains to the design, and test vectors will be generated to provide greater than 95% fault coverage. This method requires only 1 or 2 added pins for Test Enable and Test Mode. This is the easiest and least expensive method of designing testability into a gate array design.

Ad Hoc means of increasing testability of a gate array are also available. Partitioning, memory array isolation, and test point insertion are encouraged and supported by the ATL60 Series gate arrays. Atmel also encourages the inclusion of Built In Self-Test (BIST) techniques whenever possible. Each of these methods is discussed in detail in the Atmel CMOS Gate Array Design Manual.

In addition to all of the above, the ATL60 Series gate arrays also support the Joint Test Action Group (JTAG) boundary scan architecture and Test Access Port (TAP) requirements. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in Atmel's cell library. Use of JTAG architecture requires an additional 4-5 pins for test mode, data, and clock signals.

Advanced Packaging

The ATL60 Series gate arrays are offered in a wide variety of standard packages, including plastic and ceramic quad flatpacks, thin quad flatpacks, ceramic pin grid arrays, and ball grid arrays. High volume on-shore and off-shore contractors provide assembly and test for commercial product, with prototype capability in Colorado Springs

Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
TQFP	44, 48, 52, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
BGA	121, 169, 225, 313
CPGA	64, 68, 84, 100, 124, 166, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340

Features

- **0.8 µ drawn (0.6 µ effective) gate length combined with triple level metal provides outstanding speed/density performance.**
- **All ATL80 arrays can operate at 5.0 volts and 3.3 volts for low-power applications. The ATL80 series can also operate in a mixed voltage environment.**
- **Design translation of existing ASIC, FPGA and PLD designs provide for easy alternate sourcing with equivalent performance.**
- **Product testability is improved using techniques such as serial and boundary scan, ATPG, built-in self test and JTAG.**
- **ATL80 arrays can be screened to MIL-STD-883.**

Description

The high-performance ATL80 Series CMOS gate arrays offer superior system performance, flexibility, testability and board utilization. The ATL80 gate arrays employ an advanced technology 0.8 µ-drawn, triple-level metal, Si-gate, CMOS technology processed in a U.S.-based, manufacturing facility.

Atmel's efficient routing scheme combined with tight spacing for three metal layers allows Atmel to provide more gates and faster speeds. With fine pitch bond pads as a standard feature, high I/O gate arrays can easily be accommodated. The ATL80 gate array can have a 3.3 volt or 5.0 volt core, combined with a 3.3 volt and/or 5.0 volt I/O on the same chip. Atmel's I/O can be personalized to accept a 5.0 volt input signal into a 3.3 volt buffer.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The 0.8 µ macro cell libraries are upward compatible with the existing 1.0 µ libraries and design utilities.

ATL80 Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate(1) Speed
ATL80/2	2,000	1,000	36	28	256 ps
ATL80/5	5,000	3,000	68	60	256 ps
ATL80/10	10,000	6,000	80	72	256 ps
ATL80/15	17,000	10,200	100	92	256 ps
ATL80/25	26,000	15,600	120	112	256 ps
ATL80/40	39,000	23,400	144	136	256 ps
ATL80/50	50,000	30,000	160	152	256 ps
ATL80/75	75,000	45,000	184	176	256 ps
ATL80/95	94,000	60,000	208	192	256 ps
ATL80/150	150,000	75,000	256	236	256 ps
ATL80/220	220,000	110,000	304	280	256 ps
ATL80/280	280,000	140,000	340	310	256 ps
ATL80/350	350,000	175,000	380	350	256 ps
ATL80/450	450,000	225,000	424	384	256 ps
ATL80/600	600,000	300,000	480	440	256 ps

Note: 1. Nominal 2 Input NAND Gate With a Fan Out of 2

ATL80 Series Gate Arrays 0.8 Micron

ATL80/2
ATL80/5
ATL80/10
ATL80/15
ATL80/25
ATL80/40
ATL80/50
ATL80/75
ATL80/95
ATL80/150
ATL80/220
ATL80/280
ATL80/350
ATL80/450
ATL80/600

5

0186C

ATL80 Design

Design Systems Supported

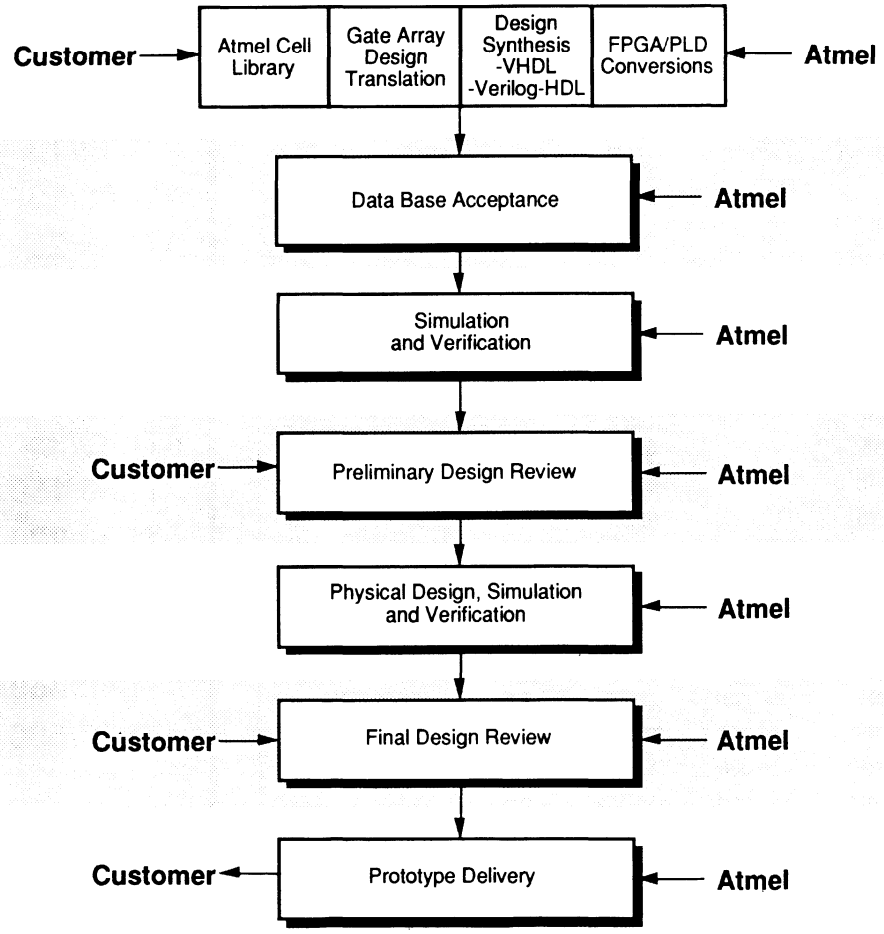
Atmel supports the major CAE/CAD software systems with complete macro cell libraries (symbols, timing and function), as well as utilities for checking the netlist and accurate pre-route delay simulations. Atmel uses Cadence's Verilog-XL as our golden simulator. The following design systems are supported:

Cadence/Composer	Viewlogic
Mentor 8.X	Synopsys

Design Flow

While Atmel provides four options for implementing a gate array design, they all have the same flow. Data base acceptance is the first milestone. This occurs when Atmel receives and accepts the complete design data base. Preliminary design review occurs when the performance of the design is set based on the Cadence simulation. Final design review is the last review of the design before making masks. The back annotation data is incorporated into the simulations. After final design review masks are released and prototypes, in ceramic packages, are delivered.

ATL80 Gate Array Design Flow



Design Options

Schematic Capture

Schematic capture and simulation are performed by the customer using an Atmel supplied macro cell library. The customer can also receive complete back annotation delay data for post-route simulation.

VHDL/Verilog-HDL

Atmel can accept Register Transfer Level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. Design via VHDL or Verilog-HDL is the preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic, Oki, NEC, Motorola, Fujitsu, SMOS, AMI and others) into our gate arrays. These designs have been optimized for speed, gate count, modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx, Actel, Altera, AMD and Atmel) into our gate arrays. The design can be optimized for speed or power consumption, modified to add logic or memory or replicated for a pin-for-pin compatible, drop-in replacement. Atmel frequently combines several devices onto a single gate array.

ATL80 Series Cell Library

Atmel's ATL80 series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 120 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. Characterization has been performed over the military temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATL80 series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters	
1x Buffer	1x Inverter
2x Buffer	Dual 1x Inverter
2x Tri-state Buffer	Quad 1x Inverter
2x Tri-state Buffer with Enable Low	Quad Tristate Inverter
3x Buffer	2x Inverter
4x Buffer	2x Tri-state Inverter
8x Buffer	3x Inverter
12x Buffer	4x Inverter
16x Buffer	8x Inverter
Delay Buffer 1.5 ns	10x Inverter
Delay Buffer 2.0 ns	Voltage Level Shifter
Delay Buffer 6.0 ns	Voltage Level Shifter with Power Supply Isolation

AND, NAND, OR, NOR Gates	
2 input AND	2 input NOR
2 input AND with High Drive	Dual 2 input NOR
3 input AND	2 input NOR with High Drive
3 input AND with High Drive	3 input NOR
4 input AND	3 input NOR with High Drive
4 input AND with High Drive	4 input NOR
5 input AND	4 input NOR with High Drive
2 input NAND	5 input NOR
Dual 2-input NAND	8 input NOR
2 input NAND with High Drive	2 input OR
3 input NAND	2 input OR with High Drive
3 input NAND with High Drive	3 input OR
4 input NAND	3 input OR with High Drive
4 input NAND with High Drive	4 input OR
5 input NAND	4 input OR with High Drive
5 input NAND with High Drive	5 input OR
6 input NAND	
6 input NAND with High Drive	
8 input NAND	
8 input NAND with High Drive	

Cell Guide

Multiplexers	
2:1 MUX	4:1 MUX
2:1 MUX with High Drive	4:1 MUX w/o Buffered Inputs
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs, High Drive
Inverting 2:1 MUX w/o Buffered Inputs, High Drive	5:1 MUX with High Drive
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable Low	8:1 MUX with Enable Low
Quad 2:1 MUX	8:1 MUX w/o Buffered Inputs High Drive
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs, High Drive	

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
3 input AND OR INVERT with High Drive	3 input OR AND INVERT with High Drive
4 input AND OR INVERT	4 input OR AND INVERT
4 input AND OR INVERT with High Drive	4 input OR AND INVERT with High Drive
4 input AND OR INVERT with 2 inputs to OR	4 input OR AND INVERT with 2 inputs to AND
6 input AND OR INVERT	8 input OR AND INVERT
6 input AND OR INVERT with High Drive	

Exclusive OR/NOR Gates	
1 bit Adder with Buffered Outputs	2 input Exclusive OR with High Drive
7 input Carry Lookahead	2 input Exclusive NOR
2 input Exclusive OR	2 input Exclusive NOR with High Drive

Decoders	
2:4 Decoder	3:8 Decoder with Enable Low
2:4 Decoder with Enble Low	

Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs and Inverted Gate Signal
D Flip-flop with Clear	LATCH with High Drive Complementary Outputs
D Flip-flop with Reset	LATCH with Reset
D Flip-flop with Set	LATCH with Set
D Flip-flop with Set/Reset	LATCH with Set and Reset
JK Flip-flop	
JK Flip-flop with Clear	
JK Flip-flop with Clear/Preset	

Cell Guide

Scan Cells	
Set-scan Flip-flop	Set Scan Flip-flop with Set and Reset
Set-scan Flip-flop with Reset	Set Scan Flip-flop with Preset
Set Scan Flip-flop with Set	

I/O Options
Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator
Output Drive Value Programmable from 2 mA to 24 mA in 2 mA increments with Slew Rate Control
CMOS or TTL Operation
Schmitt Trigger (Bidirectional, Input)
Inverting and Non-inverting Input Buffers (Bidirectional, Input)
Pullup Resistor - 12K Ω to 372K Ω
Pulldown Resistor - 3.5K Ω to 108.5K Ω

74XX Series Soft Macros
24 cells available

CMOS/TTL Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	3.5 V Minimum	1.5 V Maximum	$V_{DD}/2$ Typical
TTL	2.0 V Minimum	0.8 V Maximum	1.4 V Typical

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Maximum Operating Voltage	6.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 4.5 V to 5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 5.5 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up) 108K Ω pull-up (U9)	$V_{IN} = V_{SS}$, V_{DD} = 5.5 V $V_{IN} = V_{SS}$, V_{DD} = 5.5 V	-10 -125	-0.01 -50	 -20	µA µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 5.5 V	-10	0.01	10	µA
V_{IL}	TTL Input Low Voltage				0.8	V
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	TTL Switching Threshold CMOS Switching Threshold	V_{DD} = 5.0 V, 25°C V_{DD} = 5.0 V, 25°C		1.4 2.4		V V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 2 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 4.5 V		0.2	0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -2 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 4.5 V	0.7 x V_{DD}	4.2		V
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 5.5 V, $V_{OUT} = V_{DD}$ V_{DD} = 5.5 V, $V_{OUT} = V_{SS}$	10 -100	50 -50	100 -10	mA mA

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

3.3 Volt DC Characteristics

Applicable over recommended operating range from T_a = -55°C to +125°C, V_{DD} = 3.0 V to 3.6 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN} = V_{DD}$, V_{DD} = 3.6 V		0.01	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-10	-0.01		µA
	108K Ω pull-up (U9)	$V_{IN} = V_{SS}$, V_{DD} = 3.6 V	-90	-35	-15	µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN} = V_{DD}$ or V_{SS}, V_{DD} = 3.6 V	-10	0.01	10	µA
V_{IL}	CMOS Input Low Voltage				0.3 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.7 x V_{DD}			V
V_T	CMOS Switching Threshold	V_{DD} = 3.3 V, 25°C		1.5		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 1 mA I_{OL} per stage.	I_{OL} = as rated V_{DD} = 3.0 V			0.4	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -1 mA I_{OH} per stage.	I_{OH} = as rated V_{DD} = 3.0 V	0.7 x V_{DD}			V
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD} = 3.6 V, $V_{OUT} = V_{DD}$ V_{DD} = 3.6 V, $V_{OUT} = V_{SS}$	5 -60	25 -25	60 -5	mA mA

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance, Input Buffer (Die)	5.0 V, 3.3 V		2.4		pF
C_{OUT}	Capacitance, Output Buffer (Die)	5.0 V, 3.3 V		5.6		pF
$C_{I/O}$	Capacitance, Bi-Directional	5.0 V, 3.3 V		6.6		pF
Schmitt Trigger						
V+	TTL Positive Threshold	25°C, 5.0 V		1.8	2.0	V
	CMOS Positive Threshold	25°C, 5.0 V		3.2	3.5	V
V-	TTL Negative Threshold	25°C, 5.0 V	0.8	1.0		V
	CMOS Negative Threshold	25°C, 5.0 V	1.0	1.2		V
ΔV	TTL Hysteresis	25°C, 5.0 V	0.5	0.8		
	CMOS Hysteresis	25°C, 5.0 V	1.0	2.0		
V+	CMOS Positive Threshold	25°C, 3.3 V		2.0	2.4	V
V-	CMOS Negative Threshold	25°C, 3.3 V	1.0	1.3		V
ΔV	CMOS Hysteresis	25°C, 3.3 V	0.5	0.7		

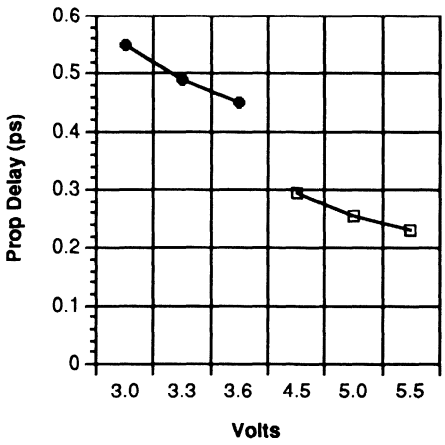
I/O Buffers

- Programmable output drive
  (2 to 24 mA I_{OL}, -2 to -24 mA I_{OH} for 5.0 V
  1 to 12 mA I_{OL}, -1 to -12 mA I_{OH} for 3.3 V)
- 3,000 volts ESD protection
- Built-in configurable test logic

The ATL80 series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 24 mA, and responds to CMOS or TTL logic levels. All outputs can be switched to a high impedance state. I/O locations on this ring can accommodate bidirectional cells.

AC Characteristics

Delay vs V_{CC}

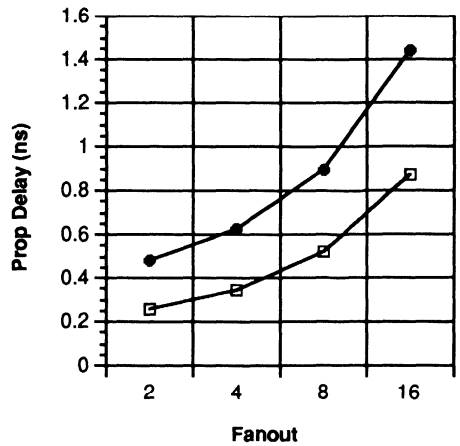


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout

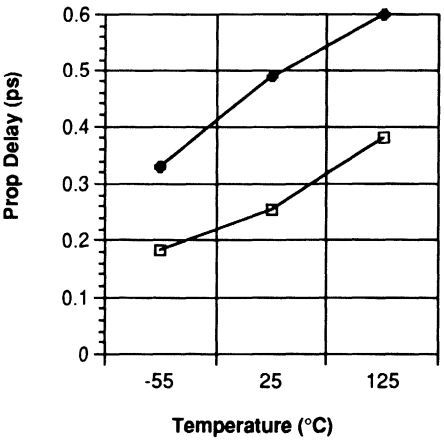


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
Temp = 25°C

Delay vs Temperature

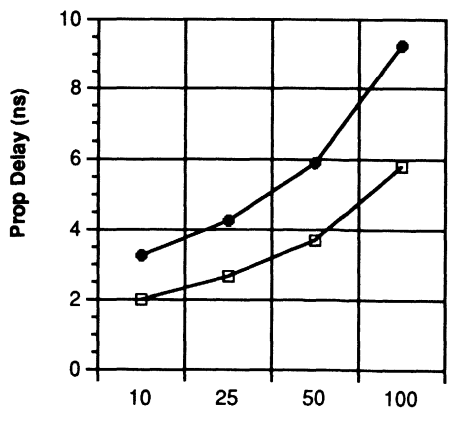


3.3 Volts V_{dd}

5.0 Volts V_{dd}

2 input NAND
FO = 2

Output Buffer vs Load



3.3 Volts V_{dd}

5.0 Volts V_{dd}

PDO4 - Output Buffer 8 mA
Temp = 25°C

5

Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board and system test time. These techniques can also improve system level test and diagnostic capability.

The ATL80 arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler. By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest and least expensive method for designing testability into a gate array design.

Advanced Packaging

Atmel supports a wide variety of standard packages for the ATL80 series, but also offers its ATL80 series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon.

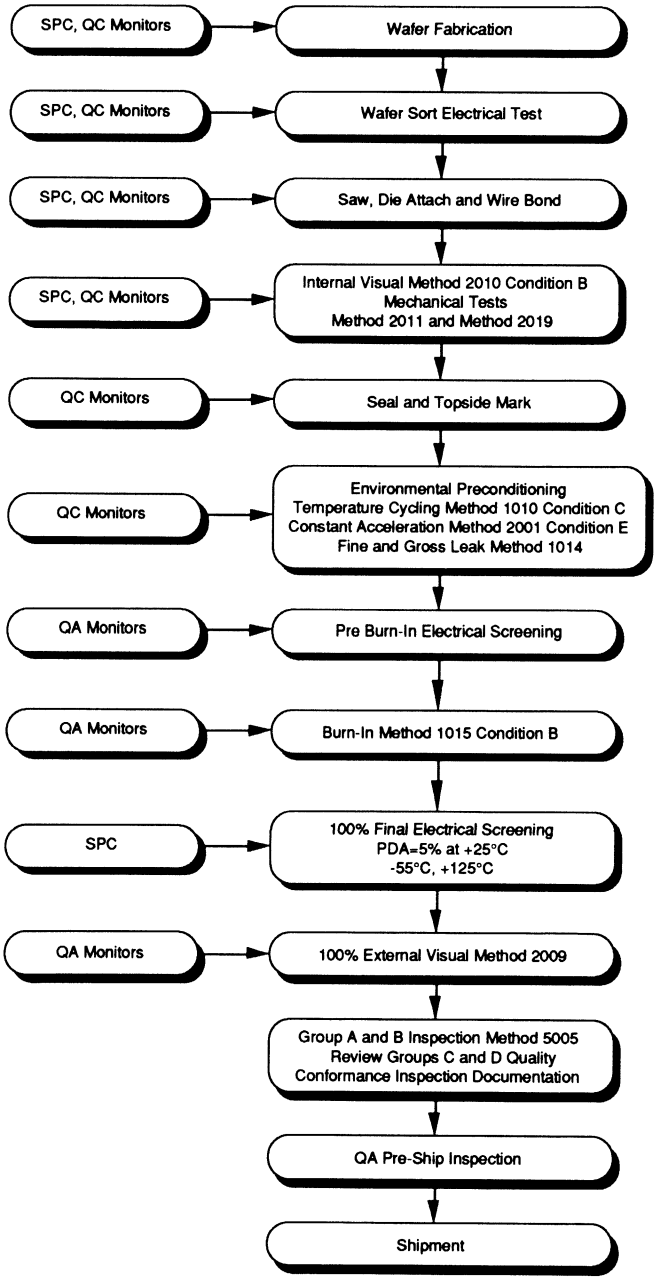
All of Atmel's standard packages have been characterized for thermal and electrical performance. When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
TQFP	44, 48, 52, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
BGA	121, 169, 225, 313

Military Product Flow Chart

MIL-STD-883 Class B



Features

- **Specifically Designed for Battery Powered Applications 1.0 - 3.0 Volts and will Operate from 0.7 to 5.5 Volts**
- **Static Current Drain of <75 nA at 1.0 Volts**
- **200 MHz Maximum Toggle Frequency for Flip Flop at 1.5 Volts**
- **1.0 µ Drawn Gate Length CMOS Gate Arrays**
- **All Package Styles Offered Including TQFP and TAB**
- **Improved Product Testability Using Serial Scan, Boundary Scan, and JTAG**
- **Second Source Existing ASIC Design in Atmel's ATLV via Design Translation. Improved Performance and Lower Cost**

ATLV Series Ultra Low Voltage Gate Arrays

ATLV2
ATLV3
ATLV5
ATLV7
ATLV10
ATLV15
ATLV20
ATLV35

5

Description

The ATLV Series CMOS gate arrays employ 1.0 µ-drawn, double-level metal, Si-gate, CMOS technology processed in Atmel's U.S.-based, advanced manufacturing facility. The arrays utilize an enhanced channelless architecture which results in greater than 50 percent usable gates.

Atmel's flexible design system uses industry design standards and is compatible with popular CAD/CAE software and hardware packages. The customer can start designing with the ATLV series today using existing CAD/CAE tools.

ATLV Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O(1) Pins	Gate(2) Speed
ATLV2	2,000	1,400	44	36	1.3 ns
ATLV3	3,000	1,600	68	60	1.3 ns
ATLV5	5,000	2,800	84	76	1.3 ns
ATLV7	7,000	4,400	100	92	1.3 ns
ATLV10	10,000	6,600	120	112	1.3 ns
ATLV15	15,000	8,000	144	136	1.3 ns
ATLV20	22,000	12,000	160	152	1.3 ns
ATLV35	35,000	18,000	208	192	1.3 ns

Notes: 1. Absolute maximum I/O pins is maximum pin count minus 8. Additional power and ground pins are assumed to be required to support simultaneous switching outputs as pin count increases.
2. Nominal 2 input nand gate with a fan out of 2 at 1.5 volts, room temperature.

ATLV Design

Design Systems Supported

Atmel supports the major CAE/CAD software systems with complete macro cell libraries (symbols, timing and function), as well as utilities for checking the netlist and accurate pre-route delay simulations. Atmel uses Cadence's Verilog-XL as our golden simulator. Design systems which are supported include Cadence, Viewlogic, Mentor, and Synopsys.

Design Flow

While Atmel provides four options for implementing a gate array design, they all have the same basic flow. Data base acceptance is the first milestone. This is when Atmel receives and accepts the complete design data base. Preliminary design review is where the performance of the design is set based on the Cadence simulation. Final design review is the last review of the design before making masks. The back annotation data is incorporated into the simulations. After final design review masks are released and prototypes in ceramic packages are delivered.

Design Options

Schematic Capture

Schematic capture and simulation are performed by the customer using an Atmel supplied macro cell library. The customer can also receive complete back annotation delay data for post-route simulation.

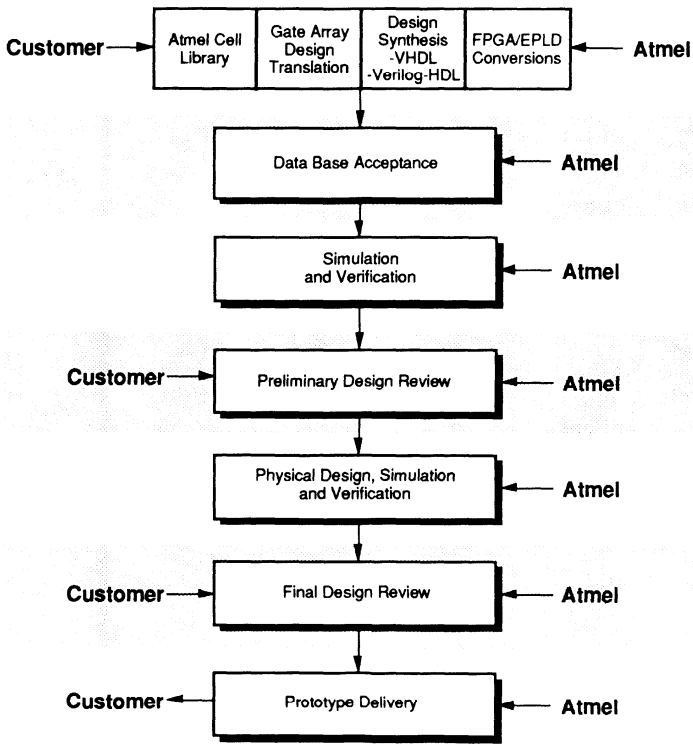
VHDL/Verilog-HDL

Atmel can accept Register Transfer level (RTL) designs for VHDL (MIL-STD-454, IEEE STD 1076) or Verilog-HDL format. Atmel fully supports Synopsys for VHDL simulation as well as synthesis. Design via VHDL or Verilog-HDL is the preferred method of performing a gate array design.

ASIC Design Translation

Atmel has successfully translated dozens of existing designs from most major ASIC vendors (LSI Logic, Oki, NEC, Fujitsu and others) into our gate arrays. These designs have been optimized for speed, gate count, modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

ATLV Gate Array Design Flow



FPGA and EPLD Conversions

Atmel has successfully translated existing FPGA/EPLD designs from most major vendors (Xilinx, Actel, Altera, AMD & Atmel) into our gate arrays. The design can be optimized for speed or power consumption, modified to add logic or memory or replicated for a pin-for-pin compatible, drop-in replacement. Atmel frequently combines several devices onto a single gate array.

ATLV Series Cell Library

Atmel's ATLV series gate arrays use cells from an accurately modeled and highly flexible library. The cell library contains over 120 hard-wired data path elements and has been characterized via extensive SPICE modeling at the transistor level and verified through measurements made on fabricated test arrays. The symbols for the ATLV cell library are compatible with Atmel's ATL (1.0 µ 3.3 and 5.0 V) and ATL80 (0.8 µ 3.3 and 5.0 V) cell libraries. Existing designs can be easily migrated to the ATLV series. Characterization has been performed over commercial temperature and 1.0 to 3.0 volts, to ensure that the simulation accurately predicts the performance of the finished product. Atmel is continually expanding the ATLV series cell library with both soft and hard macros. Check with your sales representative for the most recent additions.

Cell Guide

Buffers and Inverters	
1x Buffer	1x Inverter
2x Buffer	Dual 1x Inverter
2x Buffer with Enable	Quad 1x Inverter
2x Buffer with Enable Low	Quad Tri-state Inverter
3x Buffer	2x Inverter
4x Buffer	Dual 2x Inverter
8x Buffer	2x Tri-state Inverter
12x Buffer	3x Inverter
16x Buffer	4x Inverter
Delay Buffer 2.0 ns	8x Inverter
Delay Buffer 3.5 ns	10x Inverter
Delay Buffer 8.0 ns	

AND, NAND, OR, NOR Gates	
2 input AND	2 input NOR
3 input AND	Dual 2 input NOR
4 input AND	3 input NOR
5 input AND	4 input NOR
2 input NAND	5 input NOR
Dual 2-input NAND	8 input NOR
3 input NAND	2 input OR
4 input NAND	3 input OR
5 input NAND	4 input OR
6 input NAND	
8 input NAND	

Multiplexers	
2:1 MUX	4:1 MUX
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs
Inverting 2:1 MUX w/o Buffered Inputs	4:1 MUX w/o Buffered Inputs
2:1 MUX with Enable Low	8:1 MUX
Quad 2:1 MUX with Enable	8:1 MUX with Enable Low
Quad 2:1 MUX	
Inverting 3:1 MUX w/o Buffered Inputs	
Inverting 3:1 MUX w/o Buffered Inputs	

Cell Guide

AND/OR, OR/AND Gates	
3 input AND OR INVERT	3 input OR AND INVERT
4 input AND OR INVERT	4 input OR AND INVERT
6 input AND OR INVERT	8 input OR AND INVERT
Exclusive OR/NOR Gates	
1 bit Adder	2 input Exclusive OR
1 bit Adder with Buffered Outputs	2 input Exclusive NOR
7 input Carry Lookahead	
Decoders	
2:4 Decoder	3:8 Decoder with Low Enable
2:4 Decoder with Low Enable	
Flip-flops/Latches	
D Flip-flop	LATCH
D Flip-flop with Clear/Preset	LATCH with Complementary Outputs
D Flip-flop with Clear	LATCH with Inverted Gate Signal
D Flip-flop with Reset	QUAD LATBG with Common Gate Signal
D Flip-flop with Set	QUAD Inverting LATCH
D Flip-flop with Set/Reset	LATCH with Reset
JK Flip-flop	LATCH with Set
JK Flip-flop with Clear/Preset	LATCH with Set and Reset
JK Flip-flop with Clear	
Scan Cells	
Set-scan Register	Set-scan Register with Set
Set-scan Register with Clear and Preset	Set-scan Register with Set and Reset
Set-scan Register with Reset	
I/O Options	
Input, Output, Bidirectional, Tristate Output, Internal Clock Driver and Oscillator	
Output Drive Value Programmable from 0.5 mA to 6 mA in 0.5 mA increments with Slew Rate Control	
CMOS Operation	
Testable NAND Gate on Input (Bidirectional, Input)	
Inverting and Non-inverting Input Buffers (Bidirectional, Input)	
Pullup Resistor - 10K Ω to 310K Ω	
Pulldown Resistor - 3.5K Ω to 108.5K Ω	

CMOS Input Interface Characteristics

Interface	Logic High	Logic Low	Switchpoint
CMOS	0.90 V_{DD}	0.1 V_{DD}	V_{DD}/2 Typical

Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +5.5 V[1]
Maximum Operating Voltage	5.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{DD} + 0.75V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

1.5 Volt DC Characteristics

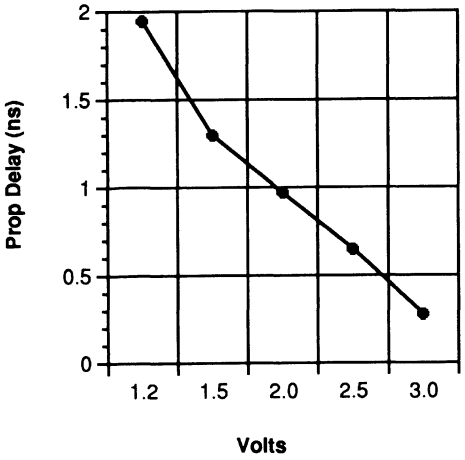
Applicable over recommended operating range from T_a = -40°C to +85°C, V_{DD} = 1.0 V to 3.0 V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{IH}	Input Leakage High	$V_{IN}=V_{DD}$, V_{DD}=1.8 V		1 x 10^{-5}	10	µA
I_{IL}	Input Leakage Low (no pull-up)	$V_{IN}=V_{SS}$, V_{DD}=1.8 V	-10	-1 x 10^{-5}		µA
I_{OZ}	Output Leakage (no pull-up)	$V_{IN}=V_{DD}$ or V_{SS}, V_{DD}=3.6 V	-10	1 x 10^{-5}	10	µA
I_{OS}	Output Short Circuit Current (3 x Buffer)(2)	V_{DD}=1.8 V, $V_{OUT}=V_{DD}$ V_{DD}=1.8 V, $V_{OUT}=V_{SS}$	5 -60	25 -25	60 -5	mA mA
V_{IL}	CMOS Input Low Voltage				0.2 x V_{DD}	V
V_{IH}	CMOS Input High Voltage		0.8 x V_{DD}			V
V_T	CMOS Switching Threshold	V_{DD}=1.5 V, 25°C		0.75		V
V_{OL}	Output Low Voltage Output buffer has 12 stages of drive capability with 0.5 mA I_{OL} per stage.	I_{OL}=as rated V_{DD}=1.5 V			0.2 x V_{DD}	V
V_{OH}	Output High Voltage Output buffer has 12 stages of drive capability with -0.5 mA I_{OH} per stage.	I_{OH}=as rated V_{DD}=1.5 V	0.8 x V_{DD}			V
I_{DD}	Static Current Input Leakage Low (no pull-up)	1.0 V 3.0 V		< 75 < 1.0		nA µA

Note: 2. This is the specification for the 3 x Output Buffer. Output short circuit current for other outputs will scale accordingly. Not more than one output shorted at a time, for a maximum of one second, is allowed.

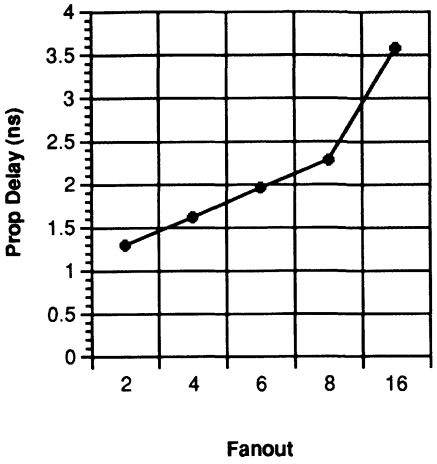
AC Characteristics

Delay vs V_{DD}



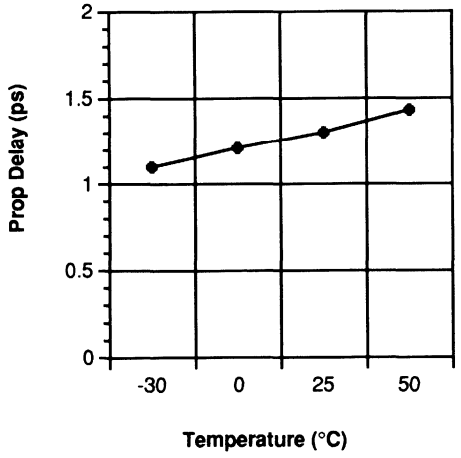
NAND2 - 2 input NAND
Temp = 25°C
FO = 2

Delay vs Fanout



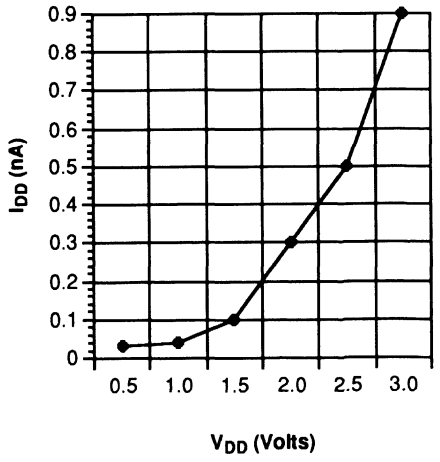
1.5 Volts V_{DD}
NAND2 - 2 input NAND
Temp = 25°C

Delay vs Temperature



1.5 Volts V_{DD}
NAND2 - 2 input NAND
FO = 2

Current Drain vs Voltage



Temp = 25°C

I/O Buffer DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Capacitance Input Buffer (Die)	1.5 V		2.4		pF
C_{OUT}	Capacitance Output Buffer (Die)	1.5 V		5.6		pF
$C_{I/O}$	Capacitance Bi-Directional	1.5 V		6.6		pF

I/O Buffers

- Programmable output drive
  0.5 to 6 mA I_{OL}, -4.5 to -6 mA I_{OH} for 1.5 V)
- 3000 volts ESD protection

The ATLV series input/output ring contains the I/O buffer circuitry capable of sourcing and sinking currents up to 6 mA, and responds to CMOS logic levels. I/O locations on this ring can accommodate bidirectional cells.

Design for Testability

Atmel supports a full range of Design-for-Test improvement techniques which reduce design and prototype debug time, production test time, and board & system test time. These techniques can also improve system level test and diagnostic capability.

The ATLV arrays support the Joint Test Action Group (JTAG) boundary scan architecture. The required soft and hard macros to implement IEEE 1149.1 compliant architecture are available in our macro cell library. Use of JTAG allows for scan testing with only 4-5 additional pins required.

Atmel can also provide automatic high fault coverage test pattern generation (ATPG) via Synopsys Test Compiler.

By following a set of design rules, Test Compiler can automatically insert the scan cells and generate test vectors providing greater than 95% fault coverage. This is the easiest and least expensive method for designing testability into a gate array design.

Advanced Packaging

Atmel supports a wide variety of standard packages for the ATLV series, but also offers its ATLV series gate arrays in packages that are custom designed to maintain the performance obtained in the silicon. All of Atmel's standard packages have been characterized for thermal and electrical performance.

When a standard package can't meet a customer's needs, Atmel's package design center can develop a package to precisely fit the application. The company has delivered custom-designed packages in a wide variety of configurations, including Tape Automated Bonding (TAB) packages. Atmel's domestic packaging facility manufactures commercial, industrial and Class B.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128, 132, 144, 160, 184, 208, 240, 304
TQFP	44, 48, 52, 64, 80, 100, 120, 128, 144, 160, 176, 216
PLCC	20, 28, 32, 44, 52, 68, 84
CPGA	64, 68, 84, 100, 124, 144, 155, 180, 223, 224, 299, 391
CQFP	64, 68, 84, 100, 120, 132, 144, 160, 224, 340
BGA	121, 169, 225

Introduction

The Atmel flexible design approach allows the customer to develop a database compatible with our design flow through a number of different design methodologies.

The traditional design approach involves capturing a schematic and running logic simulation using an Atmel macrocell library and an EDA CAD workstation. Atmel provides comprehensive libraries for the major EDA software systems. The current versions supported, as well as the platforms are shown in the Design Tools table on the following page.

In addition to the macrocell libraries Atmel also provides several proprietary utility software packages. Our Netlist Checker, v3, will perform checks for common design errors and potential problems, as well as calculate power and gate count. Incorporated in v3 is our Slew Rate Delay Calculator (SRDC). The SRDC provides an interface with the simulators for very accurate timing analysis. SRDC has both pre-route and post-route back annotation capability. Atmel also provides our Test Vector Checker (tvc) which checks the test vectors to ensure that they are in the proper format and can be quickly converted into a test program.

Increasingly, designs are being done through logic synthesis. In this method an HDL (VHDL or Verilog-HDL) description of the logic is synthesized into a gate level description utilizing Atmel macro cells. Resulting netlists are then simulated in a manner similar to the schematic capture approach. Benefits of this approach include more structured design, better adherence to design rules; and, therefore, a shorter overall design cycle. Logic synthesis also simplifies the task of scan insertion and ATPG.

Gate Array Design

Atmel Design Tools

System	Version	Simulator and Schematic Capture	Netlist Checker	Test Vector Checker	Delay Calculator/ Back Annotation	Computer
Cadence/Composer	1.3 2.0 4.2	Veritime/ Verilog-XL/ Composer	v3	tvc	Yes	Sun 4, HP
Viewlogic	5.1-PC 5.3-Sun	ViewSIM, ViewDRAW ViewSIM, ViewDRAW	- v3	tvc tvc	Yes Yes	386/486/Pentium™ Sun 4
Mentor	8.2	QuickSIM II, Neted	v3	tvc	Yes	Sun 4, HP
Synopsys	3.2	Test Compiler, Synthesis and VHDL Simulation			Yes	Sun 4,HP

Another design approach is translation of an existing gate array or standard cell design into an Atmel gate array. Using design translation, Atmel can deliver a pin-for-pin compatible drop-in replacement, a gate array with improved performance or even combine several designs into one. For this approach Atmel requires a detailed database of the original design including a specification netlist, vectors and post-route timing. A checklist of the data required to achieve database acceptance is in the ASIC translation design approach section later in this chapter. After translating the design into an Atmel cell library, Atmel can provide a netlist in Cadence™, Mentor™, Synopsys™ or Viewlogic™ format for simulation and verification at the customer's facility. It should be emphasized that this approach still requires the customer to review and approve the performance of the Atmel gate array.

Conversion of FPGA/PLD designs into a gate array is also a common approach. Prototype designs can be verified with a programmable device, and then converted into a gate array for production. As with an ASIC design translation, Atmel can deliver a pin-for-pin compatible drop-in replacement, a gate array with improved performance (speed), or combine several FPGA/PLD into a single gate array. Atmel has successfully combined up to 18 FPGA/PLD into a single gate array. A detailed database including test vectors is required. Like an ASIC translation, this approach requires the customer to review and approve the performance of the Atmel gate array.

Design Flow

Atmel's design flow has four major milestones independent of the design methodology used:

Database Acceptance
Preliminary Design Review
Final Design Review
Prototype Delivery

Atmel has defined specific requirements for each milestone that must be accomplished.

Database Acceptance (DA)

At this milestone Atmel formally accepts the design database as complete and begins work on the design. At DA Atmel will verify that the complete database has been received, confirm that there are no known errors (netlist checker and test vector checker) and insure that the netlist, vectors, etc., are all in the correct format.

It is critical that all the required data elements are submitted at one time in the correct format and that the database is final (no anticipated changes). Completion of DA marks the start of the Atmel design cycle.

Database Summary
- -Flat netlist
- -Test Vectors (TV) per Atmel's Test Vector Checklist (tvc)

Documentation
- -Report from v3 Netlist Checker
- -Report from tvc
- -Timing Diagram (clocks, vectors applied, vectors sampled)
- -Critical paths
- -System load

A detailed database acceptance checklist for each of the four design flows (Cell Library, ASIC Translation, FPGA/PLD Conversion and Design Synthesis) provides the designer with the exact requirements. Copies of the checklists are located at the end of this design section.

Preliminary Design Review (PDR)

After DA Atmel will migrate all designs into the Cadence Design System. Atmel uses Cadence's Verilog-XL™/Veritime™ as our golden simulator, and all designs are signed-off based on the Cadence results. The submitted design is ported to Verilog and re-simulated using the customer supplied vectors. Functional performance is verified as well as key timing performance. Once this has been successfully completed, a PDR is held between Atmel and the customer to agree upon the performance level of the gate array. Following are the requirements for PDR:

Confirm v3 file correct
Confirm tvc file correct
I/O buffer listing and bonding diagram
Preliminary testability compiler report (optional) indicating areas that may not be covered
Clock tree approach and timing requirements
Verilog simulation - preferably, at speed
- -worst case, best case
- -review clock timing
- -at-speed
- -clock skew (if required)
- -listing of timing warnings with explanation

Review critical path information (tSU, tHOLD, tPD)
Verilog or Veritime estimates
I/O electrical including SSO (Simultaneous Switching Output)
Electromigration calculation pre-FDR

Physical Design

Once PDR has been successfully completed and the circuit has been fully simulated and evaluated for compliance to the specification and performance goals, the netlist is moved into the physical design phase. Currently Atmel uses the Cadence physical design tools to accomplish place and route. This is where each instance of each macro cell is physically placed in the array and then connected together (routed) per the schematic. After place-and-route, the design is re-simulated in Verilog-XL to incorporate the effects of parasitic capacitance networks associated with the double metal routing of the physical design (back annotation data). These effects will already have been anticipated in the initial simulations by the customer and by Atmel, since a typical

parasitic capacitance loading will have been supplied with the cell library timing models. Therefore, performance changes between pre- and post-route simulation results are minimal.

Back Annotation or Post-Route Simulation

The router does an extraction of timing related data - either by creating a delay report or an RC report. The delay report allows for an immediate static-path timing analysis, while the RC report allows data to be exported back to the baseline simulator, Verilog-XL, to confirm that the previously incorporated estimates for parasitic RC associated with placement and routing were accurate.

The timing performance of the circuit is updated at this time with the customer prior to going to silicon fabrication. The post-route simulation is done with customer supplied load conditions and with the Automatic Test Equipment ATE load conditions so that a test specification can also be signed off at FDR. A back annotation report will be provided to the customer in the supported design systems. This will give the customer the most accurate timing information possible.

Design Verification

Part of Atmel's design flow is the design verification of the completed design. This includes Design Rule Checking (DRC) to verify the design meets the detailed CMOS mask design rules for the fabrication process. Layout Versus Schematic (LVS) is run to guarantee that the routed design matches the final simulation netlist.

The base array and cell library have already been through this checkout procedure and have been verified in silicon using test vehicles containing cells from the Atmel libraries. It is necessary to verify that the personalization levels accurately reflect both the customer functional circuit and the CMOS process design rules before masks are made. The results of these verification steps are available at the FDR for customer sign-off. Together with the extensive timing analysis, verification guarantees to the customer that prototype parts will meet the specification.

Final Design Review (FDR)

The Final Design Review is the last joint review between Atmel and the customer before committing to prototypes. Prior to the meeting both Atmel and the customer will have reviewed the post-route Verilog-XL simulations. Below are the requirements for FDR.

Confirm that v3 and tvc files are correct
- -post-route netlist changes

I/O buffer listing and bonding diagram
Testability report
Clock tree and analysis of worst case and best case delay
Verilog simulation - with back annotation data
Worst case, best case (with no timing violations)
- -review clock timing
- -at-speed
- -clock skew (if required)
- -listing of time warnings with explanation

Review critical path information (tSU, tHOLD, tPD)
- -Verilog or Veritime results

I/O electrical
Electromigration calculation
Ground bounce analysis
LVS/DRC

Prototype Delivery

After FDR has been successfully completed, and the FDR approval form signed by the customer, a PG tape is released to the mask shop. Atmel will deliver 10 prototype units in ceramic packages to the customer. These units will be functionally tested at room temperature, the purpose of the units is to verify the design's functionality and electrical performance. Prior to starting any production or pre-production wafer, Atmel must receive a signed Prototype Approval form from the customer.

Cell Library Design Approach

The traditional approach to designing ASICs is for the customer to perform schematic capture of the logic diagram using a CAE workstation that has the ASIC supplier's symbols and timing libraries resident on the computer (see Figure 1). The customer is required to perform schematic entry, test vector generation and functional simulation. Atmel uses Verilog-XL as our golden simulator, however, other simulators are also supported.

Atmel provides several utility software programs to assist the customer in the design process. The v3 netlist checker, checks the netlist for common design errors and potential problems. v3 also provides an accurate gate count for the design and can provide preliminary power consumption information. An error free v3 report is a requirement for meeting each of the 3 design milestones, DA, PDR, and FDR. v3 comes with a complete installation and usage manual. For more specific details see these documents.

Incorporated in v3 is Atmel's Slew Rate Delay Calculator (SRDC). The SRDC is a highly accurate analysis tool which interfaces with the supported simulators. SRDC provides both pre and post route delay calculations.

Atmel SRDC incorporates slew rate correction. The time for each cell accounts for the effect of the cell driving it. The output delay from the driving cell is propagated into the next cell affecting both the rising and falling slope. In submicron design it is particularly important to account for this effect.

The SRDC also has a Module Input Port Delay (MIPD) feature. This allows the capacitance to be distributed on cells with multiple fan outs. This provides a more accurate timing than the traditional lump capacitance method. In addition, the SRDC provides individual deratings (process, temperature, and voltage)

Atmel Cell Library Design Flow

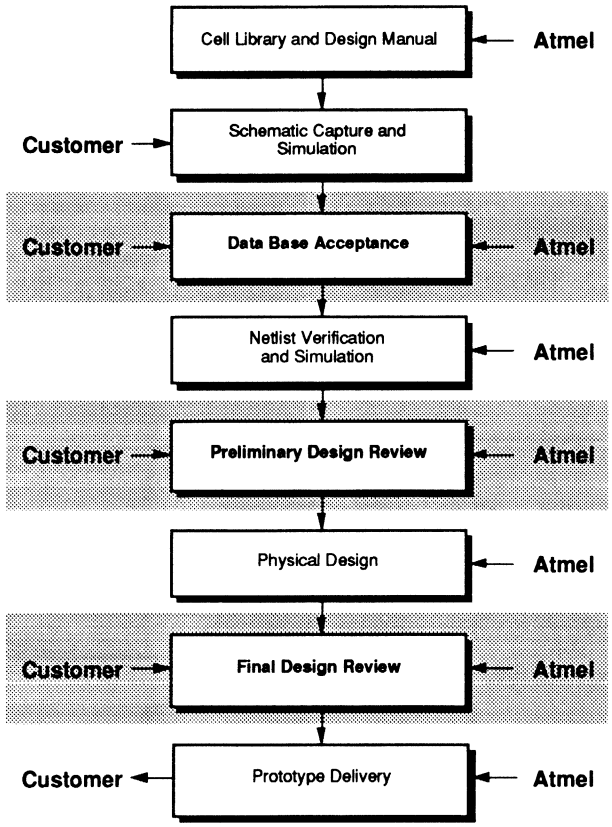


Figure 1

for each cell, the ability to handle mixed voltages and comes with an SDF interface.

Atmel's tvc test vector checker checks the customer vector set for conformance to Atmel's vector format rules. However, tvc does not produce vectors, or check for fault coverage. It's primary purpose is to ensure the vectors are received in correct and consistent format. This is especially critical for the vector sets which will be used to generate the production test program. Problems with vectors are the most common cause of delays in the gate array design cycle. The designer should thoroughly read the Test section of this design manual, in particular the Customer Test Application Checklist and the Test System Formatting sections. The required elements for Database Acceptance of a cell library design are detailed in the checklists located at the end of this section.

It is recommended that before starting a design, the customer thoroughly read the Design for Testability section in this manual. Many problems with simulation, verification and test can be prevented by incorporating good testability techniques up front. In particular, generation of a sufficient number of vectors to achieve a desired level of fault grading (95%) can be extremely time consuming if proper design techniques are not used.

ASIC Translation Design Approach

Atmel's ASIC translation design process, Figure 2, is structured to reqiured minimum engineering resources from the customer, provided the requisite design database is received. The requirements for achieving database acceptance are listed in the checklist located at the end of this section.

The first step toward meeting DA is the submission of the design database to Atmel. If all required elements for DA are present the design database can quickly be accepted. Frequently issues arise in the vector format (or another element) or with missing items which require some work to be done to meet DA. Because Atmel can never be certain as to what type of database will be received from the customers, all schedules for the design use DA as the starting point. In other words, the clock starts once DA has been met.

Once data base acceptance has been met, the netlist is read into Synopsys. Using Synopsys, each cell of the original design is mapped into an equivalent cell in the Atmel cell library. Atmel defines an equivalent cell as one having not only the same function, but the similar speed as the original cell. Sometimes more than one Atmel cell is required. For instance, if the original design was implemented in 1.2µ CMOS, added delays may be required to match the timing of the original cell to avoid race conditions. By matching the timing of each individual cell as closely as possible, time consuming modifications of the design at the netlist level are avoided.

If performance needs to be improved in a particular area, Atmel will address this issue before the Preliminary Design Review. For instance, several cells in the original design may have been used to construct a particular register. To improve performance, Atmel may elect to implement the register as a hard macro. In parallel with the mapping of the netlist, the functional simulation vectors are translated into Atmel format.

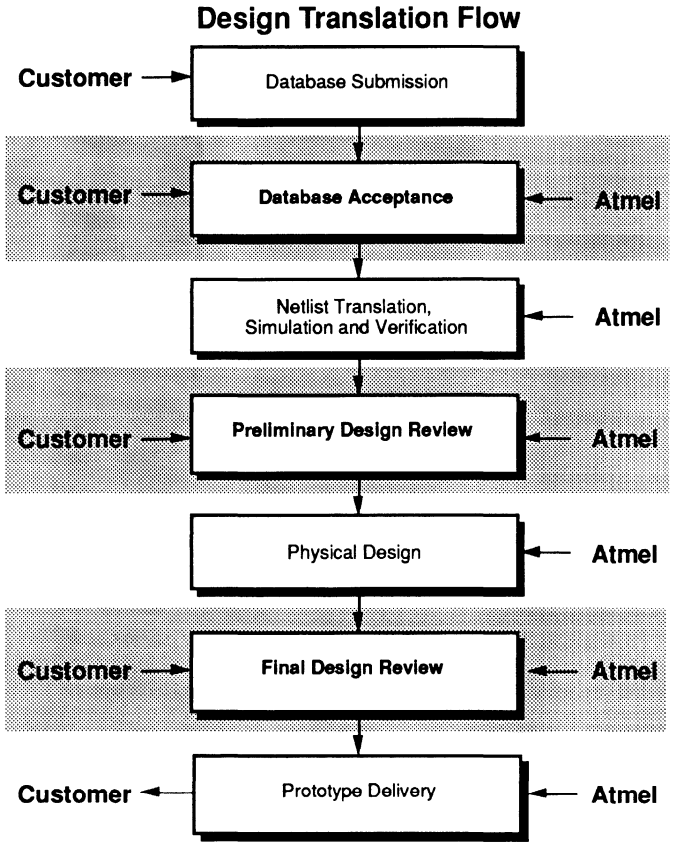


Figure 2

Verifying Performance

The new netlist and translated vectors are used to perform functional simulation. Atmel uses Cadence's Verilog-XL as its "golden simulator." The first step in verification is running the functional simulation vectors. Once functionality has been established, timing verification begins. Atmel will again use Verilog-XL to run the functional vectors at system speed over worst case environmental conditions (voltage and temperature). This can be done for commercial, industrial or military applications. Increasing clock frequency to failure (Fmax) can also provide a measure of design margin. This is performed by running functional vectors in strobe format, rather than print-on-change format.

The timing performance of the original device, either via simulation or Atmel characterization of the sample part, is used for a direct comparison. Atmel performs a waveform comparison of the timing. The system can be programmed to compare timing and report any difference. The net with a greater than desired timing difference can then be sped up or slowed down to meet specification. At this point, Atmel works with the customer to improve performance of a given critical path or to give greater design margin. Veritime, another Cadence design tool, can be used to verify critical paths (input to register, register to register and register to output) for which timing specifications exist. As a path trace tool, Veritime will identify timing for all paths on the chip, independent of test vectors.

There are other timing-critical simulations that can be run. Pulse width checks on the clocked elements and glitch detection can be performed to ensure proper latch and register transfers after routing. SPICE simulation of the I/O buffers can be run to ensure a match with the switching characteristics. In addition, the clock latency, input set-up times, input hold times and clock-to-output delays can be compared to the original design to ensure there are adequate design margins.

FPGA/PLD Conversion Design Approach

The Conversion Process Summary

Atmel's conversion process is designed to minimize the amount of engineering support required from the system designers. Figure 3 outlines the conversion process flow. The inputs required vary depending on the original manufacturer of the FPGA/PLD. Atmel's FPGA/PLD conversion design process is structured to require minimal engineering resources from the customer, provided the requisite design database is received.

The first step toward meeting DA is the submission of the design data base to Atmel. If all required elements for DA are present, the design datebase can quickly be accepted. Frequently issues arise with format of the vectors (or another element) or with missing items which require some work to be done to meet DA. Because, Atmel can never be certain what type of data base will be received from the customers, all schedules for the design use DA as the starting point. In other words, the clock starts once DA has been met. Once Atmel datebase acceptance has been met, the original design is converted into an equivalent netlist using the Atmel cell library. The equivalent netlist ensures that both the functionality and timing of the new design match the original. Using this technique, almost any FPGA/PLD design can be converted to a gate array.

The original test vectors are also converted and are used to verify the gate array design. Good functional vectors must be provided or developed. This is important because the functional test vectors are the verification vehicle for the design. After the design has been converted and verified for functional performance, the optimization process begins. The design can be optimized to match the timing performance of the original FPGA/PLD design or to meet new performance goals. Additional logic functions or memory can be added to the gate array as well.

Before physical design of the chip begins, a joint Preliminary Design Review is held with Atmel and the customer to approve the results of the converted design. From this point on, the design process is identical to that of a traditionally designed gate array. The design is physically placed and routed on the gate array and verified for electrical and design rules. Atmel uses Cadence's Verilog-XL™ as a golden simulator. Atmel guarantees performance equal to or better than that predicted by Verilog-XL post route simulation.

Back annotation data is extracted from the actual layout and incorporated into the post-route functional and timing simulation. Minor layout modifications may be required to meet the timing specification. A Final Design Review is held to approve the post-route simulation data. After customer approval, the design is released for mask generation and prototyping. Prototypes can be delivered in as little as three weeks and production units in as short as six weeks after customer approval of prototypes. Atmel guarantees the gate array will be a pin-for-pin compatible replacement for the FPGA/PLD.

The exact database requirements for each type of FPGA/PLD are detailed in the checklist located in the appendix at the end of this section.

FPGA/PLD Conversion Flow

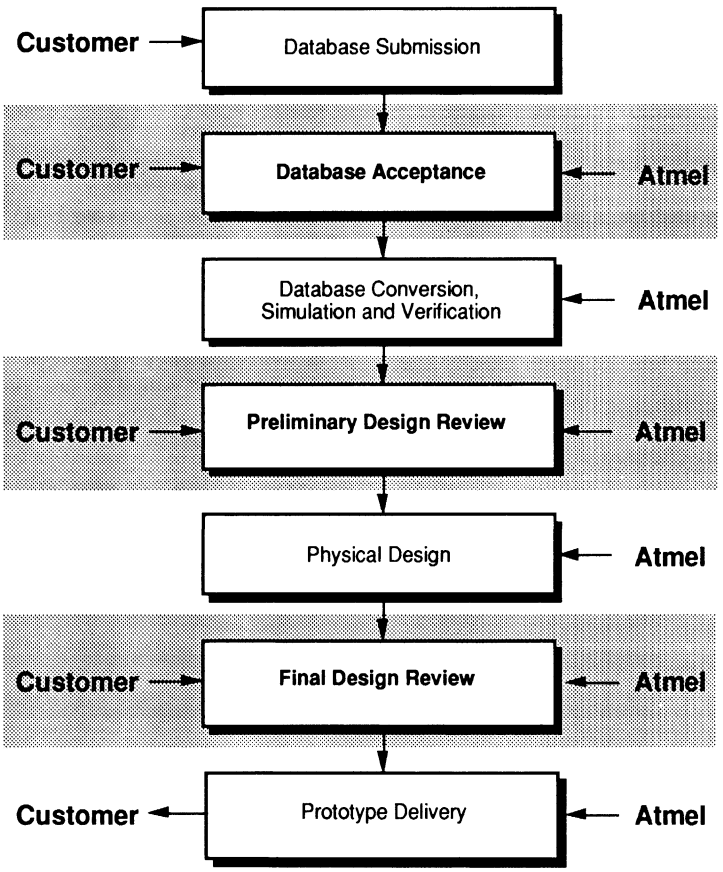


Figure 3

Design Synthesis Design Approach

Atmel can accept HDL level inputs in either VHDL or Verilog-HDL languages, see Figure 4, incorporating behavioral, data flow and structural level language constructs. Atmel uses Synopsys to perform design synthesis, translation from RTL design to a netlist, and design optimization. Atmel will also use Synopsys' Test Compiler to develop a set of functional vectors for simulation and test. If a customer has Synopsys CAE tools, Atmel can provide a timing library and the customer can perform design synthesis. The input to Atmel would then be a netlist and test vectors.

After netlist simulation on Verilog-XL™, the PDR will be held. At PDR the gate-level netlist, simulations and test vectors will be reviewed and agreed to by both parties.

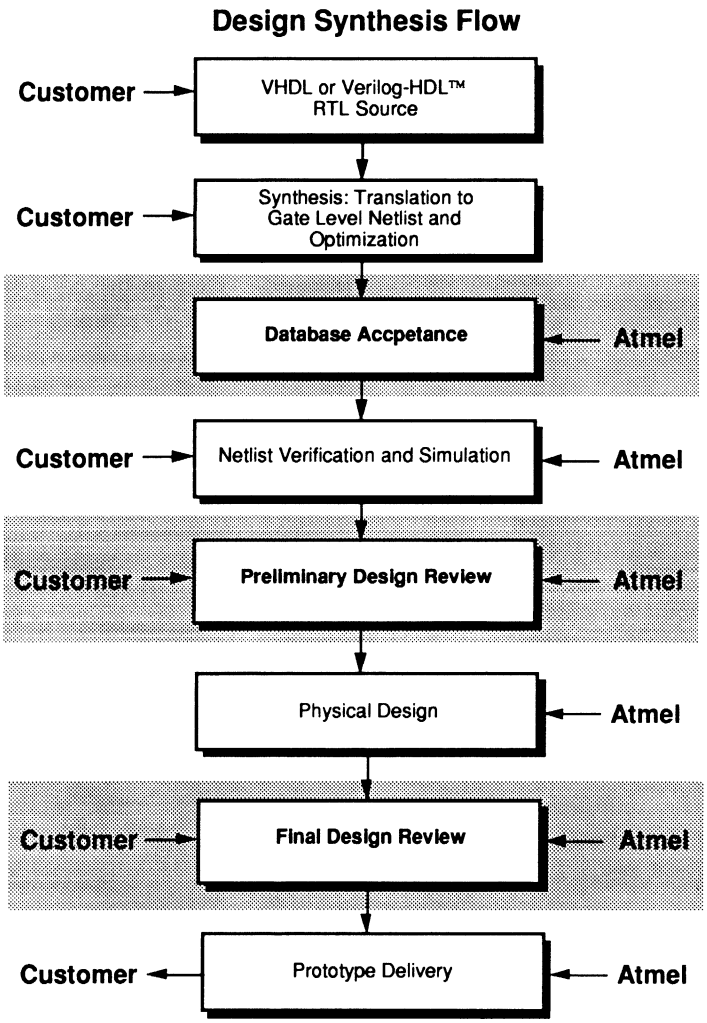


Figure 4

Gate Array Design Flow

Atmel's design flow has four major milestones independent of the design interface used.

Database Acceptance
Preliminary Design Review
Final Design Review
Prototype Delivery

Atmel has defined specific requirements for each milestone that must be accomplished prior to moving on in the design flow.

Database Acceptance (DA)

At this milestone Atmel formally accepts the design database as complete and begins work on the design. At DA Atmel will verify that the complete database has been received, there are no known errors (netlist checker and test vector checker) and that the netlist, vectors, etc. are all in the correct format.

It is critical that all the required data elements are submitted at one time in the correct format and that the database is final (no anticipated changes).

Database Summary
Flat netlist (at level netlist if test compiler will be used)
TV's per Atmel's test vector checklist

Documentation
- v3 Netlist Checker Report
-Test Vector Checker (tvc) Report
-Timing Diagram (clocks, vectors applied, vectors sampled)
- Critical Paths
- Best/Worst Case Conditions
- System Loading Requirements
- Purpose of TV Sets

A detailed database acceptance checklist, for each of the four design flows (cell library, ASIC translation, FPGA/EPLD conversion and VHDL/Verilog-HDL) provides the designer with the exact requirements.

Preliminary Design Review (PDR)

After DA, Atmel will migrate all designs into the Cadence Design System. Atmel uses Cadence's Verilog-XL/Veritime as our golden simulator and all designs are signed off based on the Cadence results. The submitted design is ported to Verilog and re-simulated using the customer supplied vectors. Functional performance is verified as well as key timing performance. Once this has been successfully completed, a PDR is held to agree upon the performance level of the gate array. Following are the requirements for PDR:

Confirm v3 and tvc files correct
I/O buffer listing and bonding diagram
Preliminary testability compiler report
Route clock tree and analysis of worst case and best case delay
Verilog simulation at-speed
-nominal, worst case, best case (with no timing violations)
Review critical path information (t_{SU}, t_{HOLD}, t_{PD})
-Verilog or Veritime estimates
I/O electrical specifications
Electromigration calculation

Final Design Review (FDR)

The Final Design Review is the last joint review between Atmel and the customer before committing to prototypes. FDR is basically a re-review of PDR. Prior to the meeting both Atmel and the customer will have reviewed the post-route Verilog-XL simulation incorporating the back annotation data. The customer will receive back annotation data for complete post-route simulation on their CAE systems. Atmel guarantees silicon performance equal to or better than predicted on the post-route Verilog-XL simulations. Below are the requirements for FDR.

Updates of cell mapping and timing (if any)

Post-route netlist check v3, tvc
-post-route netlist changes
Post-route timing simulation to specification
-review clock timing
-at speed
-clock skew (if required)
-listing of timing warnings with explanation

Static path analysis (as specified)
Electromigration Calculation
Bonding diagrams and pin list
-bond pad plot

LVS/DRC/ERC

Prototype Delivery

Atmel will deliver 10 prototypes in ceramic packages to the customer. The purpose of the units are to verify the design's functionality and electrical performance.

Gate Array Database Acceptance Checklist - Atmel Cell Library

Design Checks

The netlist must be in one of the following formats:

_____ EDIF™ 2.0.0

_____ Cadence™Verilog™ structural netlist

_____ Viewlogic™ wirelist files

_____ Synopsys™ .db

Atmel provides a software program, the v3 Netlist Checker, which checks the customer netlist for errors and potential design problems. The netlist must pass the Atmel v3 Netlist Checker for Digital ASIC. The customer is required to submit a v3 report with the design database.

v3 Checks (See the v3 manual for the complete list of checks)

_____ No Q → D for flip-flops driven by the same clock

_____ No rise/fall delays greater than 2.5 ns

_____ No floating inputs

_____ All internal Tri-state™ nets have HLD cells on them

_____ No "confused" nets

_____ Chip fits on target array (discuss the percent of utilization with an Atmel engineer)

_____ No mixed pads

_____ Electromigration checked at _____ MHz

_____ No net aliasing problem

_____ All parallel cells are intentional

Gate Array DA Checklist - Atmel Cell Library

Simulation/Test Vector Format

The simulation/test vectors are the most difficult aspect of a design. This is often because they are poorly understood or poorly communicated in the DA phase of the design. Atmel provides a software program, Test Vector Checker (tvc), to check the vectors for format errors and potential problems.

The general format of ASCII vectors is 1 vector per line, with a timestamp in the left column. When there are bidirectional signals, the vector set must define when the signal is an output and when it is an input. These and other requirements are discussed in the manual for the tvc.

_____ There are _____ vector sets.
_____ All vector sets pass all the tvc program (Report attached.)
_____ The production parts will be verified using ATPG vectors.

Vector requirements:

_____ All vectors have a stated purpose and are in an identical format; input, output, Tri-state™, bidirectional and enable.
_____ Outputs are sampled once per clock cycle. Atmel recommends strobing at the 75% cycle point.
_____ Test vectors must have a 1 MHz set for probe and an at-speed set for final test.

The simulation/test vector tape must be in one of the following formats:

_____ Mentor™ QuickSIM™, include the following file:
    _____ .LIST files (strobed and print on change format)

_____ Cadence Verilog™ vectors, include the following files:
    _____ Fixture file
    _____ All pattern files
    _____ 1 print on change file for each vector set containing all of the I/O and Tri-state™ enables

____ Viewlogic™, include the following files:
    _____ ASCII vector files; 1 print on change file for each vector set containing all of the I/O and Tri-state™ enables
    _____ .CMD file

Gate Array DA Checklist - Atmel Cell Library

Design Documentation and Specifications

The design documentation must include ALL of the following:

_____ Verify Atmel Device Definition List (DDL) [Atmel task].
_____ The design contains RAM blocks (list RAMs used).
_____ A diagram showing the distribution of each clock with all instance and net names clearly visible is included. Frequencies and latencies are defined for each clock.
_____ A timing diagram showing the relationship of all clocks, input vector transition points and output sample points is included.
_____ Data pages showing all timing requirements are included (must show min/max times and full instance path).
_____ Explicit documentation detailing any special timing requirements (must show minimum and maximum times and full instance path).

Gate Array Specification

_____ I/O and packaging requirements are included.
_____ Package pin list (Showing I/O and pwr/gnd pins) is included.
_____ Verify correct number of pwr/gnd pins to prevent pwr/gnd bounce and proper shunt protection for I/O pads.
_____ I/O list showing pad type and system loads is included.
_____ Package markings are defined.
_____ List any other special considerations.

System operating voltage:

_____ 5v operation
_____ 3v operation
_____ Other _____
_____ Mixed voltage operation; simultaneous multiple power supplies. See the ATL80 Series Gate Array Mixed Voltage Application Note
_____ Either 3v or 5v operation on the same die (no mixed voltage).

Simulation/characterization conditions:

_____ Use system loads in simulation (must pass with tester loads).
_____ Voltage: ±10%, ±5%
_____ Temperature: -55 °C, 0 °C, 70 °C, 125 °C _____Other (Select minimum and maximum)

Gate Array DA Checklist - ASIC Translation

When Atmel accepts a gate array design that uses a macrocell library, other than our gate array library, we must map all cells from the source library into our library. This is usually done by adding a level of hierarchy which has a definition for all of the cells used from the source library. These definitions are in terms of Atmel gate array cells. This mapping preserves the structure (instance and signal names) of the design.

Design Database Format

The netlist must be in one of the following formats:

_____ EDIF™ 2.0.0

_____ Cadence Verilog™ structural netlist

_____ Viewlogic™ wire list files

_____ Synopsys™ .db files

_____ LSI Logic™ .NDL

Gate Array DA Checklist - ASIC Translation

Simulation/Test Vector Format

The simulation/test vectors are the most difficult aspect of a design. This is often because they are poorly understood or poorly communicated in the DA phase of the design. Atmel provides a software program, Test Vector Checker (tvc), to check the vectors for format errors and potential problems.

The general format of ASCII vectors is 1 vector per line, with a timestamp in the left column. When there are bidirectional signals, the vector set must define when the signal is an output and when it is an input. These and other requirements are discussed in the manual for the tvc.

_____ There are _____ vector sets.
_____ All vector sets pass all the tvc program (report attached).
_____ The production parts will be verified using ATPG vectors.

Vector requirements:

_____ All vectors have a stated purpose and are in an identical format; input, output, Tri-state™, bidirectional and enable.
_____ Outputs are sampled once per clock cycle. Atmel recommends strobing at the 75% cycle point.
_____ Test vectors must have a 1 MHz set for probe and an at-speed set for final test.

The simulation/test vector tape must be in one of the following formats:

_____ Mentor™QuickSIM™, include the following files:
  _____ .LIST files (strobed and print on change format)

_____ Cadence Verilog ™ vectors, include the following file:
  _____ Fixture file
  _____ All pattern files
  _____ 1 print on change file for each vector set containing all of the I/O and Tri-state enables

_____ Viewlogic™, include the following files:
  _____ ASCII vector files; 1 print on change file for each vector set containing all of the I/O and Tri-state enables
  _____ .CMD file

_____ LSI Logic™ LSIM, include the following files:
  _____ All LSIM files
  _____ A print on change for all of the I/O

Gate Array DA Checklist - ASIC Translation

Design Documentation And Specifications

The design documentation must include ALL of the following:

_____ Verify Atmel Device Definition List (DDL) [Atmel task].
_____ The design contains RAM blocks (list RAMs used).
_____ Detailed description of the source library (logic symbols, truth tables, timing numbers, drive strengths, ...) is included.
_____ As routed delay of original design is included.
_____ Full hierarchical schematics are included.
_____ A diagram showing the distribution of each clock with all instance and net names clearly visible is included. Frequencies and latencies are defined for each clock.
_____ A timing diagram showing the relationship of all clocks, input vector transition points and output sample points is included.
_____ Explicit documentation detailing, any special requirements (must show minimum and maximum times and full instance paths).

Gate Array Specification

_____ I/O and packaging requirements are included.
_____ Package pin list (showing I/O and pwr/gnd pins) is included.
_____ Verify correct number of pwr/gnd pins to prevent pwr/gnd bounce and proper shunt protection for I/O pads.
_____ I/O list showing pad type and system loads is included.
_____ Package markings are defined.
_____ List any other special considerations.

System operating voltage:

_____ 5v operation
_____ 3v operation
_____ Other _____
_____ Mixed voltage operations; simultaneous multiple power supplies. See the ATL80 Series Gate Array Mixed Voltage Applicatin Note
_____ Either 3v or 5v operation on the same die (No mixed voltage)

Simulation/characterization conditions:

_____ Use system loads on simulation (must pass with tester loads)
_____ Voltage: ±10%, ±5%
_____ Temperature: -55 °C, 0 °C, 70 °C, 125 °C Other _____
(Select minimum and maximum)

REV 2.0-3/95

Gate Array DA Checklist - FPGA/PLD Conversions

When Atmel accepts a FPGA or PLD design for conversion, the first step is to map the FPGA/PLD cells into our library. Atmel requires a set of simulation/test vectors, and the vectors must cleanly run our Test Vector Checker (tvc). Atmel can combine several FPGA/PLD designs into a single gate array for X into 1 conversion. Atmel requires a database vector for the individual designs as well as top level vectors and schematics for the combined design.

Design Database Format

_____ EDIF™ 2.0.0

_____ Cadence™Verilog™ Structural netlist

_____ Viewlogic™ wire list files

_____ Synopsys™ .db files

_____ Altera™ .RPT files

5

Gate Array DA Checklist - FPGA/PLD Conversions

Simulation/Test Vector Format

The simulation/test vectors are the most difficult aspect of a design. This is because they are often poorly understood or poorly communicated in the DA phase of the design. Atmel provides a software program, Test Vector Checker (tvc), to check the vectors for format errors and potential problems.

The general format of ASCII vectors is 1 vector per line, with a timestamp in the left column. When there are bidirectional signals, the vector set must define when the signal is an output and when it is an input. These and other requirements are discussed in the manual for the tvc.

_____ There are _____ vector sets.
_____ All vector sets pass all the tvc program (report attached).
_____ The production parts will be verified using ATPG vectors.
_____ Both top-level and individual vectors exist (for X into 1 conversions).

Vector Requirements:

_____ All vectors have a stated purpose and are in an identical format, input, output, Tri-state™, bidirectional and enable.
_____ Outputs are sampled once per clock cycle. Atmel recommends strobing at the 75% cycle point.
_____ Test vectors must have a 1 MHz set for probe and an at-speed set for final test.

The simulation/test vector tape must be in one of the following formats:

_____ Mentor ™QuickSIM™, include the following file:
  _____ .LIST files (strobed and print on change format)

_____ Cadence Verilog ™ vectors, include the following files:
  _____ Fixture file
  _____ All pattern files
  _____ 1 print on change file for each vector set containing all of the I/O and Tri-state enables

_____ Viewlogic ™, include the following files:
  _____ ASCII vector files; 1 print on change file for each vector set containing all of the I/O and Tri-state enables
  _____ .CMD file

Gate Array DA Checklist - FPGA/PLD Conversions

Design Documentation and Specifications

The design documentation must include ALL of the following:

_____ Verify Atmel Device Definition List (DDL) [Atmel task].
_____ Full hierarchical schematics, including top level interconnections for X into 1 conversions.
_____ Provide detailed description of source library.
_____ The design contains RAM blocks (list RAMs used).
_____ A diagram showing the distribution of each clock with all instance and net names clearly visible is included. Frequencies and latencies are defined for each clock.
_____ A timing diagram showing the relationship of all clock, input vector transition points and output sample points).
_____ Explicit documentation detailing any special timing requirements (must show minimum and maximum times and full instance path).

Gate Array Specification

_____ I/O and packaging requirements are included.
_____ Package pin list (showing I/O and pwr/gnd pins) is included.
_____ Verify correct number of pwr/gnd pins to prevent pwr/gnd bounce and proper shunt protection for I/O pads.
_____ I/O list showing pad type and system loads is included.
_____ Package markings are defined.
_____ List any other special considerations.

System operating voltage:

_____ 5v operation
_____ 3v operation
_____ Other_____
_____ Mixed voltage operation; simulations multiple power supplies. See the ATL80 Series Gate Array Mixed Voltage Application Note
_____ Either 3v or 5v operation on the same die (no mixed voltage)

Simulation/characterization conditions:

_____ Use system loads in simulation (must pass with tester loads)
_____ Voltage: ±10%, ±5%
_____ Temperature: -55 °C, 0 °C, 70 °C, 125 °C Other _____
(Select minimum and max)

REV 2.0-3/95

Gate Array Preliminary Design Review (PDR) Checklist

Overview of the PDR

PDR is the design review prior to the start of place and route. Atmel has established this set of checklists to assure that designs don't have any problems that might make placement or routing difficult or impossible. This checklist is completed by the Atmel designer and reviewed by both Atmel and the customer before routing begins.

The Checklist:

_____ All of the DA v3 checks are completed (include a copy in this report).
_____ The logic simulations pass all requested conditions using estimated wire loads.
_____ All timing checks pass all requested conditions using estimated wire loads.
_____ Grouping files have been created for any critical cells or multiple voltages.
_____ There are layouts for all cells.
_____ The diagram showing the distribution of each clock with all instance and net names clearly visible is included (include a grouping of files for the instances on each clock if needed).
_____ Pre-route electromigration calculation has been performed.
_____ I/O bonding diagram has been approved by the customer, and Package Engineering.
_____ Ground bounce analysis has been performed.

Gate Array Final Design Review (FDR) Checklist

Overview of the FDR

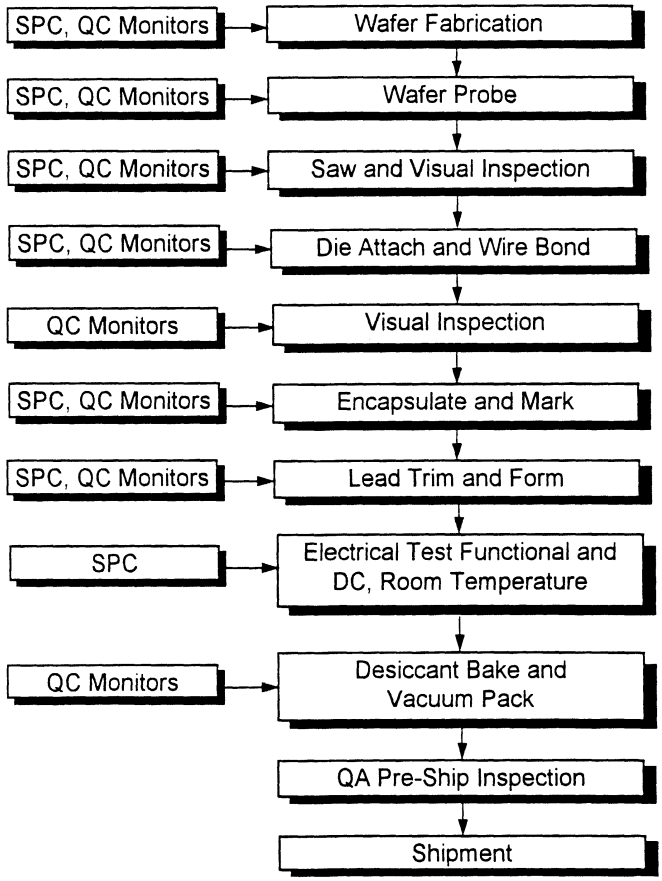
FDR is the design review prior to tape out of design to the mask shop. Atmel has established this checklist to ensure that designs sent to the mask shop have been verified and match the design specifications. This checklist is to be completed by the Atmel designer and reviewed by both Atmel and the customer before the design is released to the mask shop.

The Checklist:

_____ All of the entries on the design folder except the tapeout section have been completed (include a copy in this report).
_____ The logic simulations pass all requested conditions using back annotated wire loads.
_____ All timing checks pass all requested conditions using back-annotated wire loads (Review all critical paths).
_____ The latency of the clock tree has been hand calculated, and a plot from tangate showing the tree is included in this report.
_____ There are layouts for all cells.
_____ All v3 checks have been performed using post layout loads.
_____ Electromigration calculation has been performed.
_____ LVS and DRC checks have been performed.

Digital ASIC

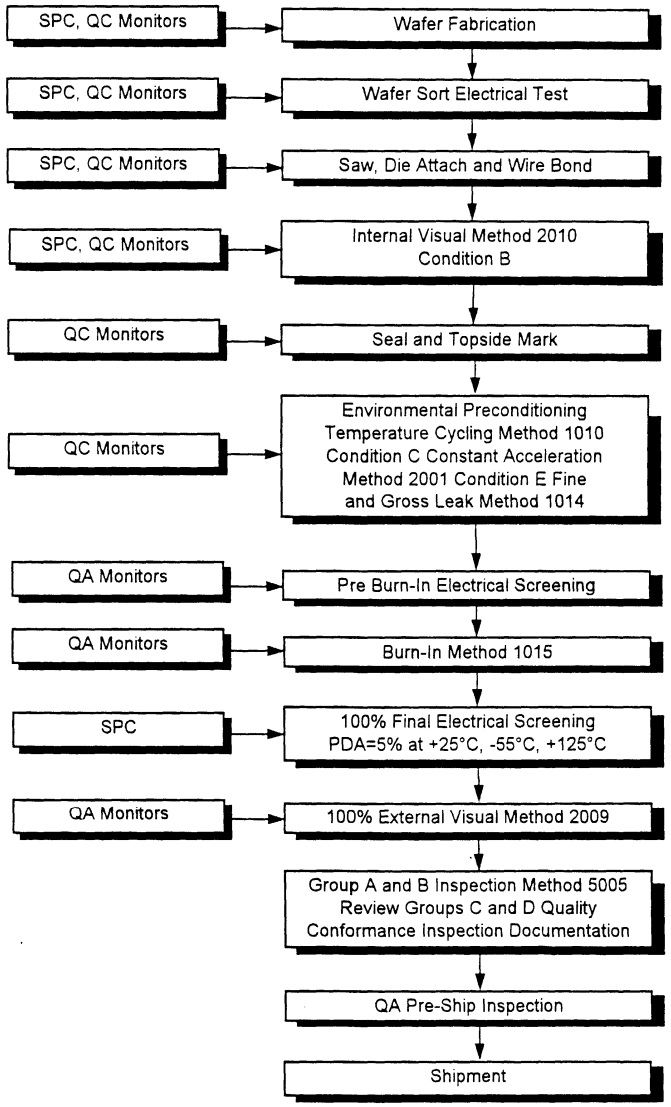
Plastic Package
Commercial Product Flow



REV 2.0-3/95

Digital ASIC

Military Class B Product Flow



REV 2.0-3/95

How to Use This Cell Library Index

The cell index contains the macro cell's timing, size, and loading information. The data included in the cell timing information is explained in detail below.

Cell Parameters

Site Count: Lists the number of gate array cell sites the macrocell occupies. This can be used by the designer to determine what size gate array is required for the design.

Input Load: Lists the number of unit loads the input represents. The number of unit loads is used to determine the propagation delay of the macrocell. This is covered in the timing section.

For initial logic design, a load of less than 12 is recommended. The logic load should be supplemented with estimated wire load (pre-route) or actual back annotated wire load (post-route). With estimated wire loads included, a load of less than 24 is recommended. After routing, a back annotated load of 30 is considered a limit. Loads greater than this will be addressed by inserting higher drive cells, reducing wire load or waiving the violation for a non-critical net (such as an external reset that is neither timing critical nor functionally subject to improper operation due to noise).

Timing

Path Timechk: Shows the path for the associated timing numbers. Path Timechk "A->O" denotes the delay from input A to output O. Path Timechk "D+CLK" denotes the Setup/Hold requirement between inputs D and CLK.

The cell index gives the designer the information needed to calculate the propagation delay based on the number of loads the macrocell is driving. The delay is calculated using the Delay = Intercept + (Slope x Loads) equation where:

- Delay is the total propagation delay.
- Intercept is the base (zero loads) delay.
- Slope is the additional delay per unit load.
- Loads is the number of unit loads (not macrocells) the macrocell is driving.

The number of unit loads each macrocell's input represents is listed under Input Load in the cell index.

74XX Series Soft Macros

Cell Name	Cell Description MSI Part Number	Similar to MSI Part Number
TTL64	4232 And Or Invert	74ALS64
TTL74	DFF	74ALS74
TTL109	JKBar FF	74ALS109
TTL138	3 to 8 Decoder	74ALS138
TTL139	Dual 2 to 4 Decoder	74ALS139
TTL148	8 to 3 Priority Encoder	74ALS148
TTL151	8 to 1 MUX	74ALS151
TTL153	4 to 1 MUX	74ALS153
TTL157	Quad 2 to 1 MUX	74ALS157
TTL158	Quad Inverting 2 to 1 MUX	74ALS158
TTL161	4 BIT Binary Counter	74ALS161
TTL164	8 BIT Serial in Parallel Out Shift Register	74ALS164
TTL166	8 BIT Parallel Load Shift Register	74ALS166
TTL169	4 BIT U/D Counter	74ALS169
TTL174	Hex DFF	74ALS174
TTL194	4 BIT BiDi Shift Register	74ALS194
TTL273	Octal DFF	74ALS273
TTL280	9 BIT Parity Generator	74ALS280
TTL283	4 BIT Fast Adder	74ALS283
TTL688	8 BIT Comparator	74ALS688
TTL823	9 BIT DFF	74ALS823
TTL825	8 BIT DFF	74ALS825
TTL85	4 BIT Magnitude Comparator	74ALS85
TTL86	Quad 2 Input Ex OR	74ALS86

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Macrocells in alpha-numeric order

Signal Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
ADD3X	1 bit full adder	CI->CO	2	0.429	0.490	0.055	0.028
	with buffered outputs (10)	CI->SO	2	0.267	0.372	0.055	0.028
		P->CO	2	0.739	0.805	0.057	0.028
		P->SO	2	0.600	0.671	0.056	0.029
		Q->CO	2	0.438	0.940	0.056	0.028
		Q->SO	2	1.066	0.811	0.056	0.029
AND2	2 input AND (2)	A->O	1	0.301	0.318	0.055	0.027
		B->O	1	0.318	0.272	0.055	0.026
AND2H	2 input AND	A->O	1	0.395	0.449	0.019	0.009
	- high drive (3)	B->O	1	0.452	0.413	0.018	0.009
AND3	3 input AND (3)	A->O	1	0.478	0.441	0.028	0.013
		B->O	1	0.532	0.405	0.028	0.013
		C->O	1	0.518	0.355	0.028	0.014
AND3H	3 input AND	A->O	1	0.638	0.583	0.014	0.007
	- high drive (4)	B->O	1	0.679	0.539	0.014	0.007
		C->O	1	0.708	0.481	0.014	0.007
AND4	4 input AND (3)	A->O	1	0.560	0.440	0.055	0.026
		B->O	1	0.544	0.400	0.056	0.026
		C->O	1	0.552	0.375	0.055	0.025
		D->O	1	0.538	0.293	0.056	0.026
AND4H	4 input AND	A->O	1	0.713	0.517	0.018	0.010
	- high drive (4)	B->O	1	0.746	0.498	0.018	0.010
		C->O	1	0.746	0.444	0.018	0.010
		D->O	1	0.756	0.410	0.018	0.010
AND5	5 input AND (5)	A->O	1	0.401	0.404	0.113	0.026
		B->O	1	0.264	0.338	0.116	0.026
		C->O	1	0.451	0.365	0.113	0.026
		D->O	1	0.320	0.286	0.116	0.025
		E->O	1	0.429	0.304	0.115	0.026
AOI22	2 input AND into 2 input NOR (2)	A->O	1	0.121	0.166	0.114	0.043
		B->O	1	0.094	0.237	0.114	0.045
		C->O	1	0.111	0.204	0.114	0.032

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
AOI22H	2 input AND into 2 input NOR - high drive (4)	A->O	2	0.136	0.192	0.057	0.021
		B->O	2	0.113	0.242	0.056	0.023
		C->O	2	0.122	0.225	0.057	0.015
AOI222	Two, 2 input ANDs into 2 input NOR (4)	A->O	1	0.121	0.338	0.085	0.045
		B->O	1	0.174	0.271	0.085	0.043
		C->O	1	0.152	0.198	0.083	0.043
		D->O	1	0.104	0.245	0.083	0.045
AOI222H	Two, 2 input ANDs into 2 input NOR - high drive (8)	A->O	2	0.152	0.358	0.042	0.022
		B->O	2	0.190	0.286	0.042	0.021
		C->O	2	0.139	0.211	0.043	0.022
		D->O	2	0.098	0.253	0.043	0.023
AOI2223	Three, 2 input ANDs into 3 input NOR (4)	A->O	1	0.368	0.368	0.113	0.043
		B->O	1	0.324	0.438	0.113	0.044
		C->O	1	0.332	0.312	0.113	0.043
		D->O	1	0.254	0.375	0.114	0.045
		E->O	1	0.242	0.230	0.112	0.043
		F->O	1	0.186	0.277	0.113	0.045
AOI2223H	Three, 2 input ANDs into 3 input NOR - high drive (7)	A->O	1	0.560	0.662	0.028	0.014
		B->O	1	0.609	0.634	0.028	0.013
		C->O	1	0.546	0.622	0.028	0.013
		D->O	1	0.594	0.593	0.028	0.013
		E->O	1	0.533	0.582	0.028	0.013
		F->O	1	0.586	0.548	0.028	0.013
AOI23	2 input AND into 3 input NOR (2)	A->O	1	0.240	0.205	0.170	0.043
		B->O	1	0.169	0.251	0.170	0.045
		C->O	1	0.388	0.259	0.170	0.030
		D->O	1	0.389	0.246	0.169	0.030
BUF1	1x buffer (2)	I->O	1	0.209	0.273	0.055	0.026
BUF2	2x buffer (2)	I->O	1	0.256	0.343	0.028	0.013
BUF2T	2x Tri State bus driver with active high enable (4)	I->O	1	0.345	0.379	0.039	0.027
		E->O	1.5	0.147	0.124	0.044	0.032

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
BUF2Z	2x Tri State bus driver with active low enable (4)	I->O	1	0.336	0.392	0.039	0.027
		E->O	1.5	0.124	0.166	0.039	0.029
BUF3	3x buffer (3)	I->O	1	0.274	0.325	0.017	0.011
BUF4	4x buffer (3)	I->O	1	0.294	0.378	0.013	0.009
BUF8	8x buffer (5)	I->O	2	0.352	0.443	0.007	0.003
BUF12	12x buffer (8)	I->O	3	0.370	0.473	0.005	0.002
BUF16	16x buffer (10)	I->O	4	0.371	0.485	0.003	0.002
CLA7X	7 input carry lookahead (5)	A->O	1	1.018	0.488	0.227	0.076
		B->O	1	0.908	0.539	0.226	0.075
		C->O	1	0.851	0.358	0.226	0.059
		D->O	1	0.428	0.336	0.170	0.044
		E->O	1	0.366	0.246	0.170	0.044
		F->O	1	0.117	0.270	0.114	0.038
		G->O	1	0.106	0.164	0.113	0.031
DEC4	2:4 decoder (7)	S0->D0	3	0.284	0.371	0.057	0.041
		S0->D1	3	0.105	0.282	0.056	0.046
		S0->D2	3	0.294	0.370	0.055	0.041
		S0->D3	3	0.105	0.282	0.056	0.046
		S1->D0	3	0.309	0.363	0.055	0.042
		S1->D1	3	0.310	0.355	0.055	0.041
		S1->D2	3	0.152	0.215	0.055	0.044
		S1->D3	3	0.151	0.216	0.055	0.043
DEC4N	2:4 decoder with active low enable (9)	S0->D0	1	0.323	0.651	0.055	0.042
		S0->D1	1	0.710	0.797	0.056	0.043
		S0->D2	1	0.309	0.696	0.055	0.044
		S0->D3	1	0.734	0.726	0.056	0.042
		S1->D0	1	0.330	0.433	0.056	0.042
		S1->D1	1	0.362	0.415	0.056	0.042
		S1->D2	1	0.501	0.591	0.056	0.042
		S1->D3	1	0.514	0.590	0.050	0.043
		E->D0	2	0.369	0.591	0.056	0.042
		E->D1	2	0.310	0.558	0.055	0.043
		E->D2	2	0.315	0.624	0.059	0.043
		E->D3	2	0.333	0.556	0.056	0.041

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
DEC8N	3:8 decoder with active low enable (24)	S0->D0	1	0.491	0.872	0.055	0.057
		S0->D1	1	1.036	1.068	0.056	0.057
		S0->D2	1	0.491	0.872	0.055	0.057
		S0->D3	1	1.036	1.068	0.056	0.057
		S0->D4	1	0.491	0.872	0.055	0.057
		S0->D5	1	1.036	1.068	0.056	0.057
		S0->D6	1	0.491	0.872	0.055	0.057
		S0->D7	1	1.036	1.068	0.056	0.057
		S1->D0	1	0.435	0.601	0.055	0.057
		S1->D1	1	0.435	0.601	0.055	0.057
		S1->D2	1	0.681	0.886	0.056	0.056
		S1->D3	1	0.681	0.886	0.056	0.056
		S1->D4	1	0.435	0.601	0.055	0.057
		S1->D5	1	0.435	0.601	0.055	0.057
		S1->D6	1	0.681	0.886	0.056	0.057
		S1->D7	1	0.681	0.886	0.056	0.056
		S2->D0	1	0.464	0.589	0.055	0.057
		S2->D1	1	0.464	0.589	0.055	0.057
		S2->D2	1	0.464	0.589	0.055	0.057
		S2->D3	1	0.464	0.589	0.055	0.057
		S2->D4	1	0.702	0.860	0.055	0.056
		S2->D5	1	0.702	0.860	0.055	0.056
		S2->D6	1	0.702	0.860	0.055	0.056
		S2->D7	1	0.702	0.860	0.055	0.056
		E->D0	2	0.518	0.831	0.055	0.056
		E->D1	2	0.518	0.831	0.055	0.056
		E->D2	2	0.518	0.831	0.055	0.056
		E->D3	2	0.518	0.831	0.055	0.056
		E->D4	2	0.518	0.831	0.055	0.056
		E->D5	2	0.518	0.831	0.055	0.056
		E->D6	2	0.518	0.831	0.055	0.056
		E->D7	2	0.518	0.831	0.055	0.056
DFF	D flip-flop (8)	CLK->Q	1	0.658	0.688	0.027	0.018
		D+CLK		0.110	0.034	0.240	0.318
DFFBCPX	D flip-flop with asynchronous clear and preset with complementary outputs (16)	CLK->Q	1	1.098	0.857	0.026	0.014
		CLK->QB	1	1.112	1.307	0.027	0.014
		C->Q	2	0.767	0.621	0.021	0.015
		C->QB	2	1.247	0.000	0.008	0.000
		P->Q	2	1.083	0.000	0.010	0.000
		P->QB	2	0.908	0.654	0.022	0.015
		D+CLK		0.001	0.028	0.528	0.314

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
DFFBSRX	D flip-flop with asynchronous set and reset with complementary outputs (16)	CLK->Q	1	0.853	1.026	0.056	0.026
		CLK->QB	1	1.113	1.181	0.056	0.026
		R->Q	2	0.000	1.052	0.000	0.026
		R->QB	2	0.634	0.761	0.056	0.027
		S->Q	2	0.533	0.624	0.055	0.027
		S->QB	2	0.000	1.019	0.000	0.026
		D+CLK		0.118	0.020	0.332	0.525
DFFC	D flip-flop with asynchronous clear (9)	CLK->Q	1	0.701	0.679	0.028	0.015
		C->Q	2	——	0.823	——	0.014
		D+CLK		0.011	0.008	0.355	0.574
DFFR	D flip-flop with asynchronous reset (11)	CLK->Q	1	0.736	0.666	0.028	0.018
		R->Q	1	——	0.881	——	0.017
		D+CLK		0.003	0.028	0.435	0.316
DFFS	D flip-flop with asynchronous set (9)	CLK->Q	1	0.663	0.708	0.027	0.021
		S->Q	2	0.476	——	0.026	——
		D+CLK		0.011	-0.097	0.234	0.629
DFFSR	D flip-flop with asynchronous set and reset (12)	CLK->Q	1	1.086	0.937	0.027	0.015
		R->Q	2	0.629	0.521	0.026	0.014
		S->Q	2	0.863	——	0.025	——
		D+CLK		0.011	-0.001	0.336	0.525
DLY1500	Delay buffer 1.5 ns (6)	I->O	1	1.590	1.543	0.055	0.030
DLY2000	Delay buffer 2.0 ns (10)	I->O	1	1.996	2.244	0.055	0.027
DLY6000	Delay buffer 6.0 ns (24)	I->O	1	6.091	6.252	0.057	0.032
DSS	Set scan D flip-flop (11)	CLK->Q	1	0.750	0.870	0.018	0.011
		D+CLK		-0.090	-0.079	0.657	0.583
		TE+CLK		-0.100	-0.056	0.869	0.908
		TI+CLK		-0.151	-0.067	0.665	0.650

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
DSSBCPY	Set scan flip-flop with clear and preset (16)	CLK->Q	1	0.628	1.097	0.029	0.015
		CLK->QB	1	1.276	1.172	0.028	0.015
		C->Q	2	0.000	1.067	0.000	0.015
		C->QB	2	0.453	0.933	0.028	0.015
		P->Q	2	0.414	0.777	0.028	0.015
		P->QB	2	0.000	1.184	0.000	0.016
		D+CLK		-0.097	-0.084	1.098	0.982
		TE+CLK		-0.101	-0.161	0.954	1.117
		TI+CLK		-0.095	-0.267	0.603	1.179
DSSBR	Set scan flip-flop with reset (13)	CLK->Q	1	0.684	0.818	0.029	0.014
		CLK->QB	1	0.982	1.204	0.027	0.014
		R->Q	2	0.000	0.791	0.000	0.013
		R->QB	2	0.389	0.000	0.028	0.000
		D+CLK		-0.195	-0.082	1.029	0.684
		TE+CLK		-0.199	-0.159	1.165	0.907
		TI+CLK		-0.199	-0.079	1.027	0.687
DSSBS	Set scan flip-flop with set (13)	CLK->Q	1	0.649	0.896	0.028	0.013
		CLK->QB	1	1.107	0.979	0.028	0.014
		S->Q	1	0.885	0.000	0.028	0.000
		S->QB	1	0.000	0.674	0.000	0.014
		D+CLK		-0.091	-0.174	0.645	0.783
		TE+CLK		-0.106	-0.156	0.863	1.007
		TI+CLK		-0.098	-0.174	0.645	0.781
DSSR	Set scan D flip-flop with reset (13)	CLK->Q	1	0.698	0.848	0.028	0.013
		R->Q	2	——	0.626	——	0.013
		D+CLK		-0.195	-0.082	1.033	0.684
		TE+CLK		-0.199	-0.159	1.177	0.907
		TI+CLK		-0.199	-0.079	1.131	0.687
DSSS	Set scan D flip-flop with set (12)	CLK->Q	1	0.635	0.893	0.029	0.013
		S->Q	1	0.841	0.000	0.028	0.000
		D+CLK		0.000	0.000	0.649	0.783
		TE+CLK		-0.101	-0.156	0.863	1.007
		TI+CLK		-0.098	-0.174	0.648	0.781
DSSSR	Set scan flip-flop with set and reset (14)	CLK->Q	1	0.770	0.899	0.028	0.013
		R->Q	1	0.546	0.617	0.029	0.013
		S->Q	1	0.908	0.000	0.028	0.000
		D+CLK		-0.088	-0.179	0.743	0.683
		TE+CLK		-0.106	-0.157	0.959	1.007
		TI+CLK		-0.099	-0.177	0.742	0.681

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
INV1	1x inverter (1)	I->O	1	0.062	0.243	0.057	0.029
INV1D	Dual 1x inverters (2)	I0->O0	1	0.062	0.243	0.057	0.029
		I1->O1	1	0.062	0.243	0.057	0.029
INV1Q	Quad 1x inverters (4)	I0->O0	1	0.062	0.243	0.057	0.029
		I1->O1	1	0.062	0.243	0.057	0.029
		I2->O2	1	0.062	0.243	0.057	0.029
		I3->O3	1	0.062	0.243	0.057	0.029
INV1TQ	Quad Tri State inverter (7)	I0->O0	1	0.095	0.258	0.115	0.042
		I1->O1	1	0.095	0.258	0.115	0.042
		I2->O2	1	0.095	0.258	0.115	0.042
		I3->O3	1	0.095	0.258	0.115	0.042
		E0->O0	1	0.319	0.689	0.115	0.041
		E0->O1	1	0.319	0.689	0.115	0.041
		E0->O2	1	0.319	0.689	0.115	0.041
		E0->O3	1	0.319	0.689	0.115	0.041
		E1->O0	1	0.310	0.643	0.114	0.041
		E1->O1	1	0.310	0.643	0.114	0.041
		E1->O2	1	0.310	0.643	0.114	0.041
		E1->O3	1	0.310	0.643	0.114	0.041
INV2	2x inverter (2)	I->O	2	0.079	0.181	0.028	0.016
INV2T	2x Tri State inverter	I->O	2	0.156	0.207	0.040	0.029
	with active high enable (3)	E->O	1.5	0.147	0.103	0.044	0.032
INV3	3x inverter (2)	I->O	3	0.086	0.202	0.019	0.010
INV4	4x inverter (2)	I->O	4	0.104	0.196	0.014	0.008
INV8	8x inverter (4)	I->O	8	0.132	0.208	0.007	0.004
INV10	10x inverter (8)	I->O	1	0.517	0.648	0.006	0.003
JKF	JK flip flop (10)	CLK->Q	1	0.643	0.734	0.028	0.016
		J+CLK		-0.137	-0.080	0.482	0.230
		K+CLK		-0.246	-0.102	0.842	0.616

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
JKFBCPX	Clear preset JK flip-flop with asynchronous clear and preset and complementary outputs (16)	CLK->Q	1	0.762	0.886	0.028	0.013
		CLK->QB	1	1.181	1.193	0.028	0.014
		C->Q	2	0.416	0.453	0.029	0.014
		C->QB	2	0.907	0.000	0.028	0.000
		P->Q	2	0.916	0.000	0.028	0.000
		P->QB	2	0.687	0.587	0.028	0.014
		J+CLK		-0.341	-0.204	1.239	1.256
		K+CLK		-0.329	-0.108	1.136	1.614
JKFC	JK flip flop with asynchronous clear (12)	CLK->Q	1	0.695	0.669	0.028	0.016
		C->Q	2	0.000	0.610	0.000	0.015
		J+CLK		-0.184	0.080	0.367	0.231
		K+CLK		-0.481	-0.196	0.943	0.453
LAT	LATCH (4)	D->Q	1	0.400	0.597	0.026	0.016
		H->Q	2	0.491	0.519	0.026	0.016
		D+H		-0.086	-0.340	0.474	0.980
LATBG	LATCH with complementary outputs and inverted gate signal (6)	D->Q	1	0.458	0.634	0.031	0.028
		D->QB	1	0.730	0.628	0.029	0.024
		G->Q	1	0.703	0.715	0.031	0.028
		G->QB	1	0.814	0.869	0.030	0.025
		D-G		0.012	-0.196	0.725	1.034
LATBH	LATCH with high drive complementary outputs (7)	D->Q	1	0.370	0.719	0.034	0.013
		D->QB	1	0.888	0.666	0.033	0.012
		H->Q	1	0.646	0.950	0.016	0.014
		H->QB	1	1.113	0.893	0.014	0.012
		D+H		0.143	-0.237	0.570	0.853
LATR	LATCH with reset (4)	D->Q	1	0.380	0.545	0.115	0.027
		H->Q	2	0.498	0.469	0.113	0.028
		R->Q	1	0.198	0.242	0.115	0.030
		D+H		-0.085	-0.241	0.572	0.893
LATS	LATCH with set (6)	D->Q	1	0.355	0.818	0.057	0.030
		H->Q	2	0.458	0.683	0.054	0.030
		S->Q	2	0.397	0.836	0.056	0.030
		D+H		-0.086	-0.449	0.472	1.477

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
LATSR	LATCH with set and reset (8)	D->Q	1	0.795	1.045	0.057	0.026
		H->Q	2	0.888	0.912	0.056	0.026
		R->Q	1	0.565	0.475	0.056	0.027
		S->Q	2	0.782	1.047	0.057	0.026
		D+H		-0.086	-0.435	0.574	1.197
LSCC	Voltage level shifter (4)	I->01	1	0.851	1.013	0.055	0.026
		I->02	1	0.729	1.126	0.054	0.027
LSISO	Voltage level shifter with power supply isolation function (12)	I->01	1	1.340	1.305	0.055	0.026
		I->02	1	1.005	1.618	0.054	0.026
		ISN->01	1.5	1.059	0.539	0.052	0.026
		ISN->02	1.5	0.511	1.105	0.055	0.028
		ISNB->01	1.5	1.059	0.539	0.052	0.026
		ISNB->02	1.5	0.511	1.105	0.055	0.028
MUX2	2:1 MUX (4)	I0->O	1	0.359	0.595	0.028	0.014
		I1->O	1	0.369	0.602	0.028	0.014
		S->O	2	0.354	0.472	0.028	0.015
MUX2H	2:1 MUX - high drive (5)	I0->O	1	0.502	0.790	0.014	0.008
		I1->O	1	0.493	0.796	0.014	0.008
		S->O	2	0.522	0.677	0.014	0.008
MUX2I	2:1 MUX with inverted output (3)	I0->O	2	0.174	0.253	0.056	0.033
		I1->O	2	0.171	0.251	0.055	0.033
		S->O	2	0.289	0.348	0.055	0.026
MUX2IH	2:1 MUX with inverted output - high drive (4)	I0->O	3	0.247	0.317	0.019	0.012
		I1->O	3	0.249	0.316	0.019	0.012
		S->O	2	0.333	0.446	0.019	0.009
MUX2N	2:1 MUX with active low enable (4)	I0->O	1	0.340	0.529	0.113	0.027
		I1->O	1	0.317	0.535	0.115	0.027
		S->O	2	0.304	0.406	0.113	0.027
		E->O	1	0.109	0.164	0.113	0.031

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
MUX2NQ	Quad 2:1 MUX with active low enable (18)	IA0->OA	1	0.331	0.518	0.056	0.042
		IA1->OA	1	0.332	0.520	0.056	0.042
		IB0->OB	1	0.331	0.518	0.056	0.042
		IB1->OB	1	0.332	0.520	0.056	0.042
		IC0->OC	1	0.331	0.518	0.056	0.042
		IC1->OC	1	0.332	0.520	0.056	0.042
		ID0->OD	1	0.331	0.518	0.056	0.042
		ID1->OD	1	0.332	0.520	0.056	0.042
		S->OA	1	0.850	0.996	0.056	0.041
		S->OB	1	0.850	0.996	0.056	0.041
		S->OC	1	0.850	0.996	0.056	0.041
		S->OD	1	0.850	0.996	0.056	0.041
		E->OA	1	0.337	0.452	0.056	0.042
		E->OB	1	0.337	0.452	0.056	0.042
		E->OC	1	0.337	0.452	0.056	0.042
		E->OD	1	0.337	0.452	0.056	0.042
MUX2Q	Quad 2:1 MUX (14)	IA0->OA	1	0.374	0.563	0.027	0.016
		IA1->OA	1	0.375	0.563	0.027	0.016
		IB0->OB	1	0.374	0.563	0.027	0.016
		IB1->OB	1	0.375	0.563	0.027	0.016
		IC0->OC	1	0.374	0.563	0.027	0.016
		IC1->OC	1	0.375	0.563	0.027	0.016
		ID0->OD	1	0.374	0.563	0.027	0.016
		ID1->OD	1	0.375	0.563	0.027	0.016
		S->OA	1	0.881	1.037	0.027	0.017
		S->OB	1	0.881	1.037	0.027	0.017
		S->OC	1	0.881	1.037	0.027	0.017
		S->OD	1	0.881	1.037	0.027	0.017
MUX3I	3:1 MUX with inverted output (6)	I0->O	2	0.223	0.266	0.084	0.045
		I1->O	2	0.209	0.272	0.085	0.044
		I2->O	1	0.123	0.337	0.085	0.045
		S0->O	2	0.334	0.317	0.116	0.040
		S1->O	2	0.091	0.227	0.114	0.044
MUX3IH	3:1 MUX with inverted output - high drive (8)	I0->O	2	0.266	0.300	0.042	0.023
		I1->O	2	0.244	0.307	0.043	0.023
		I2->O	2	0.154	0.357	0.042	0.022
		S0->O	2	0.363	0.429	0.043	0.021
		S1->O	2	0.264	0.399	0.057	0.020

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
MUX4	4:1 MUX (9)	I0->O	1	0.675	0.888	0.019	0.016
		I1->O	1	0.669	0.890	0.019	0.016
		I2->O	1	0.673	0.884	0.019	0.016
		I3->O	1	0.668	0.891	0.018	0.016
		S0->O	3	1.116	1.209	0.026	0.022
		S1->O	2	0.770	0.746	0.024	0.021
MUX4X	4:1 MUX with transmission gate data inputs (10)	I0->O	2	0.403	0.618	0.056	0.028
		I1->O	2	0.397	0.595	0.056	0.028
		I2->O	2	0.371	0.572	0.055	0.028
		I3->O	2	0.386	0.566	0.055	0.028
		S0->O	3	0.602	0.824	0.056	0.028
		S1->O	2	0.297	0.385	0.055	0.027
MUX4XH	4:1 MUX with transmission gate data inputs - high drive (10)	I0->O	2	0.448	0.706	0.028	0.014
		I1->O	2	0.454	0.701	0.028	0.014
		I2->O	2	0.428	0.667	0.028	0.014
		I3->O	2	0.440	0.664	0.028	0.014
		S0->O	3	0.641	0.921	0.028	0.014
		S1->O	2	0.354	0.471	0.028	0.015
MUX5H	5:1 MUX - with high drive (14)	I0->O	1	0.882	1.144	0.028	0.014
		I1->O	1	0.890	1.141	0.028	0.014
		I2->O	1	0.894	1.144	0.028	0.014
		I3->O	1	0.894	1.142	0.027	0.014
		I4->O	1	0.369	0.602	0.028	0.014
		S0->O	1	1.243	1.452	0.027	0.014
		S1->O	2	0.729	0.926	0.028	0.014
		S2->O	2	0.354	0.471	0.028	0.015
MUX8	8:1 MUX (18)	I0->O	1	0.793	1.066	0.055	0.036
		I1->O	1	0.793	1.066	0.055	0.036
		I2->O	1	0.794	1.067	0.055	0.036
		I3->O	1	0.793	1.067	0.055	0.036
		I4->O	1	0.793	1.067	0.055	0.036
		I5->O	1	0.792	1.067	0.055	0.036
		I6->O	1	0.793	1.066	0.055	0.036
		I7->O	1	0.793	1.066	0.055	0.036
		S0->O	1	1.240	1.523	0.057	0.036
		S1->O	1	0.843	0.924	0.056	0.036
		S2->O	1	0.574	0.598	0.056	0.034

ATL80 - 0.8 µ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
MUX8N	8:1 MUX with active low enable (20)	E->O	1	0.095	0.187	0.114	0.033
		I0->O	1	0.769	1.029	0.114	0.031
		I1->O	1	0.769	1.029	0.114	0.036
		I2->O	1	0.777	1.029	0.114	0.036
		I3->O	1	0.777	1.029	0.114	0.036
		I4->O	1	0.774	1.030	0.114	0.036
		I5->O	1	0.769	1.030	0.114	0.036
		I6->O	1	0.777	1.030	0.114	0.036
		I7->O	1	0.777	1.030	0.114	0.036
		S0->O	1	1.253	1.493	0.113	0.036
		S1->O	1	0.861	0.927	0.111	0.035
		S2->O	1	0.573	0.606	0.114	0.033
MUX8XH	8:1 MUX with transmission data inputs - high drive (18)	I0->O	2	0.672	0.930	0.027	0.017
		I1->O	2	0.672	0.930	0.027	0.017
		I2->O	2	0.655	0.934	0.028	0.017
		I3->O	2	0.655	0.933	0.028	0.017
		I4->O	2	0.659	0.932	0.029	0.017
		I5->O	2	0.659	0.932	0.029	0.017
		I6->O	2	0.684	0.942	0.028	0.016
		I7->O	2	0.684	0.939	0.027	0.016
		S0->O	1	0.952	1.323	0.028	0.016
		S1->O	3	0.627	0.756	0.028	0.017
		S2->O	2	0.390	0.468	0.028	0.016
NAN2	2 input NAND (2)	A->O	1	0.127	0.204	0.056	0.042
		B->O	1	0.086	0.257	0.057	0.044
NAN2D	Dual 2 input NAND (3)	A0->O0	1	0.127	0.201	0.056	0.043
		A1->O0	1	0.127	0.201	0.056	0.043
		B0>O1	1	0.086	0.257	0.057	0.044
		B1->O1	1	0.086	0.257	0.057	0.044
NAN2H	2 input NAND - high drive (2)	A->O	2	0.129	0.217	0.028	0.021
		B->O	2	0.087	0.253	0.028	0.023
NAN3	3 input NAND (2)	A->O	1	0.183	0.273	0.055	0.057
		B->O	1	0.146	0.333	0.056	0.057
		C->O	1	0.107	0.335	0.057	0.059
NAN3H	3 input NAND - high drive (3)	A->O	2	0.176	0.236	0.027	0.030
		B->O	2	0.142	0.269	0.028	0.030
		C->O	2	0.104	0.281	0.027	0.032

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
NAN4	4 input NAND (3)	A->O	1	0.223	0.337	0.055	0.072
		B->O	1	0.191	0.371	0.055	0.072
		C->O	1	0.144	0.386	0.057	0.072
		D->O	1	0.107	0.373	0.057	0.074
NAN4H	4 input NAND - high drive (4)	A->O	2	0.162	0.338	0.027	0.038
		B->O	2	0.162	0.338	0.027	0.038
		C->O	2	0.170	0.346	0.027	0.038
		D->O	2	0.170	0.346	0.027	0.038
NAN5	5 input NAND (5)	A->O	1	0.433	0.744	0.055	0.027
		B->O	1	0.382	0.628	0.057	0.027
		C->O	1	0.407	0.781	0.055	0.027
		D->O	1	0.328	0.657	0.056	0.027
		E->O	1	0.341	0.777	0.056	0.028
NAN5H	5 input NAND - high drive (6)	A->O	1	0.507	0.964	0.019	0.010
		B->O	1	0.449	0.851	0.019	0.010
		C->O	1	0.465	0.999	0.019	0.010
		D->O	1	0.395	0.901	0.019	0.010
		E->O	1	0.409	0.005	0.019	0.010
NAN6	6 input NAND (6)	A->O	1	0.502	0.788	0.026	0.018
		B->O	1	0.488	0.803	0.026	0.016
		C->O	1	0.467	0.834	0.026	0.017
		D->O	1	0.443	0.833	0.026	0.016
		E->O	1	0.415	0.846	0.026	0.017
		F->O	1	0.383	0.856	0.027	0.016
NAN6H	6 input NAND - high drive (7)	A->O	1	0.591	1.008	0.013	0.009
		B->O	1	0.564	1.012	0.013	0.009
		C->O	1	0.542	1.039	0.013	0.009
		D->O	1	0.521	1.032	0.013	0.009
		E->O	1	0.493	1.055	0.013	0.009
		F->O	1	0.479	1.073	0.013	0.008
NAN8	8 input NAND (7)	A->O	1	0.537	0.910	0.026	0.016
		B->O	1	0.509	0.931	0.026	0.016
		C->O	1	0.498	0.925	0.026	0.017
		D->O	1	0.481	0.908	0.026	0.017
		E->O	1	0.465	0.937	0.026	0.016
		F->O	1	0.439	0.923	0.027	0.016
		G->O	1	0.411	0.929	0.026	0.016
		H->O	1	0.380	0.933	0.027	0.016

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
NAN8H	8 input NAND - high drive (7)	A->O	1	0.598	1.159	0.014	0.008
		B->O	1	0.591	1.164	0.014	0.008
		C->O	1	0.555	1.173	0.014	0.008
		D->O	1	0.535	1.193	0.014	0.007
		E->O	1	0.520	1.162	0.014	0.008
		F->O	1	0.503	1.178	0.014	0.008
		G->O	1	0.467	1.171	0.014	0.008
		H->O	1	0.436	1.157	0.014	0.008
NOR2	2 input NOR (2)	A->O	1	0.091	0.196	0.114	0.031
		B->O	1	0.109	0.164	0.113	0.031
NOR2D	Dual 2 input NOR (3)	A0->O0	1	0.091	0.196	0.114	0.031
		A1->O1	1	0.091	0.196	0.114	0.031
		B0->O0	1	0.109	0.163	0.113	0.031
		B1->O1	1	0.109	0.163	0.113	0.031
NOR2H	2 input NOR - high drive (2)	A->O	2	0.131	0.146	0.054	0.019
		B->O	2	0.143	0.116	0.054	0.018
NOR3	3 input NOR (2)	A->O	1	0.258	0.217	0.171	0.031
		B->O	1	0.234	0.201	0.171	0.032
		C->O	1	0.183	0.174	0.170	0.031
NOR3H	3 input NOR - high drive (3)	A->O	2	0.202	0.210	0.085	0.016
		B->O	2	0.182	0.194	0.085	0.016
		C->O	2	0.129	0.172	0.085	0.015
NOR4	4 input NOR (3)	A->O	1	0.427	0.206	0.227	0.032
		B->O	1	0.391	0.201	0.227	0.033
		C->O	1	0.331	0.193	0.226	0.033
		D->O	1	0.220	0.152	0.227	0.034
NOR4H	4 input NOR - high drive (4)	A->O	2	0.314	0.133	0.112	0.019
		B->O	2	0.314	0.133	0.112	0.019
		C->O	2	0.342	0.150	0.112	0.019
		D->O	2	0.342	0.150	0.112	0.019

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
NOR5	5 input NOR (5)	A->O	1	0.796	0.450	0.055	0.026
		B->O	1	0.527	0.447	0.056	0.026
		C->O	1	0.803	0.420	0.055	0.026
		D->O	1	0.529	0.417	0.056	0.026
		E->O	1	0.726	0.389	0.056	0.026
NOR8	8 input NOR (7)	A->O	1	1.096	0.483	0.027	0.014
		B->O	1	1.073	0.520	0.027	0.014
		C->O	1	1.086	0.464	0.026	0.015
		D->O	1	1.057	0.520	0.027	0.014
		E->O	1	1.041	0.451	0.026	0.014
		F->O	1	0.992	0.489	0.027	0.014
		G->O	1	0.938	0.422	0.026	0.014
		H->O	1	0.897	0.456	0.027	0.014
OAI22	2 input OR into 2 input NAND (2)	A->O	1	0.250	0.240	0.114	0.043
		B->O	1	0.232	0.260	0.113	0.043
		C->O	1	0.107	0.285	0.057	0.045
OAI22H	2 Input OR into 3 input NAND - high drive (4)	A->O	2	0.099	0.295	0.056	0.022
		B->O	2	0.103	0.247	0.057	0.023
		C->O	2	0.182	0.256	0.027	0.018
OAI222	Two, 2 input ORs into 2 input NAND (2)	A->O	1	0.238	0.248	0.113	0.043
		B->O	1	0.233	0.276	0.113	0.043
		C->O	1	0.117	0.324	0.114	0.045
		D->O	1	0.128	0.278	0.114	0.045
OAI222H	Two, 2 input ORs into 2 input NAND - high drive (4)	A->O	2	0.295	0.227	0.055	0.024
		B->O	2	0.290	0.273	0.053	0.023
		C->O	2	0.150	0.208	0.054	0.021
		D->O	2	0.156	0.158	0.054	0.022
OAI22224	Four, 2 input ORs into 4 input NAND (6)	A->O	1	0.635	0.619	0.056	0.027
		B->O	1	0.632	0.669	0.056	0.027
		C->O	1	0.486	0.625	0.056	0.027
		D->O	1	0.478	0.566	0.056	0.028
		E->O	1	0.607	0.598	0.056	0.028
		F->O	1	0.601	0.659	0.056	0.027
		G->O	1	0.452	0.610	0.056	0.027
		H->O	1	0.462	0.547	0.055	0.028

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
OAI23	2 input OR into 3 input NAND (3)	A->O	1	0.137	0.357	0.114	0.059
		B->O	1	0.150	0.310	0.114	0.060
		C->O	1	0.202	0.292	0.055	0.057
		D->O	1	0.178	0.331	0.056	0.058
ORR2	2 input OR (2)	A->O	1	0.215	0.437	0.056	0.027
		B->O	1	0.180	0.444	0.055	0.027
ORR2H	2 input OR - high drive (3)	A->O	1	0.324	0.633	0.019	0.010
		B->O	1	0.285	0.650	0.019	0.010
ORR3	3 input OR (3)	A->O	1	0.317	0.768	0.027	0.018
		B->O	1	0.305	0.754	0.026	0.019
		C->O	1	0.270	0.717	0.026	0.018
ORR3H	3 input OR - high drive (4)	A->O	1	0.406	1.119	0.014	0.008
		B->O	1	0.380	1.106	0.014	0.008
		C->O	1	0.367	1.047	0.013	0.008
ORR4	4 input OR (3)	A->O	1	0.280	0.915	0.055	0.032
		B->O	1	0.270	0.900	0.055	0.032
		C->O	1	0.222	0.820	0.056	0.032
		D->O	1	0.193	0.732	0.055	0.032
ORR4H	4 input OR - high drive (4)	A->O	1	0.371	1.273	0.018	0.012
		B->O	1	0.357	1.270	0.018	0.012
		C->O	1	0.338	1.215	0.018	0.012
		D->O	1	0.297	0.106	0.019	0.012
ORR5	5 input OR (5)	A->O	1	0.283	0.755	0.055	0.043
		B->O	1	0.248	0.458	0.055	0.042
		C->O	1	0.240	0.730	0.056	0.043
		D->O	1	0.212	0.449	0.055	0.042
		E->O	1	0.195	0.678	0.055	0.043
XNR2	2 input exclusive NOR (4)	A->O	2	0.306	0.348	0.115	0.040
		B->O	2	0.194	0.301	0.113	0.040

ATL80 - 0.8 μ Cell Index (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path Timechk	Input Load	Intercept Rising Hold-R	Intercept Falling Hold-F	Slope Rising Setup-R	Slope Falling Setup-F
XNR2H	2 input exclusive NOR - high drive (4)	A->O	1	0.520	0.801	0.028	0.014
		B->O	2	0.447	0.516	0.029	0.015
XOR2	2 input exclusive OR (4)	A->O	2	0.384	0.337	0.110	0.041
		B->O	2	0.187	0.318	0.114	0.039
XOR2H	2 input exclusive OR - high drive (4)	A->O	1	0.449	0.729	0.028	0.015
		B->O	2	0.366	0.652	0.028	0.014

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Sample of buffers composed of modular I/O building blocks

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBD2C	4 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	2.0	0.882	1.479	0.087	0.066
		E0->P	2.0	1.207	1.716	0.087	0.067
		E1->P	2.0	0.939	1.457	0.087	0.067
PBD3C	6 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	2.0	1.029	1.648	0.058	0.046
		E0->P	2.0	1.351	1.897	0.058	0.047
		E1->P	2.0	1.083	1.628	0.058	0.047
PBD32TS	6 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	2.0	1.445	4.239	0.061	0.054
		E0->P	3.0	1.787	5.330	0.061	0.054
		E1->P	4.5	1.467	5.021	0.061	0.054
PBD5C	10 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	2.0	1.290	1.929	0.036	0.032
		E0->P	2.0	1.592	2.215	0.036	0.032
		E1->P	2.0	1.325	1.952	0.036	0.032
PBDSCSITS	48 mA NMOS SCSI buffer TTL Schmitt Trigger input (1)	P->AI0		2.173	4.376	0.018	0.010
		AO->P		5.759	2.348	0.015	0.017
		E0->P		2.985	2.985	0.022	0.022
		R->P		2.985	2.985	0.022	0.022
PBS1C	2 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.0	0.964	1.548	0.182	0.114
		E0->P	2.0	0.732	0.889	0.181	0.136
PBS1CS	2 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.0	0.964	1.548	0.182	0.114
		E0->P	2.0	0.732	0.889	0.181	0.136
		P->AI0		0.733	1.050	0.014	0.007
		AO->P		0.964	1.548	0.182	0.114
		E0->P		0.732	0.889	0.181	0.136
PBS1TS	2 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.0	0.964	1.548	0.182	0.114
		E0->P	2.0	0.732	0.889	0.181	0.136

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBS2C	4 mA bidi CMOS input buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.0	1.072	1.006	0.091	0.068
		E0->P	2.0	0.848	1.117	0.091	0.068
PBS2CS	4 mA bidi CMOS input buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.0	1.072	1.006	0.091	0.068
		E0->P	2.0	0.848	1.117	0.091	0.068
PBS2T	4 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.070
		AO->P	3.0	1.072	1.006	0.091	0.068
		E0->P	2.0	0.848	1.117	0.091	0.068
PBS2TS	4 mA with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.0	1.072	1.006	0.091	0.068
		E0->P	2.0	0.848	1.117	0.091	0.068
PBS3C	6 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.0	1.275	1.228	0.061	0.046
		E0->P	2.0	1.021	1.329	0.061	0.046
PBS3CS	6 mA with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.0	1.275	1.228	0.061	0.046
		E0->P	2.0	1.021	1.329	0.061	0.046
PBS31T	6 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.0	1.608	2.304	0.061	0.041
		E0->P	2.0	1.252	2.548	0.061	0.041
PBS3T	6 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	5.0	1.275	1.228	0.061	0.046
		E0->P	2.0	1.021	1.329	0.061	0.046
PBS3TS	6 mA bidi with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.0	1.275	1.228	0.061	0.046
		E0->P	2.0	1.021	1.329	0.061	0.046
PBS4C	8 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.0	1.376	1.459	0.046	0.036
		E0->P	2.5	1.411	2.095	0.046	0.038

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBS4CS	8 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.0	1.376	1.459	0.046	0.036
		E0->P	2.0	1.411	2.095	0.046	0.038
PBS4T	8 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.0	1.376	1.459	0.046	0.036
		E0->P	2.5	1.411	2.095	0.046	0.038
PBS4TS	8 mA bidi TTL buffer (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.0	1.376	1.459	0.046	0.036
		E0->P	2.5	1.411	2.095	0.046	0.038
PBS5C	10 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.0	1.503	1.592	0.037	0.031
		E0->P	2.5	1.450	1.670	0.037	0.030
PBS5CS	10 mA bidi with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.0	1.503	1.592	0.037	0.031
		E0->P	2.5	1.450	1.670	0.037	0.030
PBS5T	10 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.0	1.503	1.592	0.037	0.031
		E0->P	2.5	1.450	1.670	0.037	0.030
PBS5TS	10 mA with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.0	1.503	1.592	0.037	0.031
		E0->P	2.5	1.450	1.670	0.037	0.030
PBS6C	12 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.426	1.390	0.031	0.026
		E0->P	2.0	1.213	1.503	0.031	0.025
PBS6CS	12 mA bidi Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.426	1.390	0.031	0.026
		E0->P	2.0	1.213	1.503	0.031	0.025
PBS6T	12 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.426	1.390	0.031	0.026
		E0->P	2.0	1.213	1.503	0.031	0.025

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBS6TS	12 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.426	1.390	0.031	0.026
		E0->P	2.0	1.213	1.503	0.031	0.025
PBS7C	14 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.528	1.781	0.027	0.025
		E0->P	2.0	1.292	1.587	0.027	0.023
PBS7CS	14 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.528	1.781	0.027	0.025
		E0->P	2.0	1.292	1.587	0.027	0.023
PBS7T	14 mA bidi TTTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.528	1.781	0.027	0.025
		E0->P	2.0	1.292	1.587	0.027	0.023
PBS7TS	14 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.528	1.781	0.027	0.025
		E0->P	2.0	1.292	1.587	0.027	0.023
PBS8C	16 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.642	1.579	0.024	0.022
		E0->P	2.0	1.396	1.696	0.024	0.022
PBS8CS	16 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.642	1.579	0.024	0.022
		E0->P	2.0	1.396	1.696	0.024	0.022
PBS8T	16 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.642	1.579	0.024	0.022
		E0->P	2.0	1.396	1.696	0.024	0.022
PBS8TS	16 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.642	1.579	0.024	0.022
		E0->P	2.0	1.396	1.696	0.024	0.022
PBS9C	18 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.733	1.994	0.022	0.022
		E0->P	2.0	1.460	1.790	0.022	0.020

ATL80 - 0.8 μ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBS9CS	18 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.733	1.994	0.022	0.022
		E0->P	2.0	1.460	1.790	0.022	0.020
PBS9T	18 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.733	1.994	0.022	0.022
		E0->P	2.0	1.460	1.790	0.022	0.020
PBS9TS	18 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.733	1.994	0.022	0.022
		E0->P	2.0	1.460	1.790	0.022	0.020
PBSAC	20 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.786	2.083	0.021	0.022
		E0->P	2.0	1.523	2.201	0.021	0.022
PBSACS	20 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.786	2.083	0.021	0.022
		E0->P	2.0	1.523	2.201	0.021	0.022
PBSAT	20 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.786	2.083	0.021	0.022
		E0->P	2.0	1.523	2.201	0.021	0.022
PBSATS	20 mA bidi with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.786	2.083	0.021	0.022
		E0->P	2.0	1.523	2.201	0.021	0.022
PBSA6T	20 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.538	2.053	0.030	0.022
		E0->P	2.0	1.189	2.160	0.031	0.022
PBSBC	22 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.868	2.174	0.019	0.021
		E0->P	2.0	1.585	2.282	0.020	0.021
PBSBCS	22 m A bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.868	2.174	0.019	0.021
		E0->P	2.0	1.585	2.282	0.020	0.021

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PBSBT	22 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.868	2.174	0.019	0.021
		E0->P	2.0	1.585	2.282	0.020	0.021
PBSBTS	22 mA bidi TTL buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
		AO->P	3.5	1.868	2.174	0.019	0.021
		E0->P	2.0	1.585	2.282	0.020	0.021
PBSCC	24 mA bidi CMOS buffer (1)	P->AI0		0.843	1.070	0.007	0.003
		AO->P	3.5	1.939	2.257	0.018	0.021
		E0->P	2.0	1.632	2.378	0.019	0.021
PBSCCS	24 mA bidi CMOS buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
		AO->P	3.5	1.939	2.257	0.018	0.021
		E0->P	2.0	1.632	2.378	0.019	0.021
PBSCT	24 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.007
		AO->P	3.5	1.939	2.257	0.018	0.021
		E0->P	2.0	1.632	2.378	0.019	0.021
PBSC1T	24 mA bidi TTL buffer (1)	P->AI0		0.733	1.050	0.014	0.010
		AO->P	3.0	2.843	3.010	0.025	0.025
		E0->P	3.0	2.824	3.273	0.025	0.025
PBSCTS	24 mA bidi TTL buffer with Schmitt Tigger (1)	P->AI0		1.479	2.768	0.019	0.007
		AO->P	3.5	1.939	2.257	0.018	0.021
		E0->P	2.0	1.632	2.378	0.019	0.021
PIC	CMOS input buffer (1)	P->AI0		0.843	1.070	0.007	0.003
PICI	CMOS inverting input buffer (1)	P->AI0		1.028	0.897	0.007	0.004
PICS	CMOS input buffer with Schmitt Trigger (1)	P->AI0		1.853	1.862	0.019	0.010
PIT	TTL input buffer (1)	P->AI0		0.733	1.050	0.014	0.007

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PITS	TTL input buffer with Schmitt Trigger (1)	P->AI0		1.479	2.768	0.019	0.010
PK8	16 mA clock driver (1)	I->O	6.5	0.579	0.715	0.001	0.001
PKC	24 mA clock driver (1)	I->O	6.5	0.612	0.957	0.001	0.001
PO1	2 mA output buffer (1)	AO->P	3.0	0.964	1.548	0.182	0.114
PO2	4 mA output buffer (1)	AO->P	3.0	1.072	1.006	0.091	0.068
PO2B	4 mA inverting output buffer (1)	AO->P	1.0	1.066	1.133	0.087	0.066
PO3	6 mA output buffer (1)	AO->P	3.0	1.276	1.228	0.061	0.046
PO4	8 mA output buffer (1)	AO->P	2.4	1.376	1.459	0.046	0.036
PO5	10 mA output buffer (1)	AO->P	3.0	1.503	1.592	0.037	0.031
PO6	12 mA output buffer (1)	AO->P	3.5	1.426	1.390	0.031	0.026
PO61	12 mA output buffer (1)	AO->P	5.0	1.962	2.050	0.032	0.029
PO7	14 mA output buffer (1)	AO->P	3.5	1.528	1.781	0.027	0.025
PO8	16 mA output buffer (1)	AO->P	3.5	1.642	1.579	0.024	0.022
POZ8B	16 mA open Crain inverting output buffer (1)	AO->P	1.0	0.000	1.316	0.000	0.100
PO9	18 mA output buffer (1)	AO->P	3.5	1.733	1.994	0.022	0.022
POA	20 mA output buffer (1)	AO->P	3.5	1.786	2.083	0.021	0.022

ATL80 - 0.8 μ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
POB	22 mA output buffer (1)	AO->P	3.5	1.868	2.174	0.019	0.021
POC	24 mA output buffer (1)	AO->P	3.5	1.939	2.257	0.018	0.021
PTD2	4 mA tristate output buffer (1)	AO->P	2.0	0.882	1.479	0.087	0.066
		E0->P	2.0	1.207	1.716	0.087	0.067
		E1->P	2.0	0.939	1.457	0.087	0.067
PTD3	6 mA tristate output buffer (1)	AO->P	2.0	1.029	1.648	0.058	0.046
		E0->P	2.0	1.351	1.897	0.058	0.047
		E1->P	2.0	1.084	1.628	0.058	0.047
PTD32	6 mA tristate output buffer (1)	AO->P	2.0	1.445	4.239	0.061	0.054
		E0->P	3.0	1.787	5.330	0.061	0.054
		E1->P	4.5	1.467	5.021	0.061	0.054
PTD5	10 mA tristate output buffer (1)	AO->P	2.0	1.290	1.929	0.036	0.032
		E0->P	2.0	1.592	2.215	0.036	0.032
		E1->P	2.0	1.325	1.952	0.036	0.032
PTS1	2 mA tristate output buffer (1)	AO->P	3.0	0.964	1.548	0.182	0.114
		E0->P	2.0	0.732	0.889	0.181	0.136
PTS2	4 mA tristate output buffer (1)	AO->P	3.0	1.072	1.006	0.091	0.068
		E0->P	2.0	0.848	1.117	0.091	0.068
PTS3	6 mA tristate output buffer (1)	AO->P	3.0	1.275	1.228	0.061	0.046
		E0->P	2.0	1.021	1.329	0.061	0.046
PTS31	6 mA tristate output buffer (1)	AO->P	5.0	1.608	2.304	0.061	0.041
		E0->P	2.0	1.252	2.548	0.061	0.041
PTS33	6 mA tristate output buffer (1)	AO->P	3.0	1.118	1.234	0.091	0.046
		E0->P	2.0	0.859	1.327	0.091	0.046
PTS4	8 mA tristate output buffer (1)	AO->P	3.0	1.376	1.459	0.046	0.036
		E0->P	2.5	1.411	2.095	0.046	0.038

ATL80 - 0.8 µ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PTS41	8 mA tristate output buffer (1)	AO->P E0->P	5.0 2.0	1.854 1.411	2.057 2.095	0.046 0.046	0.038 0.038
PTS5	10 mA tristate output buffer (1)	AO->P E0->P	3.0 2.5	1.503 1.450	1.592 1.670	0.037 0.037	0.031 0.030
PTS6	12 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.426 1.213	1.390 1.503	0.031 0.031	0.026 0.025
PTS63	12 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.112 0.854	1.401 1.478	0.060 0.061	0.025 0.026
PTS7	14 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.528 1.292	1.781 1.587	0.027 0.027	0.025 0.023
PTS8	16 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.642 1.396	1.579 1.696	0.024 0.024	0.022 0.022
PTS81	16 mA tristate output buffer (1)	AO->P E0->P	3.0 3.0	2.444 2.426	2.487 2.733	0.029 0.029	0.027 0.027
PTS9	18 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.733 1.460	1.994 1.790	0.022 0.022	0.022 0.020
PTSA	20 mA tristate output Buffer (1)	AO->P E0->P	3.5 2.0	1.786 1.523	2.083 2.201	0.021 0.021	0.022 0.022
PTSA6	20 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.538 1.189	2.053 2.160	0.030 0.031	0.022 0.022
PTSB	22 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.868 1.585	2.174 2.282	0.019 0.020	0.021 0.021
PTSC	24 mA tristate output buffer (1)	AO->P E0->P	3.5 2.0	1.939 1.632	2.257 2.378	0.018 0.019	0.021 0.021
PTSC1	24 mA tristate output buffer (1)	AO->P E0->P	3.0 3.0	2.843 2.824	3.010 3.273	0.025 0.025	0.025 0.025

ATL80 - 0.8 μ I/O Buffer Cells (Typical Delays at Tj = 25°C; Vdd = 5.0 V; Input Rise and Fall Times = 1 ns; Process = Nominal)

Cell Name	Description (Site Count)	Path	Input Load	Intercept Rising	Intercept Falling	Slope Rising	Slope Falling
PTSC2	24 mA tristate output buffer (1)	AO->P	3.0	1.815	3.092	0.090	0.021
		E0->P	3.0	1.546	3.239	0.091	0.025
PX2CL	4 mA crystal oscillator buffer (left side normalized input) (1)	PI->PO		1.108	1.433	0.060	0.068
		PI->AI0		0.843	1.070	0.007	0.003
PX2CR	4 mA crystal oscillator buffer (right side normalized input) (1)	PI->PO		1.108	1.433	0.060	0.068
		PI->AI0		0.843	1.070	0.007	0.003
PX4CL	8 mA crystal oscillator buffer (left side normalized input) (1)	PI->PO		1.618	1.991	0.032	0.036
		PI->AI0		0.843	1.070	0.007	0.003
PX4CR	8 mA crystal oscillator buffer (right side normalized input) (1)	PI->PO		1.618	1.991	0.032	0.036
		PI->AI0		0.843	1.070	0.007	0.003

PCI Buffer Description

Atmel has designed a PCI Buffer for the ATL80 array family. Designated PTSA6, this Tri-state output has 20mA pulldown and 12mA pullup when operating at 5 volts. The output can be combined with TTL inputs to create bidirectional pins. This buffer also meets the 3.3 volt PCI requirements; in this mode the output drive is rated at 10mA pulldown and 6mA pullup.

The chart below shows some performance data on the buffer taken from characterized silicon.

PCI Buffer Characterization Data

IOL = [FORCE = 0.6 x VDD, SPEC = (16mA to 64mA) x VDD]

VDD	Force	Spec	Temperature	Results
3.0 volts	1.80 volts	48mA to 192mA	0°C	71.6mA
3.3 volts	1.98 volts	52.8mA to 211.2mA	25°C	81.2mA
3.6 volts	2.16 volts	57.6mA to 230.4mA	70°C	88.1mA
4.75 to 5.25 volts	2.20 volts	95mA to 380mA	0°C to 70°C	135mA to 270mA

IOH = [FORCE = 0.3 x VDD, SPEC = (-12mA to -48mA) x VDD]

VDD	Force	Spec	Temperature	Results
3.0 volts	0.90 volts	-36mA to -144mA	0°C	-50.6mA
3.3 volts	0.99 volts	-39.6mA to -158.8mA	25°C	-58.4mA
3.6 volts	1.08 volts	-43.2mA to -172.8mA	70°C	-66.0mA
4.75 to 5.25 volts	1.40 volts	-40mA to -176mA	0°C to 70°C	-54mA to 109mA

Compiled (gate level) SRAMs

Atmel offers a variety of SRAMs compiled within the ATL80 series of gate arrays. These SRAMs utilize the standard metallization process, and are implemented using the gate array sites to form memory elements. The SRAMs are fully static with an active low write enable (WE). The SRAM architecture supports various architectures, including dual port, dual writes and SRAM enables.

Dual port SRAMs have two address inputs, a read address (RD_ADDR#) and a write address (WR_ADDR#). The output of the SRAM is the word pointed to by the read address. When WE goes low, the value at the data in bus is written to the word addressed by write address.

Dual write SRAMs have separate WE signals for the lower and upper part of a word. For example, an RAM8X16DW has two WE signals, one for the lower eight bits and one for the upper eight bits.

SRAMs with enables are useful for applications that are very power sensitive. When the chip is enabled, (CE = 0), the SRAMs operate as before. When the SRAM is disabled, however, the address decoders and output drivers are gated off (the output bus goes high).

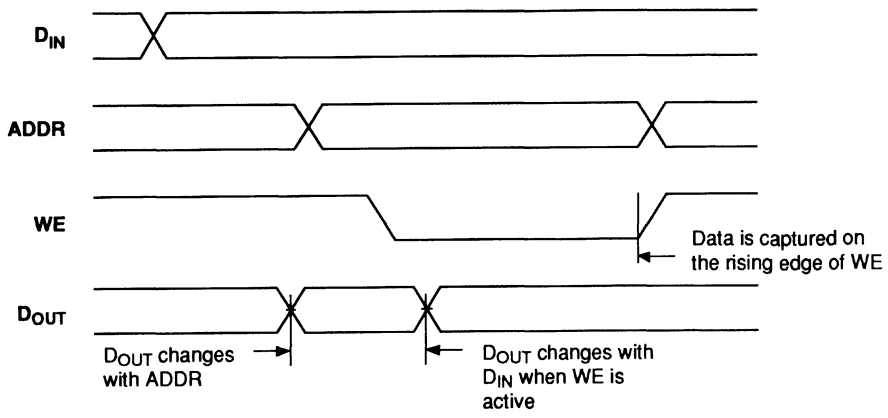
Enables are also useful for building deeper SRAMs out of smaller building blocks. For example, you can build a 128 x 16 SRAM by gating (NAND) the outputs of four SRAM 32 x 16 N blocks, and by decoding the upper two address bits section of the SRAM.

Logic simulation and static path models are supported within the tool sets. The structural SRAM netlist is provided with a custom back annotation file for correct delay calculation. The structural netlist represents the SRAM layout and as such provides the greatest modeling accuracy. This approach allows for simulation and static path analysis in the tool set.

Designing with the SRAM is a simple process of instantiating the SRAM within the design. When simulating the design, a special SRAM minicell library is referenced by the simulator as well as the design and SRAM netlist. The custom back annotation file is used within the tool delay calculator to generate accurate pin to pin timing. Setup, hold and width checks are made at the memory element level to insure proper SRAM timing.

The chart below lists the current SRAM blocks, the typical speed and the number of routing sites (gates) required to implement the SRAM. If the type of SRAM you require is not listed, check with your Atmel FAE. New SRAMs are being added continually and custom SRAMs can be easily developed.

SRAM	Speed (ns) ADDR to DATA	Sites	Description
RAM8X16	3.3	820	8 word - 16 bits/word SRAM
RAM8X16DW	2.9	984	8 word - 16 bits/word dual write
RAM8X72DP	4.0	3526	8 word - 72 bits/word dual port SRAM
RAM16X6	4.3	803	16 word - 6 bits/word SRAM
RAM32X16N	8.1	2835	32 word - 16 bits/word SRAM with enable



Effect of CE, when preset is to drive all D_{OUT} pins to 1 and disable address decoders.

RAM8X16 Specifications
8 X 16 Static RAM

Inputs:
3 Address (ADDR2, ADDR1, ADDR0)
1 Write Enable (WE), Active Low
16 Data In (DIN15 - DIN0)

Outputs:
16 Data Outputs (DOUT15 - DOUT0)

WE:
An active low write
WE = 0 write to current address
WE = 1 read current address
(Note: DOUT always reflects contents of current address)

Area:
20 columns x 41 rows
820 sites

Speed:

	Nom	WC Mil
ADDR# > DOUT	3.3	5.7
WE > DOUT	4.25	7.5
DIN# > DOUT	1.7	2.7

Pin Capacitance:

DIN#	2
ADDR#	2
WE	2

Output Drive:
DOUT# have the drive corresponding to an INV2 in the gate array library

RAM8X16DW Specifications
8 X 16 Dual Write Enable Static RAM

Inputs:
3 Address (ADDR2, ADDR1, ADDR0)
2 Write Enable (WE_LO, WE_HI), Active Low
16 Data In (DIN15 - DIN0)

Outputs:
16 Data Outputs (DOUT15 - DOUT0)

WE:
WE_LO, WE_HI are active low writes
WE_LO=0 write low byte (7:0) to current address
WE_LO=1 read current address (NOTE: DOUT always reflects contents of current address)
WE_HI=0 write hi byte (15:8) to current address
WE_HI=1 read current address (NOTE: DOUT always reflects contents of current address)

Area:
24 columns x 41 rows
984 sites
Flipped orientation

Speed:

	Nom	WC Mil
ADDR# > DOUT	2.9	4.8
WE* > DOUT	3.1	4.8
DIN# > DOUT	1.7	3.1

Pin Capacitance:

DIN#	2
ADDR#	7
WE*	2

Output Drive:
DOUT# have the drive corresponding to an INV2 in the gate array library

RAM8X72D Specifications
8 X 72 Dual Port Static RAM

Inputs:

3 Read Address Inputs (RD_ADDR2, RD_ADDR1, RD_ADDR0)
3 Write Address Inputs (WR_ADDR2, WR_ADDR1, WR_ADDR0)
1 Write Enable (WE), Active Low
72 Data In (DIN71 - DIN0)

Outputs:

72 Data Outputs (DOUT71 - DOUT0)

WE:

An active low write
WE = 0 write to current WR_ADDR address
WE = 1 write not active

DOUT always reflects the values in the memory location pointed to by RD_ADDR

Area:

86 columns x 41 rows
3526 sites
Flipped orientation

Speed:

	Nom	WC Mil
ADDR# > DOUT	4.0	7.3
WE > DOUT	4.72	7.7
DIN# > DOUT	1.61	2.42

Pin Capacitance:

DIN#	2
RD_ADDR#	2
WR_ADDR#	2
WE	3

Output Drive:

DOUT# have the drive corresponding to an INV2 in the gate array library

RAM16X6 Specifications
16 X 6 Static RAM

Inputs:

4 Address (ADDR3, ADDR2, ADDR1, ADDR0)
1 Write Enable (WE), Active Low
6 Data In (DIN5 - DIN0)

Outputs:

6 Data Outputs (DOUT5 - DOUT0)

WE:

An active low write
WE=0 write to current address
WE=1 read current address (NOTE: DOUT always reflects contents of current address)

Area:

11 columns x 73 rows
803 sites
Normal orientation

Speed:

	Nom	WC Mil
ADDR# > DOUT	4.3	7.1
WE > DOUT	4.5	8.8
DIN# > DOUT	2.7	4.8

Pin Capacitance:

DIN#	2
ADDR#	2
WE	2

Output Drive:

DOUT# have the drive corresponding to an INV2 in the gate array library

RAM32X16N Specifications
32 X 16 Static RAM with Enable

Inputs:

5 Address (ADDR4, ADDR3, ADDR2, ADDR1, ADDR0)
1 Write Enable (WE), Active Low
1 Chip Enable (CE), Active Low
16 Data In (DIN15 - DIN0)

Outputs:

16 Data Outputs (DOUT15 - DOUT0)

WE:

An active low write
WE=0 write to current address
WE=1 read current address (NOTE: when RAM enabled, DOUT always reflects contents of current address)

CE:

An active low enable
CE=0 chip is enabled
CE=1 chip is disabled. Outputs go hi and address decoders are disabled.

Area:

21 columns x 135 rows
2835 sites

Speed:

	Nom	WC Mil
ADDR# > DOUT	8.1	14.25
WE > DOUT	6.91	11.7
DIN# > DOUT	4.86	6.0

Pin Capacitance:

DIN#	2
ADDR#	2
WE	2
CE	3

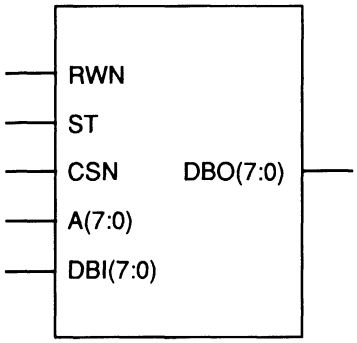
Output Drive:

DOUT# have the drive corresponding to an NAN2 in the gate array library

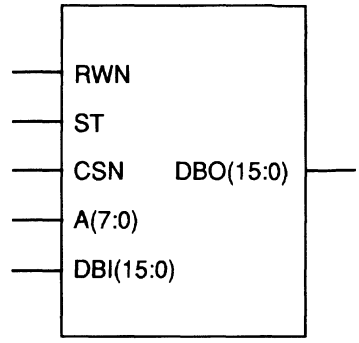
Embedded SRAM

In addition to the compiled (gate level) SRAM, Atmel offers a variety of embedded SRAM. These larger memories can not be implemented in a standard gate array, but require an embedded array. The embedded array incorporates the SRAM as a custom block, much like a standard cell. The memory block is surrounded by standard gates and a standard gate array I/O ring. This approach requires that a full custom mask set be built and wafers started from scratch for each design. The result is a higher NRE charge and a longer development and production cycle time compared to a standard gate array. The customer benefit is a lower production unit price due to the denser SRAM implementation of the embedded memory over the compiled (gate level) memory. Embedded memories are only suitable for high volume applications. The designer should be certain that an embedded array was proposed by Atmel prior to using one of the embedded SRAM cells.

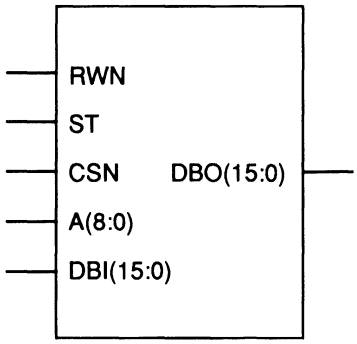
Embedded Single Port SRAM Pinouts



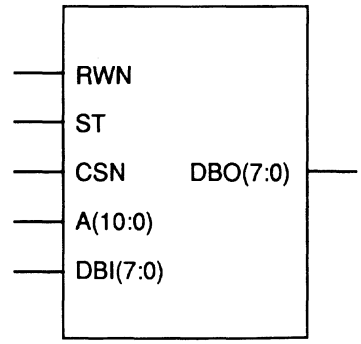
256 x 8 RAM



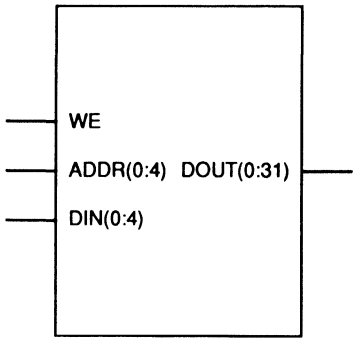
256 x 16 RAM



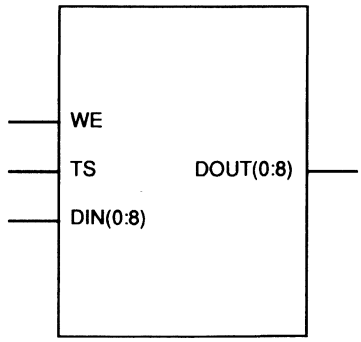
512 x 16 RAM



2K x 8 RAM



32 x 32 SRAM



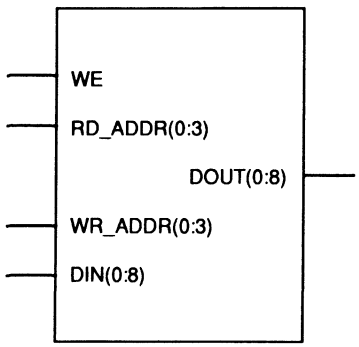
32 x 8 SRAM with Tri-state

The RAM cell does require a precharge prior to data read or write. This is done with the ST input, which, when strobed low, precharges all internal nodes to the proper levels for the next operation. Failure to precharge may result in loss of previously stored data.

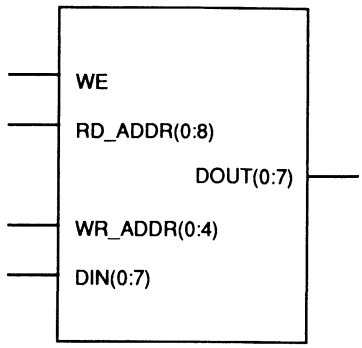
Pin Definitions:

A(1) - Address inputs to the decoding section of the RAM.
DBI(n) - Data bit inputs to be written into RAM.
DBO(n) - Data bit outputs to be read from RAM.
RWN - Read/Write control. When high, data is read from RAM and when low, data is written to RAM.
CSN - Chip Select Input. Active low input which enables any operation to happen within the RAM. When high, the RAM is disabled and the RAM goes into a low power mode, such that all circuitry after the input buffers is gated off.
ST - Strobe input. The read cycle can begin on the low to high transition, while data is written on the high-to-low transition. When ST is low, the RAM is in the precharge mode.

Embedded Dual Port SRAM Pinouts

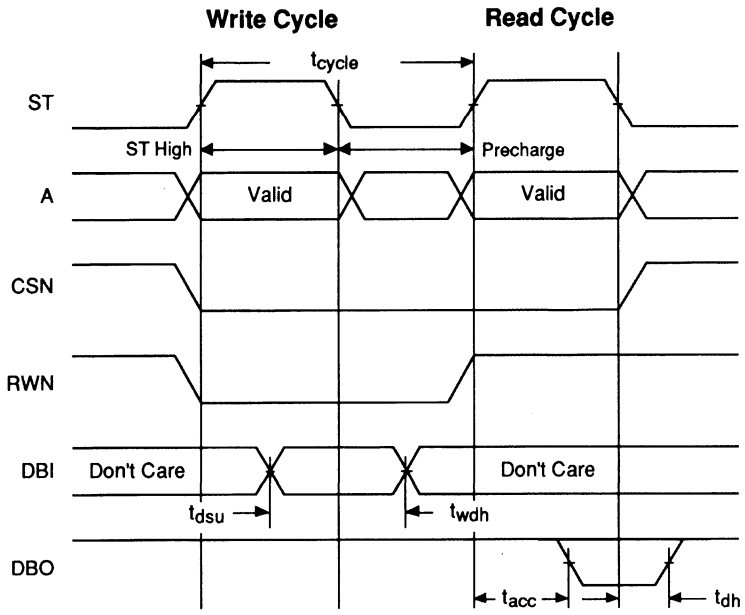


16 x 9 Dual Port SRAM

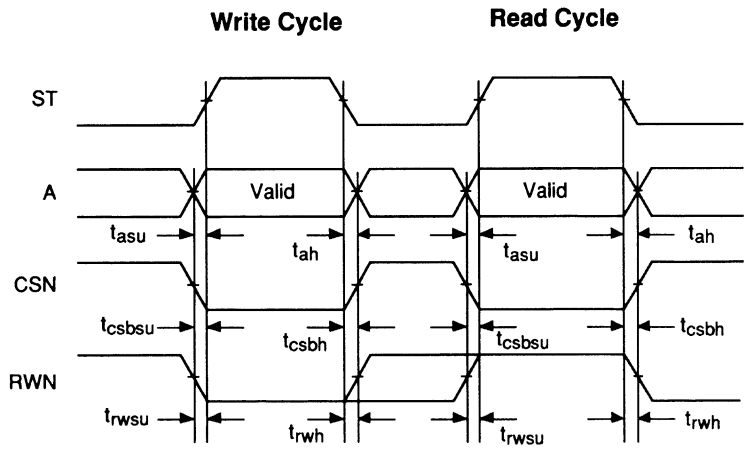


32 x 8 Dual Port SRAM

Read/Write Timing Diagram



Control Timing Diagram



SRAM SPICE Timing (256 x 8)

Symbol	Characteristics	3 Volt			5 Volt		
		Min V_{DD} - 3.3V Best Case Model 20°C	**Typ** V_{DD} - 3.0V Typical Model 25°C	**Max** V_{DD} - 2.7V Worst Case Model 70°C	**Min** V_{DD} - 5.5V Best Case Model 20°C	**Typ** V_{DD} - 5.0V Typical Model 25°C	**Max** V_{DD} - 2.7V Worst Case Model 705°C
t_{asu}	Address Setup Time (ns) A(1) to ST	0	0	0	0	0	0
t_{ah}	Address Hold Time (ns) ST to A(1)	0.9	2.2	3.2	0.9	1.1	2.1
t_{twsu}	Read/Write Setup Time (ns) RWB to ST	0	0	0	0	0	0
t_{rwh}	Read/Write Hold Time (ns) ST to RWB	0	0	0	0	0	0
t_{csbsu}	Chip Select Setup Time (ns) CSB to ST	0	0	0	0	0	0
t_{csbh}	Chip Select Hold Time (ns) ST to CSB	0	0	0	0	0	0
t_{dsu}	Write Data Setup Time (ns) DB1(n) to ST	1.4	2.4	4.0	1.1	1.6	2.3
t_{wdh}	Write Data Hold Time (ns) ST to DB1(n)	1.0	2.1	2.9	0.5	1.1	2
t_{acc}	Access Time (ns) ST(LH) to DB0(n)	5.35	8.4	16.4	3.7	5.6	9.2
t_{dh}	Data Out Hold Time (ns) ST(HL) to DB0(n)	4.6	8.4	14.3	3.4	5.1	7.9

These results obtained using META-SOFT H92B.01 SPICE, with ATMEL AT24K Transitor Models Dated 8/21/92

Specifications

	256 x 8	256 x 16	512 x 16	2K x 8
Operation	-20°C to +70°C	-20°C to +70°C	-20°C to +70°C	-20°C to +70°C
Max IDD0	100uA	100uA	100uA	200uA
Max IDD	0.23mA/MHz	0.35mA/MHz	0.55mA/MHz	1.0mA/MHz
Max Size	56 x 40 Mils	57 x 64 Mils	99 x 64 Mils	98 x 110 Mils
V_{DD}	2.7 VDC to 5.5 VDC	2.7 VDC to 5.5 VDC	2.7 VDC to 5.5 VDC	2.7 VDC to 5.5 VDC

Input Capacitance Per Line

Input	Capacitance
RWB	0.021 = 0.64 UL
ST	0.021 = 0.64 UL
CSB	0.021 = 0.64 UL
A(i)	0.094 = 2.65 UL
DB(i)	0.038 = 1.15 UL

V_{DD} = 4.5 to 5.5 VDC; TA = -20°C to +70°C

Symbol	Characteristics	256 x 8		256 x 16		512 x 16		2K x 8	
		Min	Max	Min	Max	Min	Max	Min	Max
t_{asu}	Address Setup Time (ns); A(i) to ST	0	0	0	0	0	0	0	0
t_{ah}	Address Hold Time (ns); ST to A(i)	0.9	2.1	0.8	1.9	0.6	2.3	1.3	2.5
t_{rwsu}	Read/Write Setup Time (ns); RWB to ST	0	0	0	0	0	0	0	0
t_{rwh}	Read/Write Hold Time (ns); ST to RWB	0	0	0	0	0	0	0	0
t_{csbsu}	Chip Select Setup Time (ns); CSB to ST	0	0	0	0	0	0	0	0
t_{csbh}	Chip Select Hold Time (ns); ST to CSB	0	0	0	0	0	0	0	0
t_{dsu}	Write Data Setup Time (ns); DB1(n) to ST	1.1	2.3	1.1	2.4	1.2	2.6	1.4	3.3
t_{wdh}	Write Data Hold Time (ns); ST to DB1(n)	0.5	2.0	0.6	2.2	0.7	2.2	0.8	2.2
t_{acc}	Access Time (ns); ST(HL) to DB0(n)	3.7	9.2	3.6	8.4	4.2	10.5	4.4	10.9
t_{dh}	Data Out Hold Time (ns); S(HL) to DB0(n)	3.4	7.9	3.4	8.2	3.9	9.1	3.9	9.2

V_{DD} = 2.7 to 3.3 VDC; TA = -20°C to +70°C

Symbol	Characteristics	256 x 8		256 x 16		512 x 16		2K x 8	
		Min	Max	Min	Max	Min	Max	Min	Max
t_{asu}	Address Setup Time (ns); A(i) to ST	0	0	0	0	0	0	0	0
t_{ah}	Address Hold Time (ns); ST to A(i)	0.9	3.2	1.0	3.2	1.0	3.0	1.5	3.6
t_{rwsu}	Read/Write Setup Time (ns); RWB to ST	0	0	0	0	0	0	0	0
t_{rwh}	Read/Write Hold Time (ns); ST to RWB	0	0	0	0	0	0	0	0
t_{csbsu}	Chip Select Setup Time (ns); CSB to ST	0	0	0	0	0	0	0	0
t_{csbh}	Chip Select Hold Time (ns); ST to CSB	0	0	0	0	0	0	0	0
t_{dsu}	Write Data Setup Time (ns); DB1(n) to ST	1.4	4.0	1.7	4.4	1.8	4.8	2.0	6.0
t_{wdh}	Write Data Hold Time (ns); ST to DB1(n)	1.0	2.9	0.9	3.8	1.0	4.3	1.1	3.9
t_{acc}	Access Time (ns); ST(HL) to DB0(n)	6.4	16.4	5.1	15.5	6.2	19.2	6.2	19.4
t_{dh}	Data Out Hold Time (ns); S(HL) to DB0(n)	4.64	14.3	4.9	14.3	5.7	16.7	5.7	16.5

Contents

Using the ATV750 and ATV750B

Introduction

This application note describes how to use the features of the ATV750 and ATV750B in the ABEL (and Atmel-ABEL) and CUPL (and Atmel-CUPL) high level description languages. The ATV750 and ATV750B are easy upgrades from a 22V10. They offer twice the logic density and more flexibility in the same footprint. Both devices have 20 registers and individual clock and AR product terms for each register. Each I/O pin has a programmable polarity control and an individual output enable product term. Independent feedback paths from each register allow all of the registers to be buried without wasting the I/O pins. For the ATV750B the registers can also be configured as D- or T-type and the clock can be selected as either a synchronous clock pin or a clock product term. The ATV750 and ATV750B macrocell is shown in Figure 1.

Device Names and Pin and Node Assignments

The device names for the ATV750 and ATV750B for each language are shown in Table 1.

Buried registers (Q1 in each macrocell) are identified by node numbers. Table 2 shows the node numbers for the Q1 registers in the ATV750 and ATV750B. Registers which are associated with the I/O pin (Q0 in each macrocell) are identified by the pin numbers. The use of the Q0 node numbers in CUPL is described in the Macrocell Configurations section.

Table 1. Device Names

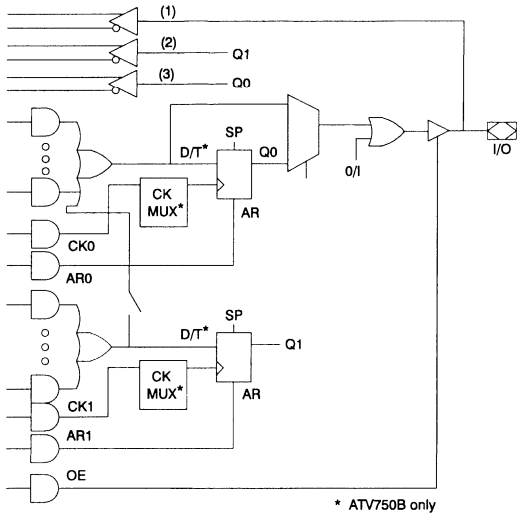
Device Type	ABEL Device Name	CUPL Device Name
ATV750 DIP	P750	V750
ATV750 PLCC	P750C	V750LCC
ATV750B DIP	P750B	V750B
ATV750B PLCC	P750BC	V750BLCC

Table 2. Node Numbers

Pin #	ABEL	CUPL	
	Q1	Q1	Q0
14(17)	26(30)	25(29)	35(39)
15(18)	27(31)	26(30)	36(40)
16(19)	28(32)	27(31)	37(41)
17(20)	29(33)	28(32)	38(42)
18(21)	30(34)	29(33)	39(43)
19(23)	31(35)	30(34)	40(44)
20(24)	32(36)	31(35)	41(45)
21(25)	33(37)	32(36)	42(46)
22(26)	34(38)	33(37)	43(47)
23(27)	35(39)	34(38)	44(48)

pin/node numbers: DIP(PLCC)

Figure 1. The ATV750 and ATV750B Macrocell



The following examples show the device type specification and the pin and node assignments:

ABEL and Atmel-ABEL

```
device_id device 'P750B'; "device_id will be used
                          "for JEDEC filename
I1,I2,I3,I4,I5 pin 1,2,3,4,5;
O23,O22 pin 23,22 istype 'reg_d,buffer';
O21,O20 pin 21,20 istype 'com';
O23Q1,O20Q1 node 35,32 istype 'reg_d';
```

CUPL and Atmel-CUPL

```
device V750B;
pin [1,2,3,4,5] = [I1,I2,I3,I4,I5];
pin [20,21,22,23] = [O20,O21,O22,O23];
pinnode [34,44,31] = [O23Q1,O23Q0,O20Q1];
```

Pin and Node Feedbacks

Each macrocell has three feedback paths into the array, one from each of the registers and one from the pin. For a buried register, the node name is used to refer to the feedback path. For a combinatorial output, the feedback comes from the pin, so the pin name is used to refer to the feedback. For a registered output, the feedback can come either from the register or from the pin. The feedback paths are labeled (1), (2), and (3) on Figure 1.

The following examples show how the different feedback paths are identified:

ABEL and Atmel-ABEL

```
O23.d = I1 # I2;
O23Q1.d = I1 & !I2;
O21 = O23      "(1)feedback from pin
    # O23.fb   "(2)feedback from Q0 register**
    # O23Q1;   "(3)feedback from buried register
```

**Note: for ABEL, either ".q" or ".fb" can be used to indicate the buried register feedback path. When ".q" extension is used, the software will select the Q output of the register, regardless of the output buffer polarity. When the ".fb" extension is used, the software will match the polarity of the register feedback with the output polarity by selecting either the Q or !Q output of the register.

CUPL and Atmel-CUPL

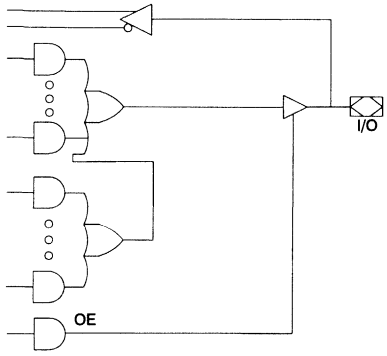
```
O23.d = I1 # I2;
O23Q1.d = I1 & !I2;
O21 = O23.io   /*(1)feedback from pin */
    # O23      /*(2)feedback from Q0 register */
    # O23Q1;   /*(3)feedback from buried register */
```

Macrocell Configurations

The basic macrocell configurations are shown in Figures 2 through 7. Each macrocell can be configured as either a registered or combinatorial output. In addition, each macrocell has a buried register. The multiple feedback paths also allow both registers to be buried, with the I/O pin used as an input pin.

The macrocells have a total of between 8 and 16 product terms. If the buried register is used, the product terms are automatically divided into two sum terms, each with half of the product terms. If the buried register is not used, all of the product terms are available for the I/O function.

Figure 2. Combinatorial Output



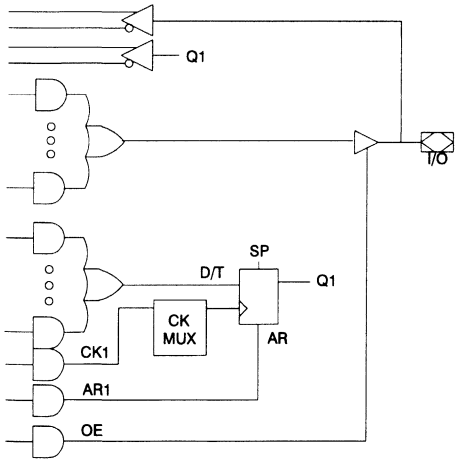
ABEL and Atmel-ABEL

```
O21 = I1 # !I2 # I3 # !I4 # I5;
```

CUPL and Atmel-CUPL

```
O21 = I1 # !I2 # I3 # !I4 # I5;
```

Figure 3. Combinatorial Output plus Buried Register



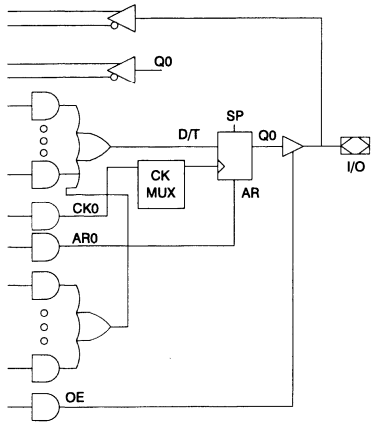
ABEL and Atmel-ABEL

```
O20 = I3 & !I4;
O20Q1.d = I2 # I3 # I4;
```

CUPL and Atmel-CUPL

```
O20 = I3 & !I4;
O20Q1.d = I2 # I3 # I4;
```

Figure 4. Registered Output



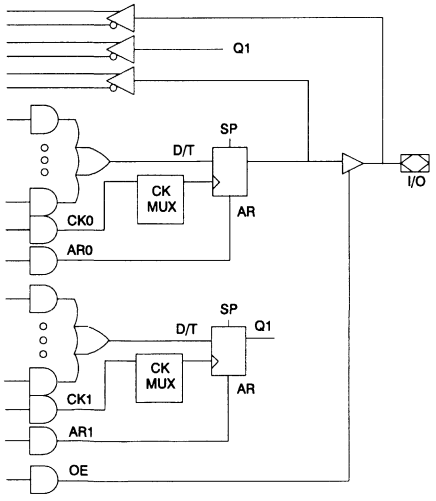
ABEL and Atmel-ABEL

```
O23.d = I1 # I2 # I3 # I4 # I5;
```

CUPL and Atmel-CUPL

```
O23.d = I1 # I2 # I3 # I4 # I5;
```

Figure 5. Registered Output plus Buried Register



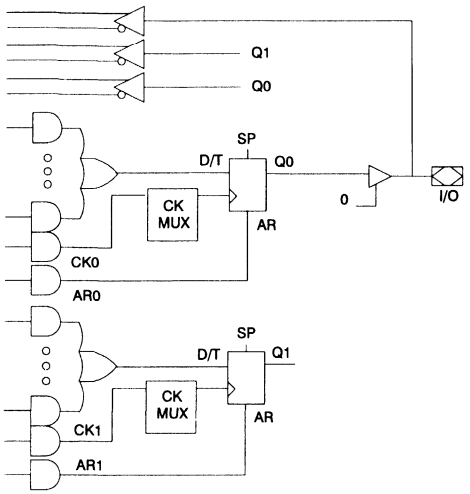
ABEL and Atmel-ABEL

```
O23.d = I1 & I2;
O23Q1.d = I3 & I4;
```

CUPL and Atmel-CUPL

```
O23.d = I1 & I2;
O23Q1.d = I3 & I4;
```

Figure 6. Both Registers Buried, I/O Pin Used as Input



ABEL and Atmel-ABEL

```
Declarations
O23 pin 23 istype 'reg_d';
O23Q1 node 35 istype 'reg_d';
INPUT_FUNC = O23;
REG_FUNC = O23.fb;

Equations
O23.d = INPUT_FUNC & I3;
O23.oe = 0;        "disable OE to use pin for input
O23Q1.d = REG_FUNC & I4;
```

CUPL and Atmel-CUPL

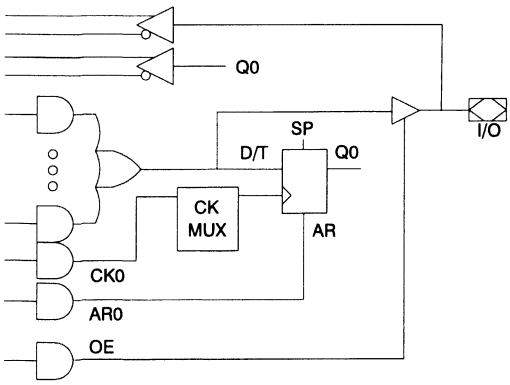
```
pin 23 = O23;
pinnode [34,44] = [O23Q1,O23Q0];
O23Q0.d = O23 & I3;
O23.oe = 'b'0;     /*disable OE to use pin for */
                   /*input */
O23Q1.d = O23Q0 & I4;
```

For ABEL, the Q1 register is identified by a node number. The Q0 register is identified by the pin number. The OE should be set to 0 to disable the outputs. The "pinname" (with no extensions) refers to the input path. The "pinname.fb" refers to the register feedback path. Another name for either the input or the register may be substituted in the Declarations section of the file, to make it clearer that they have separate functions. The pin and node names will be substituted back into the equations when the file is compiled.

For CUPL, there are node numbers for both the Q1 and Q0 registers. The Q0 node numbers should only be used if the Q0 register is buried and the pin is used as an input. The Q0 node name refers to the register and the pin name refers to the pin.

6

Figure 7. Combinatorial Output, Q0 Register Used to Latch Data



ABEL and Atmel-ABEL

```
O21 = I3;
O21.ck = CLK;
O23.d = O21.fb;  " registered O21 output
```

CUPL and Atmel-CUPL

```
O21 = I3;
O21.ck = CLK;
O23.d = O21.dfb; /* registered O21 output */
```

For this configuration, the output should be defined as combinatorial, and the equation written as combinatorial. A clock equation should also be written for the output. The registered signal which is fed back into the array is identified with ".fb" or ".q" for ABEL or ".dfb" for CUPL.

Asynchronous Reset, Synchronous Preset and Output Enable

There is an individual asynchronous reset product term for each register. A single synchronous preset product term is used to preset all registers. Since the synchronous preset requires a clock, an individual register will only preset if it is clocked. Each I/O pin has an individual output enable product term. The following examples show how the asynchronous reset, synchronous preset, and output enable functions are defined:

ABEL and Atmel-ABEL

```
O23.ar = I1;
O23.sp = I2;  "NOTE: preset is for all registers
O23.oe = I3 & I4;
O22.oe = 1;
```

CUPL and Atmel-CUPL

```
O23.ar = I1;
O23.sp = I2;  /*NOTE: preset is for all registers*/
O23.oe = I3 & I4;
O22.oe = 'b'1;
```

Programmable Polarity Control

Each I/O pin has programmable polarity control. Please refer to the application note "Using the Programmable Polarity Control" for details on using the polarity control.

Clock Options

For the ATV750, each register has an independent clock product term. For the ATV750B, each register can be configured to use either the clock product term or a synchronous clock pin (see Figure 8).

The following examples show how the clock is defined for the two different modes:

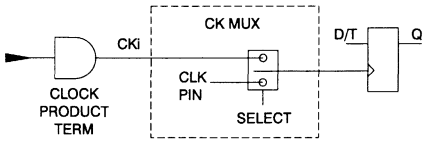
ABEL and Atmel-ABEL

```
SYNC_CLK pin 1;
ASYNC_CLK,EN pin 2,3;
O23.ck = SYNC_CLK;          "clock assigned to pin 1,
                            "no clock equation,
                            "software selects
                            "synchronous clock pin
                            "(for ATV750B only)
O23Q1.ck = ASYNC_CLK;       "clock assigned to pin 2,
                            "software selects clock
                            "product term
O22.ck = ASYNC_CLK & EN;    "clock uses product term,
                            "software selects clock
                            "product term
```

CUPL and Atmel-CUPL

```
pin 1 = SYNC_CLK;
pin [2,3] = [ASYNC_CLK,EN];
O23.ckmux = SYNC_CLK;       /*.ckmux extension */
                            /*selects synchronous */
                            /*clock pin */
                            /*(for ATV750B only) */
O23Q1.ck = SYNC_CLK;        /*.ck extension selects */
                            /*clock product term */
O22.ck = ASYNC_CLK & EN;
```

Figure 8. Clock Options



D-type or T-type Registers

For the ATV750, the registers can only be configured as D-type flip-flops. For the ATV750B, the registers can be configured as either D-type or T-type flip-flops. The following examples show how to configure the registers as either D- or T-type:

ABEL and Atmel-ABEL

```
O13 pin 13 istype 'reg_t';
O23.d = I1 & I2;
O13.t = I1 # I2;
```

CUPL and Atmel-CUPL

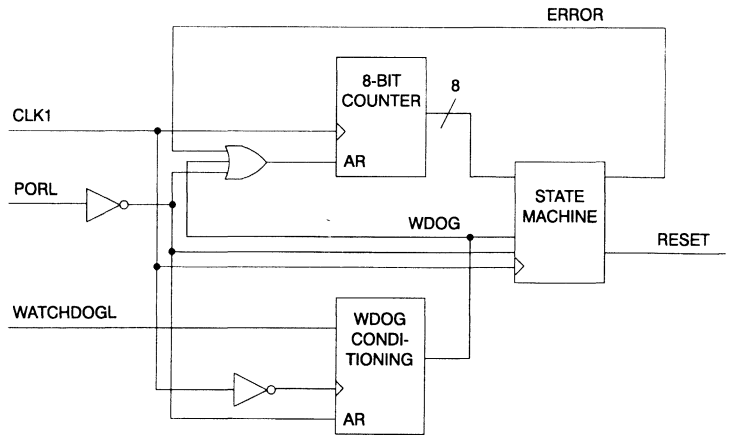
```
pin 13 = O13;
O23.d = I1 & I2;
O13.t = I1 # I2;
```

Design Example

Figure 9 shows a watchdog timer circuit which is implemented in an ATV750B. The circuit detects whether an event occurs at a regular interval. For this design, the timer is set to detect whether the WATCHDOGL input goes low every 18ms. An 8-bit counter running on a 1ms clock counts the number of clock cycles between events. A small state machine detects whether the event occurs within the expected window. If the event occurs either too soon or too late, an error is generated. If the event occurs during the window, the counter is reset to time the next event.

The ABEL and CUPL descriptions for this design follow.

Figure 9. Design Example



Example ABEL Description File

```
module WATCH;
title 'Watchdog Timer V750B Design Example
       ATMEL Corporation    March 27, 1995';

WATCH device 'P750B';

CLK1,WATCHDOGL,PORL       pin 1,2,3;
RESET,CLEARCOUNT          pin 23,22 istype 'com,buffer';
ERRPULSE,ERRPULSE2        pin 21,20 istype 'reg_d,buffer';
WDOG,WDOG2                pin 17,16 istype 'reg_d,buffer';
Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7   node 35,34,33,32,29,28,27,26 istype 'reg_t';
REGA, REGB                pin 18,19 istype 'reg_d,buffer';

COUNT8 = [Q7..Q0]; "8-bit counter

H,L,Z,C,K,X,U,D = 1,0,.Z.,.C.,.K.,.X.,.U.,.D.;

"Define state values
POWERUP =  ^B00;
IDLE    =  ^B10;
WAIT    =  ^B01;
ERROR   =  ^B11;

STATE_MACH = [REGB,REGA];

"Internal counter values used in state machine
" (these are 1 less than actual due to state machine delay)
LT18 = (COUNT8 < 16);
GT22 = (COUNT8 > 20);
MS256 = (COUNT8 == 255);

IRESET = (STATE_MACH == ERROR);

Equations

" For WATCHDOGL input, generate a 1 clock cycle wide pulse.
" Uses opposite edge of system clock from the state machine to
" insure that there are no setup or metastability problems between
" the inputs to the state machine and the state machine clock.
WDOG.d   = (!WATCHDOGL & !WDOG2.fb);
WDOG2.d  = (!WATCHDOGL);
WDOG.ck  = !CLK1;
WDOG2.ck = !CLK1;
WDOG.ar  = !PORL;
WDOG2.ar = !PORL;

" Generate 1 clock cycle wide error pulse upon entering ERROR
" state. Uses opposite clock edge from state machine to ensure
" error pulse generation is clean.
ERRPULSE.d   = (IRESET & !ERRPULSE2.fb);
ERRPULSE2.d  = IRESET;
ERRPULSE.ck  = !CLK1;
ERRPULSE2.ck = !CLK1;
ERRPULSE.ar  = !PORL;
ERRPULSE2.ar = !PORL;

"256mS Internal Timer
" (resets on power-up reset, watchdog input, or ERROR state)
CLEARCOUNT = (!PORL # WDOG # ERRPULSE.fb);
COUNT8.ck = CLK1;
COUNT8.ar = CLEARCOUNT;
```

```
COUNT8.t = (COUNT8 + 1) $ COUNT8;

RESET = (!PORL # IRESET); "external RESET output

"State machine clocks and resets
STATE_MACH.ck = CLK1;
STATE_MACH.ar = !PORL;

state_diagram STATE_MACH;

  state POWERUP:
   if (WDOG & !MS256) then IDLE;
     else if (MS256) then ERROR;
       else POWERUP;
  state IDLE:
   if (WDOG) then ERROR;
     else if (!LT18) then WAIT;
       else IDLE;
  state WAIT:
   if (WDOG) then IDLE;
     else if (!WDOG & GT22) then ERROR;
     else WAIT;
  state ERROR:
   if (MS256) then POWERUP;
     else ERROR;


"Test normal powerup and normal watchdog input
TEST_VECTORS (
[CLK1, PORL,WATCHDOGL] -> [STATE_MACH,COUNT8,RESET])
[ U,   0,   X        ] -> [POWERUP,   0,     1    ];
[ K,   1,   1        ] -> [POWERUP,   1,     0    ];
[ K,   1,   1        ] -> [POWERUP,   2,     0    ];
[ K,   1,   1        ] -> [POWERUP,   3,     0    ];
[ K,   1,   0        ] -> [IDLE,      0,     0    ];
@CONST CNT = 0;
@REPEAT 9 {
@CONST CNT = CNT + 1;
[ K,   1,   0        ] -> [   IDLE,   CNT,   0    ];}
@REPEAT 7 {
@CONST CNT = CNT + 1;
[ K,   1,   1        ] -> [IDLE,      CNT,   0    ];}
[ K,   1,   1        ] -> [WAIT,      17,    0    ];
[ K,   1,   1        ] -> [WAIT,      18,    0    ];
[ K,   1,   1        ] -> [WAIT,      19,    0    ];
[ K,   1,   0        ] -> [IDLE,      0,     0    ];
[ K,   1,   0        ] -> [IDLE,      1,     0    ];
[ K,   1,   0        ] -> [IDLE,      2,     0    ];


"Now test various state transitions and timeouts
TEST_VECTORS (
[CLK1, PORL,WATCHDOGL] -> [STATE_MACH,COUNT8,RESET])
[ U,   0,   X        ] -> [POWERUP,   0,     1    ];
[ K,   1,   1        ] -> [POWERUP,   1,     0    ];
[ K,   1,   1        ] -> [POWERUP,   2,     0    ];
[ K,   1,   1        ] -> [POWERUP,   3,     0    ];
[ K,   1,   0        ] -> [IDLE,      0,     0    ];
@CONST CNT = 0;
@REPEAT 15 {
@CONST CNT = CNT + 1;
[ K,   1,   1        ] -> [IDLE,      CNT,   0    ];}
[ K,   1,   1        ] -> [IDLE,      16,    0    ];
```

```
[ K,   1,   1        ] -> [WAIT,      17,    0    ];
[ K,   1,   1        ] -> [WAIT,      18,    0    ];
[ K,   1,   1        ] -> [WAIT,      19,    0    ];
[ K,   1,   1        ] -> [WAIT,      20,    0    ];
[ K,   1,   1        ] -> [WAIT,      21,    0    ];
[ K,   1,   1        ] -> [ERROR,     22,    1    ]; "Input doesn't happen
[ K,   1,   1        ] -> [ERROR,     0,     1    ];
[ K,   1,   1        ] -> [ERROR,     1,     1    ];
[ K,   0,   X        ] -> [POWERUP,   0,     1    ]; "RESET
[ K,   1,   1        ] -> [POWERUP,   1,     0    ];
[ K,   1,   0        ] -> [IDLE,      0,     0    ];
[ K,   1,   1        ] -> [IDLE,      1,     0    ];
[ K,   1,   0        ] -> [ERROR,     0,     1    ]; "Input hits too soon
[ K,   1,   1        ] -> [ERROR,     0,     1    ];
[ K,   1,   1        ] -> [ERROR,     1,     1    ];
[ U,   0,   1        ] -> [POWERUP,   0,     1    ];
@REPEAT 255 {                                      "Test POWERUP timeout
[ K,   1,   1        ] -> [POWERUP,   X,     0    ];}
@REPEAT 257 {                                      "Test ERROR timeout
[ K,   1,   1        ] -> [  ERROR,   X,     1    ];}
[ K,   1,   1        ] -> [POWERUP,   X,     0    ];
[ K,   1,   1        ] -> [POWERUP,   X,     0    ];
[ K,   1,   1        ] -> [POWERUP,   X,     0    ];

END WATCH;
```

Example CUPL Description File

```
Name            WATCH;
Partno          N/A;
Date            3/27/95;
Rev.            -;
Designer        Wendey Mueller;
Company         Atmel;
Assembly        -;
Location        -;
Device          V750B;

pin [1,2,3] = [CLK1,WATCHDOGL,PORL];
pin [23,22] = [RESET,CLEARCOUNT];
pin [21,20] = [ERRPULSE,ERRPULSE2];
pin [17,16] = [WDOG,WDOG2];
pin [18,19] = REGA, REGB;
pinnode [34,33,32,31,28,27,26,25] = [Q0..Q7];

field COUNT8 = [Q7..Q0]; /* 8-bit counter */

/* Define state values */
$define POWERUP 'b'00
$define IDLE    'b'10
$define WAIT    'b'01
$define ERROR   'b'11

field STATE_MACH = [REGB,REGA];

/* Internal counter values used in state machine */
/*  (these are 1 less than actual due to state machine delay) */
LT18 = COUNT8:[0..F];
GT22 = COUNT8:[15..FF];
MS256 = COUNT8:FF;

IRESET = STATE_MACH:ERROR;

/* Equations */

/* For WATCHDOGL input, generate a 1 clock cycle wide pulse.
Uses opposite edge of system clock from the state machine to
insure that there are no setup or metastability problems between
the inputs to the state machine and the state machine clock. */
WDOG.d   = (!WATCHDOGL & !WDOG2);
WDOG2.d  = (!WATCHDOGL);
WDOG.ck  = !CLK1;
WDOG2.ck = !CLK1;
WDOG.ar  = !PORL;
WDOG2.ar = !PORL;

/* Generate 1 clock cycle wide error pulse upon entering ERROR
state. Uses opposite clock edge from state machine to ensure
error pulse generation is clean. */
ERRPULSE.d   = (IRESET & !ERRPULSE2);
ERRPULSE2.d  = IRESET;
ERRPULSE.ck  = !CLK1;
ERRPULSE2.ck = !CLK1;
ERRPULSE.ar  = !PORL;
ERRPULSE2.ar = !PORL;

/* 256mS Internal Timer
(resets on power-up reset, watchdog input, or ERROR state) */
CLEARCOUNT = (!PORL # WDOG # ERRPULSE);
```

```
COUNT8.ck = CLK1;
COUNT8.ar = CLEARCOUNT;
Q0.t = 'b'1;
Q1.t = Q0;
Q2.t = Q1 & Q0;
Q3.t = Q2 & Q1 & Q0;
Q4.t = Q3 & Q2 & Q1 & Q0;
Q5.t = Q4 & Q3 & Q2 & Q1 & Q0;
Q6.t = Q5 & Q4 & Q3 & Q2 & Q1 & Q0;
Q7.t = Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0;

RESET = (!PORL # IRESET); /* external RESET output */

/* State machine clocks and resets */
STATE_MACH.ck = CLK1;
STATE_MACH.ar = !PORL;

sequence STATE_MACH {

  present POWERUP
   if (WDOG & !MS256) next IDLE;
   if (MS256) next ERROR;
   default next POWERUP;
  present IDLE
   if (WDOG) next ERROR;
   if (!WDOG & !LT18) next WAIT;
   default next IDLE;
  present WAIT
   if (WDOG) next IDLE;
   if (!WDOG & GT22) next ERROR;
   default next WAIT;
  present ERROR
   if (MS256) next POWERUP;
   default next ERROR;
}
```

```
CUPL Simulation Input File (WATCH.SI)
Name            WATCH;
Partno          N/A;
Date            3/27/95;
Rev.            -;
Designer        Wendey Mueller;
Company         Atmel;
Assembly        -;
Location        -;
Device          V750B;

ORDER: CLK1,%1,PORL,%1,WATCHDOGL,%2,STATE_MACH,%1,COUNT8,%1,RESET;
BASE: decimal;
VECTORS:
$MSG "Test normal powerup and normal watchdog input";
1 0 X  "0" "0"  H
K 1 1  "0" "1"  L
K 1 1  "0" "2"  L
K 1 1  "0" "3"  L
K 1 0  "2" "0"  L
$REPEAT 9;
K 1 0  "2" "*"  L
$REPEAT 7;
K 1 1  "2" "*"  L
K 1 1  "1" "17" L
K 1 1  "1" "18" L
```

```
K 1 1  "1" "19" L
K 1 0  "2" "0"  L
K 1 0  "2" "1"  L
K 1 0  "2" "2"  L

$MSG "Test various state transitions and timeouts";
1 0 X  "0" "0"  H
K 1 1  "0" "1"  L
K 1 1  "0" "2"  L
K 1 1  "0" "3"  L
K 1 0  "2" "0"  L
$REPEAT 15;
K 1 1  "2" "*"  L
K 1 1  "2" "16" L
K 1 1  "1" "17" L
K 1 1  "1" "18" L
K 1 1  "1" "19" L
K 1 1  "1" "20" L
K 1 1  "1" "21" L
K 1 1  "3" "22" H /*Input doesn't happen*/
K 1 1  "3" "0"  H
K 1 1  "3" "1"  H
K 0 X  "0" "0"  H /*RESET*/
K 1 1  "0" "1"  L
K 1 0  "2" "0"  L
K 1 1  "2" "1"  L
K 1 0  "3" "0"  H /*Input hits too soon*/
K 1 1  "3" "0"  H
K 1 1  "3" "1"  H
1 0 1  "0" "0"  H
$REPEAT 255;      /*Test POWERUP timeout*/
K 1 1  "0" "*"  L
$REPEAT 257;      /*Test ERROR timeout*/
K 1 1  "3" "*"  H
K 1 1  "0" "*"  L
K 1 1  "0" "*"  L
K 1 1  "0" "*"  L
```

Using the ATV2500 and ATV2500B

Introduction

This application note describes how to use the features of the ATV2500 and ATV2500B in the ABEL (and Atmel-ABEL) and CUPL (and Atmel-CUPL) high level description languages. The ATV2500 and ATV2500B are the most powerful programmable logic devices available in a 40/44-pin package. They combine high density and global routing, making them easy to use and understand. Both devices have 24 macrocells, each with three sum terms, two registers, and 17 product terms. Each register has individual clock and AR product terms. Each I/O pin has a programmable polarity control and an individual output enable product term. Independent feedback paths from each register allow all of the registers to be buried without wasting the I/O pins. A universal bus routes all input and feedback signals to all product terms on all macrocells. The ATV2500B has the additional features of D- or T-type configurable registers, three different clock options, and buried combinatorial nodes. The ATV2500 and ATV2500B macrocell is shown in Figure 1.

Device Names and Pin and Node Assignments

The device names for the ATV2500 and ATV2500B for each language are shown in Table 1.

The buried nodes (Q1 and Q2/F2 in each macrocell) are identified by node numbers, as shown in Table 2.

The following examples show the device type specification and the pin and node assignments:

ABEL and Atmel-ABEL

```
device_id device 'P2500B';
   "device_id will be used for
   "JEDEC filename
I1,I2,I3,I17,I18 pin 1,2,3,17,18;
O4,O5 pin 4,5 istype 'reg_d,buffer';
O6,O7 pin 6,7 istype 'com';
O4Q2,O7Q2 node 41,44 istype 'reg_d';
O6F2 node 43 istype 'com';
O7Q1 node 220 istype 'reg_d';
```

CUPL and Atmel-CUPL

```
device V2500B;
pin [1,2,3,17,18] = [I1,I2,I3,I17,I18];
pin [7,6,5,4] = [O7,O6,O5,O4];
pinnode [41,65,44] = [O4Q2,O4Q1,O7Q2];
pinnode [43,68] = [O6Q2,O7Q1];
```

Table 1. Device Names

Device Type	ABEL Device Name	CUPL Device Name
ATV2500 DIP	P2500	V2500
ATV2500 PLCC	P2500C	V2500LCC
ATV2500B DIP	P2500B	V2500B
ATV2500B PLCC	P2500BC	V2500BLCC

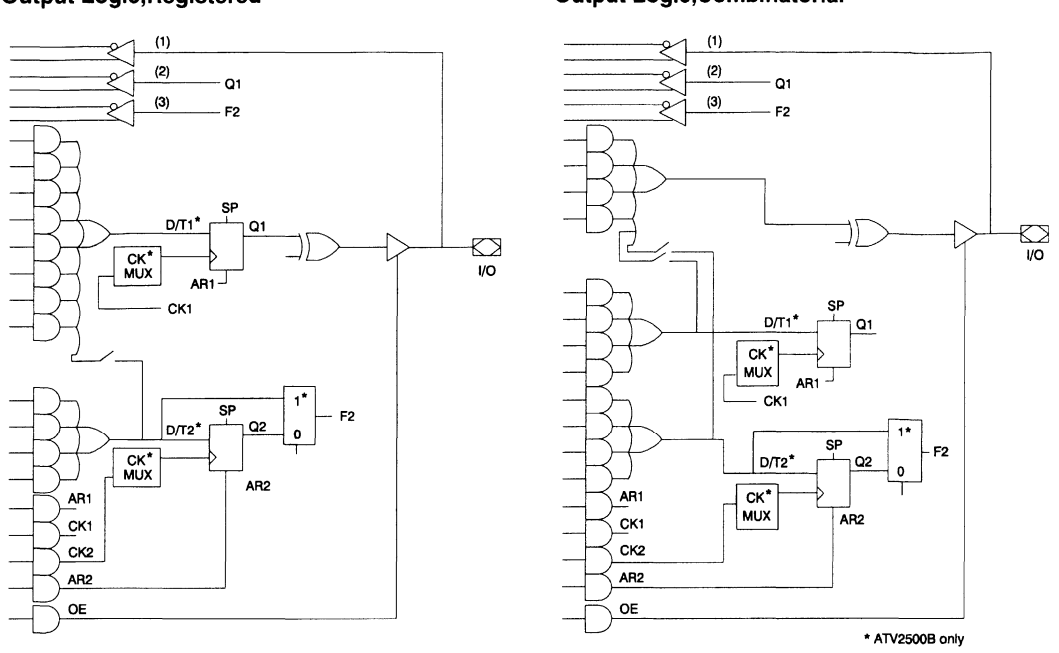
UV Erasable Programmable Logic Device

Application Note

6

0458A

Figure 1. The ATV2500 and ATV2500B Macrocell



Pin and Node Feedbacks

Each macrocell has three feedback paths into the array, one from each of the registers and one from the pin. For a buried node, the node name is used to refer to the feedback path. For a combinatorial output, the feedback comes from the pin, so the pin name is used to refer to the feedback. For a registered output, the feedback can come either from the register or from the pin. The feedback paths are labeled (1), (2), and (3) on Figure 1. The following examples show how the different feedback paths are identified:

ABEL and Atmel-ABEL

```
O4.d = I1 # I2;
O4Q2.d = I1 & !I2;
O6 = O4     "(1)feedback from pin
  # O4.fb   "(2)feedback from Q1 register**
  # O4Q2;   "(3)feedback from buried register
```

**Note: for ABEL, either ".q" or ".fb" can be used to indicate the buried register feedback path. When ".q" extension is used, the software will select the Q output of the register, regardless of the output buffer polarity. When the ".fb" extension is used, the software will match the polarity of the register feedback with the output polarity by selecting either the Q or !Q output of the register.

CUPL and Atmel-CUPL

```
O4.d = I1 # I2;
O4Q2.d = I1 & !I2;
O6 = O4.io   /*(1)feedback from pin */
  # O4       /*(2)feedback from Q1 register */
  # O4Q2;    /*(3)feedback from buried register */
```

Table 2. Node Numbers

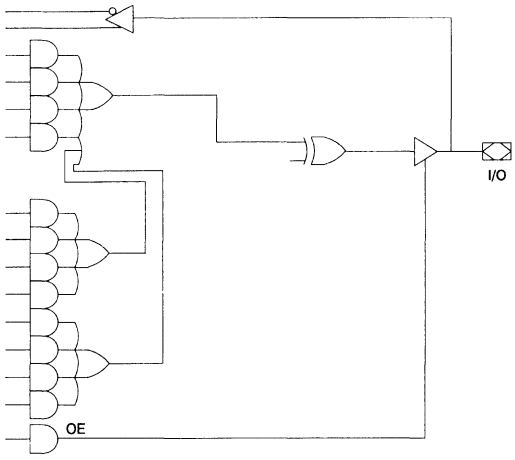
Pin #	ABEL		CUPL	
	Q1	Q2/F2	Q1	Q2/F2
4(5)	217(221)	41(45)	65(69)	41(45)
5(6)	218(222)	42(46)	66(70)	42(46)
6(7)	219(223)	43(47)	67(71)	43(47)
7(8)	220(224)	44(48)	68(72)	44(48)
8(9)	221(225)	45(49)	69(73)	45(49)
9(10)	222(226)	46(50)	70(74)	46(50)
11(13)	223(227)	47(51)	71(75)	47(51)
12(14)	224(228)	48(52)	72(76)	48(52)
13(15)	225(229)	49(53)	73(77)	49(53)
14(16)	226(230)	50(54)	74(78)	50(54)
15(17)	227(231)	51(55)	75(79)	51(55)
16(18)	228(232)	52(56)	76(80)	52(56)
24(27)	229(233)	53(57)	77(81)	53(57)
25(28)	230(234)	54(58)	78(82)	54(58)
26(29)	231(235)	55(59)	79(83)	55(59)
27(30)	232(236)	56(60)	80(84)	56(60)
28(31)	233(237)	57(61)	81(85)	57(61)
29(32)	234(238)	58(62)	82(86)	58(62)
31(35)	235(239)	59(63)	83(87)	59(63)
32(36)	236(240)	60(64)	84(88)	60(64)
33(37)	237(241)	61(65)	85(89)	61(65)
34(38)	238(242)	62(66)	86(90)	62(66)
35(39)	239(243)	63(67)	87(91)	63(67)
36(40)	240(244)	64(68)	88(92)	64(68)

Pin/node numbers: DIP(PLCC)

Macrocell Configurations

The basic macrocell configurations are shown in Figures 2 through 9. Each macrocell has three sum terms, each with four product terms. The sum terms can be combined for wider fan-in functions or separated and used for buried logic. The output can be configured as either combinatorial or registered. For a combinatorial output, the other two sum terms can be connected to buried registers. For a registered output, two of the sum terms are combined for the output and the third can be connected to a buried register. The multiple feedback paths also allow both registers to be buried, with the I/O pin used as an input pin. For the ATV2500B, the Q2 node can also be configured as a buried combinatorial node, F2, as shown in Figure 9.

Figure 2. Combinatorial Output (12 product terms)



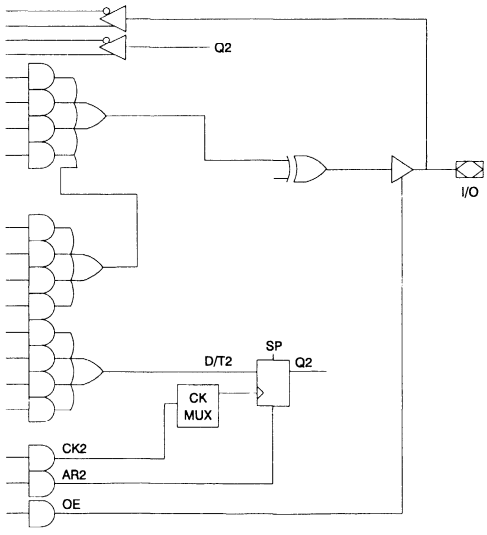
ABEL and Atmel-ABEL

```
O6 = I1 # !I2 # I3 # !I17 # I18;
```

CUPL and Atmel-CUPL

```
O6 = I1 # !I2 # I3 # !I17 # I18;
```

Figure 3. Combinatorial Output (8 product terms) plus Buried Register (4 product terms)



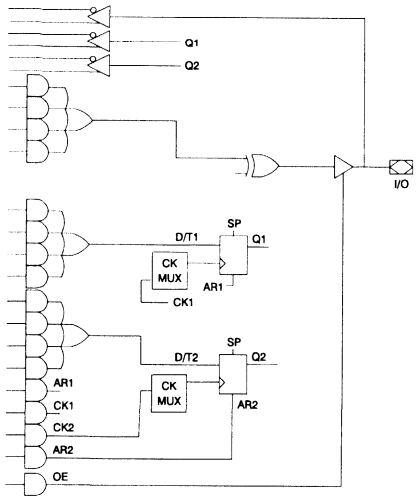
ABEL and Atmel-ABEL

```
O7 = I1 # !I2 # I3 # !I17 # I18;
O7Q2.d = I2 # I3 # I17;
```

CUPL and Atmel-CUPL

```
O7 = I1 # !I2 # I3 # !I17 # I18;
O7Q2.d = I2 # I3 # I17;
```

Figure 4. Combinatorial Output (4 product terms) plus 2 Buried Registers (4 product terms each)



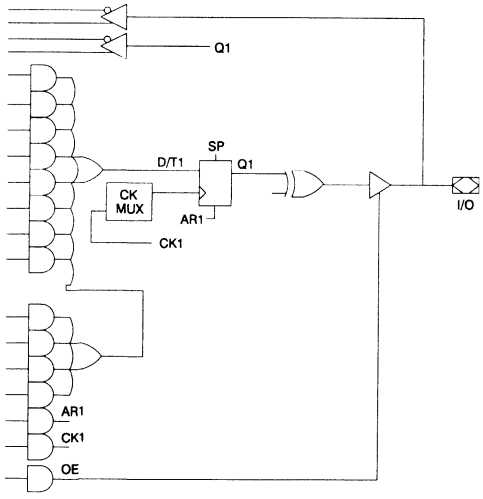
ABEL and Atmel-ABEL

```
O7 = I3 & !I17;
O7Q1.d = I1 & I2;
O7Q2.d = I2 # I3 # I17;
```

CUPL and Atmel-CUPL

```
O7 = I3 & !I17;
O7Q1.d = I1 & I2;
O7Q2.d = I2 # I3 # I17;
```

Figure 5. Registered Output (12 product terms)



ABEL and Atmel-ABEL

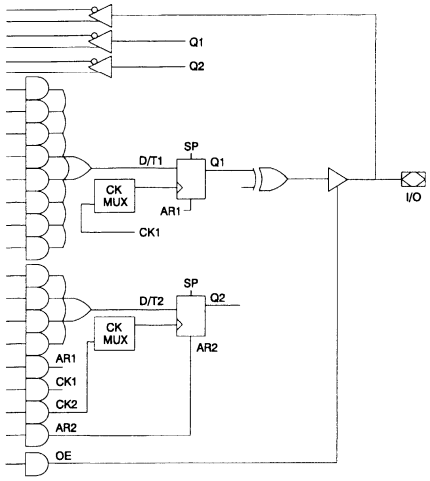
```
O4.d = I1 # I2 # I3 # I17 # I18;
```

CUPL and Atmel-CUPL

```
O4.d = I1 # I2 # I3 # I17 # I18;
```

6

Figure 6. Registered Output (8 product terms) plus Buried Register (4 product terms)



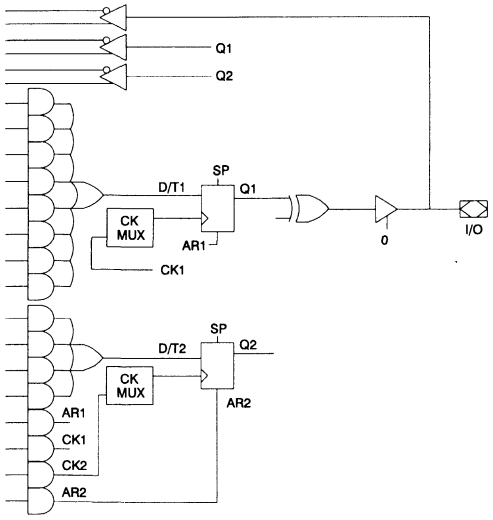
ABEL and Atmel-ABEL

```
O4.d = I1 & I2;
O4Q2.d = I3 & I17;
```

CUPL and Atmel-CUPL

```
O4.d = I1 & I2;
O4Q2.d = I3 & I17;
```

Figure 7. Both Registers Buried (Q1 - 8 product terms, Q2 - 4 product terms), I/O Pin Used as Input



ABEL and Atmel-ABEL

```
Declarations
O4 pin 4 istype 'reg_d';
O4Q2 node 41 istype 'reg_d';
INPUT_FUNC = O4;
REG_FUNC = O4.fb;

Equations
O4.d = INPUT_FUNC & I3;
O4.oe = 0;      "disable OE to use pin for input
O4Q2.d = REG_FUNC & I17;
```

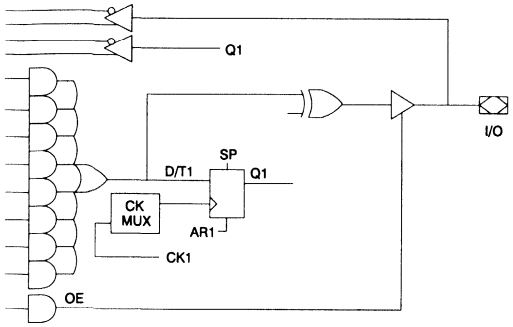
CUPL and Atmel-CUPL

```
pin 4 = O4;
pinnode [41,65] = [O4Q2,O4Q1];
O4Q1.d = O4 & I3;
O4.oe = 'b'0;  /*disable OE to use pin for input */
O4Q2.d = O4Q0 & I17;
```

For ABEL, the Q2 register is identified by a node number. The Q1 register is identified by the pin number (the Q1 node numbers should only be used for the configuration shown in Figure 4). The OE should be set to 0 to disable the outputs. The "pinname" (with no extensions) refers to the input path. The "pinname.fb" or "pinname.q" refers to the register feedback path. Another name for either the input or the register may be substituted in the Declarations section of the file, to make it clearer that they have separate functions. The pin and node names will be substituted back into the equations when the file is compiled.

For CUPL, there are node numbers for both the Q2 and Q1 registers. The Q1 node name refers to the register and the pin name refers to the pin.

Figure 8. Combinatorial Output, Q1 Register Used to Latch Data



ABEL and Atmel-ABEL

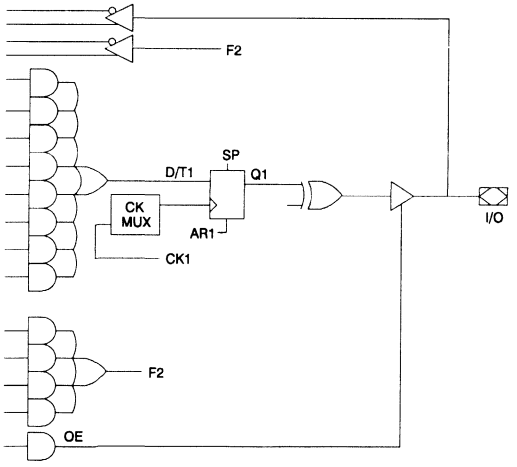
```
O6 = I3;
O6.ck = CLK;
O4.d = O6.fb;  "registered O6 output
```

CUPL and Atmel-CUPL

```
O6 = I3;
O6.ck = CLK;
O4.d = O6.dfb; /* registered O6 output */
```

For this configuration, the output should be defined as combinatorial, and the equation written as combinatorial. A clock equation should also be written for the output. The registered signal which is fed back into the array is identified with ".fb" or ".q" for ABEL or ".dfb" for CUPL.

Figure 9. ATV2500B ONLY: Registered or Combinatorial Output plus Buried Combinatorial Node (4 product terms)



ABEL and Atmel-ABEL

```
Declarations
O4 pin 4 istype 'reg_d';
O4F2 node 41 istype 'com';

Equations
O4.d = I2 & I3;
O4F2 = I17 & I18;
```

CUPL and Atmel-CUPL

```
pin 4 = O4;
pinnode 41 = O4F2;
O4.d = I2 & I3;
O4F2 = I17 & I18;
```

Asynchronous Reset, Synchronous Preset, and Output Enable

There is an individual asynchronous reset product term for each register. Each I/O pin has an individual output enable product term. There are eight synchronous preset product terms which are used to preset banks of four or eight registers. Table 3 shows the groups of registers connected to each of the synchronous preset product terms. Since the synchronous preset requires a clock, an individual register will only preset if it is clocked.

The following examples show how the asynchronous reset, synchronous preset, and output enable functions are defined:

ABEL and Atmel-ABEL

```
O4.ar = I1;
O4.sp = I2;  "NOTE: preset is for 8 registers
O4.oe = I3 & I17;
O5.oe = 1;
```

CUPL and Atmel-CUPL

```
O4.ar = I1;
O4.sp = I2;  /*NOTE: preset is for 8 registers */
O4.oe = I3 & I17;
O5.oe = 'b'1;
```

Programmable Polarity Control

Each I/O pin has programmable polarity control. Please refer to the application note "Using the Programmable Polarity Control" for details on using the polarity control.

Clock Options

For the ATV2500, each register has an independent clock product term. For the ATV2500B, each register can be configured to use either the clock product term, a synchronous clock pin, or a gated synchronous clock (see Figure 10).

The following examples show how the clock is defined for the different modes:

ABEL and Atmel-ABEL

```
SYNC_CLK pin 1;
ASYNC_CLK,EN pin 2,3;
O4.ck = 1;              "synchronous clock pin
                        "(for ATV2500B only)
O4.ce = SYNC_CLK;
O4Q2.ck = I2 & EN;      "synchronous clock pin ANDed
                        "with clock product term
O4Q2.ce = SYNC_CLK;     "(for ATV2500B only)
O5.ck = ASYNC_CLK & EN; "clock product term
```

CUPL and Atmel-CUPL

```
pin 1 = SYNC_CLK;
pin [2,3] = [ASYNC_CLK,EN];
O4.ce = 'b'1;           /*synchronous clock pin */
                        /*(for ATV2500B only) */
O4Q2.ce = I2 & EN;      /*synchronous clock pin */
                        /*ANDed with clock product */
                        /*term (for ATV2500B only) */
O5.ck = ASYNC_CLK & EN; /*clock product term */
```

D-type or T-type Registers

For the ATV2500, the registers can only be configured as D-type flip-flops. For the ATV2500B, the registers can be configured as either D-type or T-type flip-flops. The following examples show how to configure the registers as either D- or T-type:

ABEL and Atmel-ABEL

```
O13 pin 13 istype 'reg_t';
O4.d = I1 & I2;
O13.t = I1 # I2;
```

CUPL and Atmel-CUPL

```
pin 13 = O13;
O4.d = I1 & I2;
O13.t = I1 # I2;
```

Figure 10. Clock Options

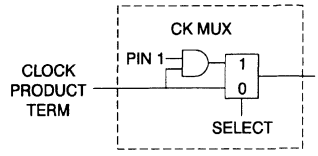


Table 3. Synchronous Preset Groups

Preset PT	DIP Pin Number + Q1, Q2 Register
SP0	4Q1,4Q2,5Q1,5Q2,6Q1,6Q2,7Q1,7Q2
SP1	8Q1,8Q2,9Q1,9Q2
SP2	33Q1,33Q2,34Q1,34Q2,35Q1,35Q2,36Q1,36Q2
SP3	31Q1,31Q2,32Q1,32Q2
SP4	13Q1,13Q2,14Q1,14Q2,15Q1,15Q2,16Q1,16Q2
SP5	11Q1,11Q2,12Q1,12Q2
SP6	24Q1,24Q2,25Q1,25Q2,26Q1,26Q2,27Q1,27Q2
SP7	28Q1,28Q2,29Q1,29Q2

Example ABEL Description File

```
module use2500b;
title 'ATV2500B Example ABEL File
       Atmel Corp.    3/27/95'
use2500b device 'P2500BC';

declarations

"T Counter
SCLK,LD,RST              pin 1,2,3;
I0,I1,I2,I3,I4,I5,I6,I7 pin 19,20,21,22,23,24,25,41;
Q0,Q1,Q2,Q3,Q4,Q5,Q6,Q7 node 45,46,47,48,49,50,51,52 istype 'reg_t';

"Grey code counter
ACLK,HOLD,OE             pin 42,43,44;
G3,G2,G1,G0              pin 5,6,7,8 istype 'reg_d,buffer';

"Seven segment display decoder
seg1,seg2,seg3,seg4      pin 9,10,13,14 istype 'com';
seg5,seg6,seg7           pin 15,16,17 istype 'com';

"Shift register
S_RST,S_LD,S_IN          pin 38,39,40;
S0,S1,S2,S3,S4,S5,S6     node 53,54,55,56,57,58,59 istype 'reg_d';
S_OUT                    pin 27 istype 'reg_d,buffer';

H,L,C,X,Z,P = 1,0,.C.,.X.,.Z.,.P.;

INPUTS = [I7..I0]; "Input data
T_CNT = [Q7..Q0];  "T counter
GCODE = [G3,G2,G1,G0]; "Grey code counter
SHIFT = [S_OUT,S6,S5,S4,S3,S2,S1,S0]; "Shift register
SHIFT1 = [S6,S5,S4,S3,S2,S1,S0,S_IN];

equations

"T Counter
T_CNT.t = ((T_CNT + 1) $ T_CNT) & !LD    "count
        # (T_CNT $ INPUTS) & LD;         "load
T_CNT.ck = ^hFF;
T_CNT.ce = SCLK;             "synchronous clock mode
T_CNT.ar = RST;

"Shift register
SHIFT.d = SHIFT1 & !S_LD     "shift
        # INPUTS & S_LD;     "load
SHIFT.ck = ACLK;             "product term clock mode
SHIFT.ar = S_RST;

"Grey code counter
GCODE.ck = !HOLD;            "gated synchronous clock mode
GCODE.ce = SCLK;
GCODE.ar = RST;
GCODE.oe = OE;

"State machine will use .q feedback
STATE_DIAGRAM GCODE
state [0,0,0,0]: goto [0,0,0,1];
state [0,0,0,1]: goto [0,0,1,1];
state [0,0,1,1]: goto [0,0,1,0];
state [0,0,1,0]: goto [0,1,1,0];
```

```
state [0,1,1,0]: goto [0,1,1,1];
state [0,1,1,1]: goto [0,1,0,1];
state [0,1,0,1]: goto [0,1,0,0];
state [0,1,0,0]: goto [1,1,0,0];
state [1,1,0,0]: goto [1,1,0,1];
state [1,1,0,1]: goto [1,1,1,1];
state [1,1,1,1]: goto [1,1,1,0];
state [1,1,1,0]: goto [1,0,1,0];
state [1,0,1,0]: goto [1,0,1,1];
state [1,0,1,1]: goto [1,0,0,1];
state [1,0,0,1]: goto [1,0,0,0];
state [1,0,0,0]: goto [0,0,0,0];

"Seven segment display decoder
"Use register feedback path
truth_table (
[GCODE.fb] -> [seg1,seg2,seg3,seg4,seg5,seg6,seg7])
[  0     ] -> [ 1,   0,   1,   1,   1,   1,   1  ];
[  1     ] -> [ 0,   0,   0,   1,   1,   0,   0  ];
[  2     ] -> [ 1,   1,   1,   1,   0,   0,   1  ];
[  3     ] -> [ 1,   1,   1,   1,   1,   0,   0  ];
[  4     ] -> [ 0,   1,   0,   1,   1,   1,   0  ];
[  5     ] -> [ 1,   1,   1,   0,   1,   1,   0  ];
[  6     ] -> [ 1,   1,   1,   0,   1,   1,   1  ];
[  7     ] -> [ 1,   0,   0,   1,   1,   0,   0  ];
[  8     ] -> [ 1,   1,   1,   1,   1,   1,   1  ];
[  9     ] -> [ 1,   1,   0,   1,   1,   1,   0  ];
[  10    ] -> [ 1,   1,   0,   1,   1,   1,   1  ];
[  11    ] -> [ 0,   1,   1,   0,   1,   1,   1  ];
[  12    ] -> [ 1,   0,   1,   0,   0,   1,   1  ];
[  13    ] -> [ 0,   1,   1,   1,   1,   0,   1  ];
[  14    ] -> [ 1,   1,   1,   0,   0,   1,   1  ];
[  15    ] -> [ 1,   1,   0,   0,   0,   1,   1  ];

@RADIX16;
@CONST CNT = 0;

TEST_VECTORS (
[SCLK,RST,LD,INPUTS]->[T_CNT]);
[0,   1,  0, 000   ]->[000  ];
@REPEAT OFF{
@CONST CNT=CNT+1;
[C,   0,  0, 000   ]->[CNT  ];}
[C,   0,  1, 0AB   ]->[0AB  ];
[C,   0,  0, 000   ]->[0AC  ];

TEST_VECTORS (
[SCLK,HOLD,RST,OE]-[G3,G2,G1,G0,seg1,seg2,seg3,seg4,seg5,seg6,seg7])
[ 0,  0,   1,  1 ]->[0, 0, 0, 0,  1,   0,   1,   1,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[0, 0, 0, 1,  0,   0,   0,   1,   1,   0,   0  ];
[ C,  0,   0,  1 ]->[0, 0, 1, 1,  1,   1,   1,   1,   1,   0,   0  ];
[ C,  0,   0,  1 ]->[0, 0, 1, 0,  1,   1,   1,   1,   0,   0,   1  ];
[ C,  0,   0,  1 ]->[0, 1, 1, 0,  1,   1,   1,   0,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[0, 1, 1, 1,  1,   0,   0,   1,   1,   0,   0  ];
[ C,  0,   0,  1 ]->[0, 1, 0, 1,  1,   1,   1,   0,   1,   1,   0  ];
[ C,  0,   0,  1 ]->[0, 1, 0, 0,  0,   1,   0,   1,   1,   1,   0  ];
[ C,  0,   0,  1 ]->[1, 1, 0, 0,  1,   0,   1,   0,   0,   1,   1  ];
[ C,  0,   0,  1 ]->[1, 1, 0, 1,  0,   1,   1,   1,   1,   0,   1  ];
[ C,  0,   0,  1 ]->[1, 1, 1, 1,  1,   1,   0,   0,   0,   1,   1  ];
[ C,  0,   0,  1 ]->[1, 1, 1, 0,  1,   1,   1,   0,   0,   1,   1  ];
[ C,  0,   0,  1 ]->[1, 0, 1, 0,  1,   1,   0,   1,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[1, 0, 1, 1,  0,   1,   1,   0,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[1, 0, 0, 1,  1,   1,   0,   1,   1,   1,   0  ];
```

```
[ C,  0,   0,  1 ]->[1, 0, 0, 0,  1,   1,   1,   1,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[0, 0, 0, 0,  1,   0,   1,   1,   1,   1,   1  ];
[ C,  0,   0,  1 ]->[0, 0, 0, 1,  0,   0,   0,   1,   1,   0,   0  ];
[ C,  1,   0,  1 ]->[0, 0, 0, 1,  0,   0,   0,   1,   1,   0,   0  ];
[ C,  0,   0,  0 ]->[Z, Z, Z, Z,  1,   1,   1,   1,   1,   0,   0  ];

TEST_VECTORS (
[ACLK,S_LD,S_RST,S_IN,INPUTS]-[S0,S1,S2,S3,S4,S5,S6,S_OUT])
[ 0,   0,   1,    0,    000   ]->[0, 0, 0, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 0, 0, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 1, 0, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 1, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 1, 0, 0, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 0, 1, 0, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 0, 0, 1, 0, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 0, 0, 0, 1, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 0, 0, 0, 0, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 0, 0, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 0, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 0, 0, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 0, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 0, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 1, 0, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 1, 1, 0    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    0,    000   ]->[0, 1, 1, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 0, 1, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 0, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 0, 1, 1, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 0, 1, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 0, 1, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 1, 0, 1    ];
[ C,   0,   0,    1,    000   ]->[1, 1, 1, 1, 1, 1, 1, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 1, 1, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 1, 1, 1, 1, 1, 1    ];
[ C,   0,   0,    0,    000   ]->[0, 0, 0, 1, 1, 1, 1, 1    ];
[ C,   1,   0,    0,    055   ]->[1, 0, 1, 0, 1, 0, 1, 0    ];
[ C,   0,   0,    0,    000   ]->[0, 1, 0, 1, 0, 1, 0, 1    ];

END
```

Example CUPL Description File

```
Name        USE2500B;
Partno      N/A;
Date        3/27/95;
Rev.        -;
Designer    Wendey Mueller;
Company     Atmel;
Assembly    -;
Location    -;
Device      V2500BLCC;

/* Example V2500B CUPL file */

/* T Counter */
pin [1,2,3] = SCLK,LD,RST;
pin [19..25,41] = [I0..I7];
pinnode [45..52] = [Q0..Q7];

/* Grey code counter */
pin [42,43,44] = [ACLK,HOLD,OE];
pin [5..8] = [G3..G0];

/* Seven segment display decoder */
pin [9,10,13..17] = [1seg,2seg,3seg,4seg,5seg,6seg,7seg];

/* Shift register */
pin [38,39,40] = [S_RST,S_LD,S_IN];
pinnode [53..59] = [S0..S6];
pinnode 60 = S_OUT;

field INPUTS = [I7..I0];    /* Input data */
field T_CNT = [Q7..Q0];     /* T counter */
field GCODE = [G3..G0];     /* Grey code counter */
field SHIFT = [S_OUT,S6..S0]; /* Shift register */
field SHIFT1 = [S6..S0,S_IN];

/* T Counter */
Q0.t = !LD
     # (Q0 $ I0) & LD;
Q1.t = !LD & Q0
     # LD & (Q1 $ I1);
Q2.t = !LD & Q1 & Q0
     # LD & (Q2 $ I2);
Q3.t = !LD & Q2 & Q1 & Q0
     # LD & (Q3 $ I3);
Q4.t = !LD & Q3 & Q2 & Q1 & Q0
     # LD & (Q4 $ I4);
Q5.t = !LD & Q4 & Q3 & Q2 & Q1 & Q0
     # LD & (Q5 $ I5);
Q6.t = !LD & Q5 & Q4 & Q3 & Q2 & Q1 & Q0
     # LD & (Q6 $ I6);
Q7.t = !LD & Q6 & Q5 & Q4 & Q3 & Q2 & Q1 & Q0
     # LD & (Q7 $ I7);
T_CNT.ce = 'h'FF;           /* synchronous clock mode */
T_CNT.ar = RST;

/* Shift register */
SHIFT.d = SHIFT1 & !S_LD    /* shift */
        # INPUTS & S_LD;    /* load */
SHIFT.ck = ACLK;            /* product term clock mode */
SHIFT.ar = S_RST;
```

```
/* Greycode counter */
GCODE.ce = !HOLD;          /* gated synchronous clock mode */
GCODE.ar = RST;
GCODE.oe = OE;

/* State machine will use register feedback path */
SEQUENCE GCODE {
present 'b'0000  next 'b'0001;
present 'b'0001  next 'b'0011;
present 'b'0011  next 'b'0010;
present 'b'0010  next 'b'0110;
present 'b'0110  next 'b'0111;
present 'b'0111  next 'b'0101;
present 'b'0101  next 'b'0100;
present 'b'0100  next 'b'1100;
present 'b'1100  next 'b'1101;
present 'b'1101  next 'b'1111;
present 'b'1111  next 'b'1110;
present 'b'1110  next 'b'1010;
present 'b'1010  next 'b'1011;
present 'b'1011  next 'b'1001;
present 'b'1001  next 'b'1000;
present 'b'1000  next 'b'0000;}

/* Seven segment display decoder */
TABLE GCODE = [1seg,2seg,3seg,4seg,5seg,6seg,7seg] {
0 => 'b'1011111;
1 => 'b'0001100;
2 => 'b'1111001;
3 => 'b'1111100;
4 => 'b'0101110;
5 => 'b'1110110;
6 => 'b'1110111;
7 => 'b'1001100;
8 => 'b'1111111;
9 => 'b'1101110;
A => 'b'1101111;
B => 'b'0110111;
C => 'b'1010011;
D => 'b'0111101;
E => 'b'1110011;
F => 'b'1100011; }
```

```
CUPL Simulation Input File (Use 2500B.SI)
Name            USE2500B;
Partno          N/A;
Date            3/27/95;
Rev.            -;
Designer        Wendey Mueller;
Company         Atmel;
Assembly        -;
Location        -;
Device          V2500BLCC;

FIELD SEVSEG=[1seg,2seg,3seg,4seg,5seg,6seg,7seg];
FIELD TST_SHIFT=[S0,S1,S2,S3,S4,S5,S6,S_OUT];

ORDER: SCLK,%1,RST,%1,LD,%1,HOLD,%1,OE,%1,INPUTS,%1,
       ACLK,%1,S_LD,%1,S_RST,%1,S_IN,%2,
       T_CNT,%2,GCODE,%2,SEVSEG,%2,TST_SHIFT;
```

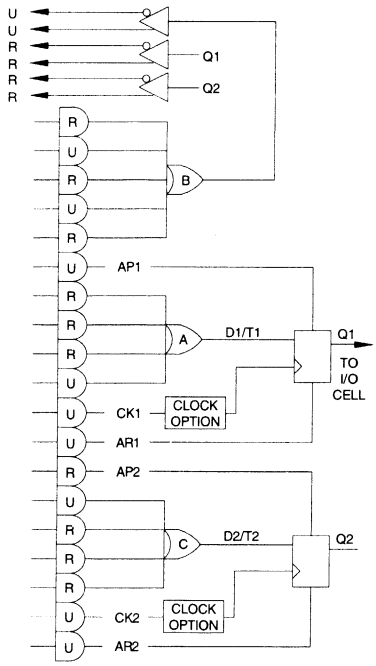
```
BASE: hex;

VECTORS:
/* Test T-counter */
0 1 0 1 1 '00' 0 0 0 0  "00"  "*"  "*"      "*"
$REPEAT 255;
C 0 0 1 1 '00' 0 0 0 0  "*"   "*"  "*"      "*"
C 0 1 1 1 'AB' 0 0 0 0  "AB"  "*"  "*"      "*"
C 0 0 1 1 '00' 0 0 0 0  "AC"  "*"  "*"      "*"
/* Test greycode counter and seven segment decoder */
0 1 0 0 1 '00' 0 0 0 0  "*"   "0"  HLHHHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "1"  LLLHHLL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "3"  HHHHHLL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "2"  HHHHLLH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "6"  HHHLHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "7"  HLLHHLL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "5"  HHHLHHL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "4"  LHLHHHL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "C"  HLHLLHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "D"  LHHHHLH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "F"  HHLLLHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "E"  HHHLLHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "A"  HHLHHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "B"  LHHLHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "9"  HHLHHHL  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "8"  HHHHHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "0"  HLHHHHH  "*"
C 0 0 0 1 '00' 0 0 0 0  "*"   "1"  LLLHHLL  "*"
C 0 0 1 1 '00' 0 0 0 0  "*"   "1"  LLLHHLL  "*"
C 0 0 0 0 '00' 0 0 0 0  "*"   "Z"  HHHHHLL  "*"
/* Test shift register */
0 0 0 0 1 '00' 0 0 1 0  "*"   "*"  "*"      LLLLLLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HLLLLLLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LHLLLLLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLHLLLLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLHLLLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLLHLLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLLLHLL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLLLLHL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLLLLLH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HLLLLLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHLLLLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHLLLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHLLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHLLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHHLL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHHHL
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHHHH
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LHHHHHHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HLHHHHHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHLHHHHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHLHHHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHLHHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHLHH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHHLH
0 0 0 0 1 '00' C 0 0 1  "*"   "*"  "*"      HHHHHHHL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LHHHHHHH
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLHHHHHH
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LLLHHHHH
0 0 0 0 1 '55' C 1 0 0  "*"   "*"  "*"      HLHLHLHL
0 0 0 0 1 '00' C 0 0 0  "*"   "*"  "*"      LHLHLHLH
```

Using the ATV5000

The ATV5000 logic cells retain the ATV2500's basic features with two registers, three sum terms and Q1, Q2, and pin feedback options. In addition, these following features make the ATV5000 even more versatile:

1. Input latches are added to every I/O pin. Each latch can be enabled or disabled independently.
2. The ATV5000 can be configured to feedback a combinatorial sum term and send Q1 to the output. Feeding the combinatorial sum term internally makes implementing logic equations with large number of product terms possible without sacrificing an I/O pin.
3. Dedicated clock pins and individual clock product terms create multiple clock options for each flip-flop.
4. The addition of the buried logic cells handles more logic than ever.
5. Each flip-flop can be configured as D- or T-type flip-flop.
6. Asynchronous preset, asynchronous reset and programmable output polarity allow registered outputs using fewer product terms.

Logic Cell with Buried Sum Term and Register to I/O Cell



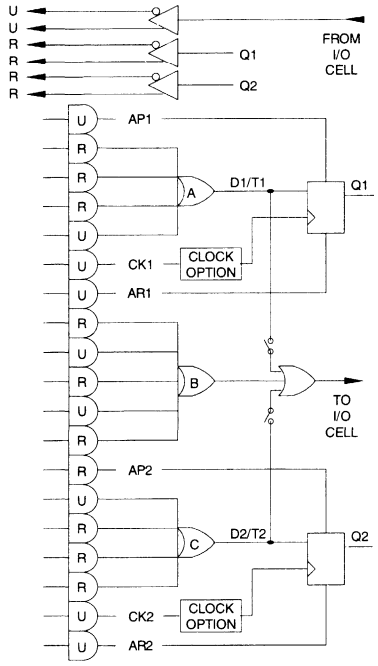
High Density UV Erasable Programmable Logic Device

Application Brief

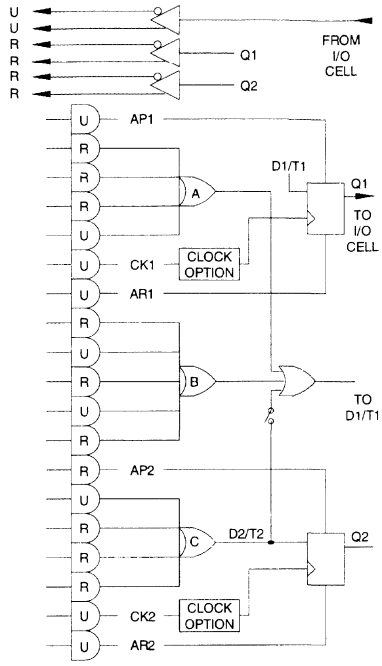
6

0480A

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell



Logic Cell with Combinable Sum Terms, Register to I/O Cell



The following are sections of ABEL™ and CUPL™ source files to illustrate how each of these features is described in the ABEL™ and CUPL™ high level description languages.

Pin and Node Assignments

All the buried registers used in the design need to be assigned node numbers. The following tables show the complete set of node numbers by quadrant.

ABEL™ and Atmel-ABEL™

```
LENA,CLOCK pin 1,2;
ACK pin 4 istype
'reg_d,buffer';
OUTA pin 5;
DRAM node 121 istype
'reg_t';
EXPAND node 70;
ACKL node 813;
```

CUPL™

```
pin 1,2 = LENA,CLOCK;
pin 4 = ACK;

pin 5 = OUTA;
pinnode 105 = DRAM;

pinnode 208 = EXPAND;
```

ATV5000 ABEL™ and Atmel-ABEL™ Node Numbers

Quadrant I					Quadrant II				
		Sum Term					Sum Term		
Pin	Input Latch	A	B	C	Pin	Input Latch	A	B	C
4	813	761	69	121	18	826	774	82	134
5	814	762	70	122	19	827	775	83	135
6	815	763	71	123	21	828	776	84	136
7	816	764	72	124	22	829	777	85	137
8	817	765	73	125	23	830	778	86	138
9	818	766	74	126	24	831	779	87	139
10	819	767	75	127	25	832	780	88	140
11	820	768	76	128	26	833	781	89	141
12	821	769	77	129	27	834	782	90	142
13	822	770	78	130	28	835	783	91	143
14	823	771	79	131	29	836	784	92	144
15	824	772	80	132	30	837	785	93	145
17	825	773	81	133	31	838	786	94	146
6 Buried Logic Cells B23 - B18 node 173 - 178 LCK1 pin 1;Quadrant Latch clock RCK1 pin 2; Quadrant Synchronous Register Clock					6 Buried Logic Cells B17 - B12 node 179 - 184 LCK2 pin 34; Quadrant Latch Clock RCK2 pin 32; Quadrant Synchronous Register Clock				

Quadrant III					Quadrant IV				
		Sum Term					Sum Term		
Pin	Input Latch	A	B	C	Pin	Input Latch	A	B	C
38	839	787	95	147	52	852	800	108	160
39	840	788	96	148	53	853	801	109	161
40	841	789	97	149	55	854	802	110	162
41	842	790	98	150	56	855	803	111	163
42	843	791	99	151	57	856	804	112	164
43	844	792	100	152	58	857	805	113	165
44	845	793	101	153	59	858	806	114	166
45	846	794	102	154	60	859	807	115	167
46	847	795	103	155	61	860	808	116	168
47	848	796	104	156	62	861	809	117	169
48	849	797	105	157	63	862	810	118	170
49	850	798	106	158	64	863	811	119	171
51	851	799	107	159	65	864	812	120	172
6 Buried Logic Cells B11 - B6 node 185 - 190 LCK3 pin 35; Quadrant Latch Clock RCK3 pin 36; Quadrant Synchronous Register Clock					6 Buried Logic Cells B5 - B0 node 191 - 196 LCK4 pin 68; Quadrant Latch Clock RCK4 pin 66; Quadrant Synchronous Register Clock				

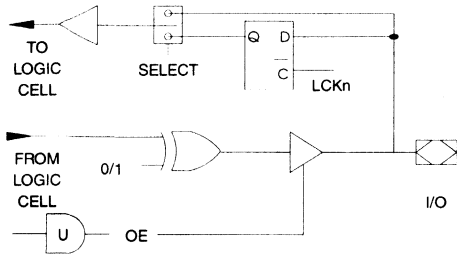
ATV5000 CUPL™ Node Numbers

Quadrant I				Quadrant II			
	Sum Term				Sum Term		
Pin	A	B	C	Pin	A	B	C
4	157	209	105	18	158	210	106
5	156	208	104	19	159	211	107
6	155	207	103	21	160	212	108
7	154	206	102	22	161	213	109
8	153	205	101	23	162	214	110
9	152	204	100	24	163	215	111
10	151	203	99	25	164	216	112
11	150	202	98	26	165	217	113
12	149	201	97	27	166	218	114
13	148	200	96	28	167	219	115
14	147	199	95	29	168	220	116
15	146	198	94	30	169	221	117
17	145	197	93	31	170	222	118
6 Buried Logic Cells B23 - B18 node 74 - 69 LCK1 pin 1; Quadrant Latch Clock RCK1 pin 2; Quadrant Synchronous Register Clock				6 Buried Logic Cells B17 - B12 node 75 - 80 LCK2 pin 34; Quadrant Latch Clock RCK2 pin 32; Quadrant Synchronous Register Clock			

Quadrant III				Quadrant IV			
	Sum Term				Sum Term		
Pin	A	B	C	Pin	A	B	C
38	183	235	131	52	184	236	132
39	182	234	130	53	185	237	133
40	181	233	129	55	186	238	134
41	180	232	128	56	187	239	135
42	179	231	127	57	188	240	136
43	178	230	126	58	189	241	137
44	177	229	125	59	190	242	138
45	176	228	124	60	191	243	139
46	175	227	123	61	192	244	140
47	174	226	122	62	193	245	141
48	173	225	121	63	194	246	142
49	172	224	120	64	195	247	143
51	171	223	119	65	196	248	144
6 Buried Logic Cells B11 - B6 node 86 - 81 LCK3 pin 35; Quadrant Latch Clock RCK3 pin 36; Quadrant Synchronous Register Clock				6 Buried Logic Cells B5 - B0 node 87 - 92 LCK4 pin 68; Quadrant Latch Clock RCK4 pin 66; Quadrant Synchronous Register Clock			

Input Latch

Each of the 52 I/Os has an input latch that can be enabled and disabled individually. When the latch is enabled and latch clock is high, the pin value is latched. When the quadrant latch clock is low, the latch becomes transparent. When the latch is disabled, an ATV5000 I/O acts like those of the ATV750 and ATV2500 I/Os. The pin input is fed directly to the array (except when sum term B is being used as a buried feedback).



The .D and the .LE (latch enable) equations are required to enable the input latch in ABEL™ AHDL. The only allowed input to the latch is the IO pin with which it is associated. The only allowed .LE input is the quadrant latch clock (pin 1,34, 35, or 68). Notice that CUPL™ does not have node numbers for the input latches. Any pin name used in a feedback with the dot extension IOL tells CUPL™ that particular pin should be a latched pin.

ABEL™ and Atmel-ABEL™

```
ACKL.D  = ACK;
ACKL.LE = LENA;
OUTA  := ACKL;
```

CUPL™

```
OUTA.D = ACK.IOL;
```

Internal Combinatorial Feedback for an I/O Cell

To implement the combinatorial feedback of the B sum term, first define the node name with the corresponding node number. This node will take a five-product term equation. Regular syntax describing a combinatorial equation will describe the B sum term.

Note: This B sum term node number is defined only when this feature is needed. When this feature is used, the output is from Q1 through an inverter/buffer. *The I/O pin becomes a output-only pin. It cannot be used as an input or as an input/output.*

ABEL™ and Atmel-ABEL™

```
OUTA pin 5;
EXPAND node 70;
OUTA.D = INA&INB# !INC&!IND;
EXPAND = INA & !INC # IND;
```

CUPL™

```
pin 5 = OUTA;
pinnode 208 = EXPAND;
OUTA.D = INA&INB#!INC&!IND;
EXPAND = INA & !INC #
IND;
```

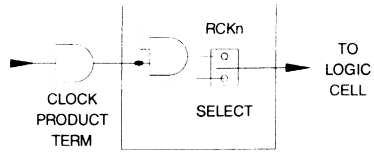
(OUTA and EXPAND are in the same I/O logic cell. OUTA is the Q1 output to pin after the inverter/buffer and EXPAND is the combinatorial sum term feedback. The feedbacks from this logic cell are Q1 before the inverter/buffer, Q2, and the B sum term)

Clocking Options

There are different methods of clocking the registers in the ATV5000. The clock options can best described as either the AND function of (quadrant clock & clock product term) or purely the function of the clock product term (like ATV750 and ATV2500).

Synchronous Operation

The quadrant clock is the only clocking element in this mode of operation. The clock product term must be defined to be equal to 1. In ABEL AHDL, .CK defines the clock product term and .CE is the corresponding quadrant clock.



In CUPL™, .CE has a different implication. The keyword .CE means the user wants the AND function (quadrant clock & clock product term) for the clock.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = 1;
OUTA.CE = CLOCK; "CLOCK is pin 2
```

CUPL™

```
OUTA.CE = 'B'1;
```

Gated Synchronous Operation

This clock option still uses the fast quadrant register clock pin, but now it has a gating element. The clock product term enables or disables the clock going to the register.

ABEL™ and Atmel-ABEL™

```
OUTA.CK = INX & INY & !INZ;
OUTA.CE = CLOCK; "CLOCK
is pin 2
```

CUPL™

```
OUTA.CE =
INX&INY&!INZ;
```

Asynchronous Operation

The quadrant clock has no effect on the register in this mode of clock option. The register is clocked by the clock product term like the ATV750 and ATV2500 registers.

ABEL™ and Atmel-ABEL™

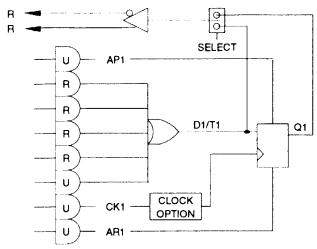
```
OUTA.CK = INA & !INB
& INC;
```

CUPL™

```
OUTA.CK = INA & !INB & INC;
```

Buried Logic Cells

There are six buried logic cells in each quadrant. Every buried logic cell can be configured as a buried register or as a combinatorial feedback to the quadrant array. In the buried register mode, it's used the same way as Q1 and Q2. In the combinatorial feedback mode, it's used the same way as the B sum term feedback.



ABEL™ and Atmel-ABEL™

```
ADDR,XDATA node 173,174;

ADDR = A16&A15&!A14#RST;
XDATA.T = !A16 & RST;
XDATA.CK = INA & INC;
XDATA.AR = INB;
```

CUPL™

```
pinnode 74,73 =
ADDR,XDATA;
ADDR = A16&A15&!A14#RST;
XDATA.T = !A16 & RST;
XDATA.CK = INA & INC;
XDATA.AR = INB;
```

D-Type and T-Type Registers

All the registers in the ATV5000 can be configured as D- or T-type. The ISTYPE statement after the PIN or NODE definition in ABEL™ AHDL tells ABEL™ which type of register is needed.

ABEL™ and Atmel-ABEL™

```
ABC   node  123 istype 'reg_t';
XYZ   pin 7 istype
'reg_d';
ABC.T = INA & INB # INC;
XYZ.D = !INA # INC;
```

CUPL™

```
pinnode 103 = ABC;
pin 7 = XYZ;

ABC.T = INA & INB # INC;
XYZ.D = !INA # INC;
```

In both languages, the .T extension is reserved for T flip-flop and .D extension for D flip-flop.

Asynchronous Preset

One of the advantanges of having a programmable output polarity I/O is that the same combinatorial output often take fewer product terms to implement using negative logic rather than positive logic or vice versa.

The same can be done for a registered output provided the power-up state is not crucial (all flip-flops are reset upon power up). With an asynchronous preset and an asynchronous reset, simply swap the two product terms and invert your equation and polaritywill let you take advantage of expressing the same logic in a different polarity. The following example shows a four-to-one reduction in product term requirement.

ABEL™ and Atmel-ABEL™

```
OUTC pin 8 istype
'invert,reg_d';
OUTD pin 9 istype
'buffer,reg_d';
OUTC.D  = INA# !INB#INC# !IND;
OUTC.CK = CLK;
OUTC.AR = !INA & RST;
OUTC.AP = INB & PRESET;
OUTD.D  = !INA&INB&!INC&IND;
OUTD.CK = CLK;
OUTD.AR = INB & PRESET;
OUTD.AP = !INA & RST;
```

CUPL™

```
pin 8 = OUTC;

pin 9 = !OUTD;

OUTC.D  = INA#!INB#INC#!IND;
OUTC.CK = CLK;
OUTC.AR = !INA & RST;
OUTC.AP = INB & PRESET;
OUTD.D  = !INA&INB&!INC&IND;
OUTD.CK = CLK;
OUTD.AR = INB & PRESET;
OUTD.AP = !INA & RST;
```

Example ABEL™ Description File

```
module V5000;
title   'Demo ATV5000 features with Atmel-abel (IBM386 or compatible)
        Atmel Corporation PLD      Joe Yu            April 28, 1991'
V5K device 'P5000';
"   The IOs, registers, latches, inputs, and combinatorial sum terms
"   feedbacks are named with the following prefixes for clarity:
"   Prefix
"   I    -    Quadrant Clocks, Latch Enables.
"   IO   -    IO pins
"   IL   -    Input Latches
"   BLC  -    Buried Logic Cells
"   STF  -    Sum Term Feedbacks
"   Valid ABEL AHDL identifiers can be used in place of them.
declarations
I1 pin 1;           " Quadrant 1   Latch Enable/Input
I2 pin 2;           " Quadrant 1   Synchronous Register Clock/Input
I32 pin 32;         " Quadrant 2   Synchronous Register Clock/Input
I34 pin 34;         " Quadrant 2   Latch Enable/Input
I35 pin 35;         " Quadrant 3   Latch Enable/Input
I36 pin 36;         " Quadrant 3   Synchronous Register Clock/Input
I66 pin 66;         " Quadrant 4   Synchronous Register Clock/Input
I68 pin 68;         " Quadrant 4   Latch Enable/Input
"    **** Quadrant I ****
" I/O LOGIC CELL
" ================
IO4,IO5,IO6,IO7,IO8,IO9                          pin 4,5,6,7,8,9 istype 'buffer,reg_d';
STF4,STF5,STF6,STF7,STF8,STF9                    node 69,70,71,72,73,74;
IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1              node 761,762,763,764,765,766;
IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2              node 121,122,123,124,125,126;
IO10,IO11,IO12,IO13,IO14,IO15,IO17               pin 10,11,12,13,14,15,17 istype
                                                 'buffer,reg_d'
STF10,STF11,STF12,STF13,STF14,STF15,STF17        node 75,76,77,78,79,80,81;
IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1 node 767,768,769,770,771,772,773;
IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2 node 127,128,129,130,131,132,133;
" INPUT LATCHES
" ================
IL4,IL5,IL6,IL7,IL8,IL9                          node 813,814,815,816,817,818;
IL10,IL11,IL12,IL13,IL14,IL15,IL17               node 819,820,821,822,823,824,825;
" BURIED LOGIC CELL
" ==================
BLC18,BLC19,BLC20,BLC21,BLC22,BLC23              node 178,177,176,175,174,173 ;
declarations "      **** Quadrant II ****
" I/O LOGIC CELL
" ================
IO18,IO19,IO21,IO22,IO23,IO24                    pin 18,19,21,22,23,24 istype
                                                 'buffer,reg_d';
STF18,STF19,STF21,STF22,STF23,STF24              node 82,83,84,85,86,87;
IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1        node 774,775,776,777,778,779;
IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2        node 134,135,136,137,138,139;
IO25,IO26,IO27,IO28,IO29,IO30,IO31               pin 25,26,27,28,29,30,31 ISTYPE 'BUFFER';
STF25,STF26,STF27,STF28,STF29,STF30,STF31        node 88,89,90,91,92,93,94;
IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1 node 780,781,782,783,784,785,786 ;
IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2 node 140,141,142,143,144,145,146 ;
" INPUT LATCHES
" ================
IL18,IL19,IL21,IL22,IL23,IL24                    node 826,827,828,829,830,831;
IL25,IL26,IL27,IL28,IL29,IL30,IL31               node 832,833,834,835,836,837,838;
```

```
" BURIED LOGIC CELL
" ==================
BLC12,BLC13,BLC14,BLC15,BLC16,BLC17                    node 184,183,182,181,180,179;
declarations "        **** Quadrant III ****
" I/O LOGIC CELL
" ===============•
IO38,IO39,IO40,IO41,IO42,IO43                          pin 38,39,40,41,42,43;
STF38,STF39,STF40,STF41,STF42,STF43                    node 95,96,97,98,99,100;
IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1              node 787,788,789,790,791,792;
IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2              node 147,148,149,150,151,152
                                                       istype'reg_t';
IO44,IO45,IO46,IO47,IO48,IO49,IO51                     pin 44,45,46,47,48,49,51;
STF44,STF45,STF46,STF47,STF48,STF49,STF51              node 101,102,103,104,105,106,107;
IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1       node 793,794,795,796,797,798,799;
IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2       node 153,154,155,156,157,158,159;
" INPUT LATCHES
" ================
IL38,IL39,IL40,IL41,IL42,IL43                          node 839,840,841,842,843,844;
IL44,IL45,IL46,IL47,IL48,IL49,IL51                     node 845,846,847,848,849,850,851;
" BURIED LOGIC CELL
" ==================
BLC6,BLC7,BLC8,BLC9,BLC10,BLC11    node 190,189,188,187,186,185
                                                       ISTYPE 'REG_D';
declarations "        **** Quadrant IV ****
" I/O LOGIC CELL
" ===============
IO52,IO53,IO55,IO56,IO57,IO58                          pin 52,53,55,56,57,58 istype 'buffer';
STF52,STF53,STF55,STF56,STF57,STF58                    node 108,109,110,111,112,113;
IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1              node 800,801,802,803,804,805;
IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2              node 160,161,162,163,164,165;
IO59,IO60,IO61,IO62,IO63,IO64,IO65                     pin 59,60,61,62,63,64,65 istype 'buffer';
STF59,STF60,STF61,STF62,STF63,STF64,STF65              node 114,115,116,117,118,119,120;
IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1       node 806,807,808,809,810,811,812;
IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2       node 166,167,168,169,170,171,172;
" INPUT LATCHES
" ================
IL52,IL53,IL55,IL56,IL57,IL58                          node 852,853,854,855,856,857;
IL59,IL60,IL61,IL62,IL63,IL64,IL65                     node 858,859,860,861,862,863,864;
" BURIED LOGIC CELL
" ==================
BLC0,BLC1,BLC2,BLC3,BLC4,BLC5                          node 196,195,194,193,192,191;
   H,L,C,D,K,U,X,Z = 1,0,.C.,.D.,.K.,.U.,.X.,.Z.;
"    MACRO (INPUT LATCH)
INPUT_LATCH MACRO (IL,IO,QUAD_LE)
{?IL.D   =    ?IO;
?IL.LE   =    ?QUAD_LE;}
equations
"                    INPUT LATCH
"   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high,
"   the pin value is latched.
"   When the quadrant latch clock is low, the latch becomes transparent.
IL4.D    =    IO4;    "The .D and the .LE (latch enable) extentions are required to describe a
IL4.LE   =    I1;     "latch in ABEL AHDL. The only allowed input to he latch is the IO pin it
                      "associates with. The only allowed .LE input is the quadrant latch enable.
                      "They are Pin 1, 34, 35, and 68.
"       INPUT_LATCH macro is another way to describe the latch.
INPUT_LATCH (IL5,IO5,I1);  "Latch Pin 5
INPUT_LATCH (IL6,IO6,I1);  "Latch Pin 6
IO4.d    =   !IO4.fb;        " When .oe is enabled by IO8, IO4 outputs a 1 bit counter.
IO4.oe   =   IO8;     " When .oe is disabled by !IO8, IO4 latches a data bit  from the bus.
```

```
IO4.ck   =   1;
IO4.ce   =   I2;
IO7      =   IL4;
test_vectors ( "Test the latches...
[I1,I2,IO8,IO4]-[IO4,IO7])
[ 0, 0, 1, X  ]    ->     [  0, 0 . ]; "Transparent
[ 0, C, 1, X  ]    ->     [  1, 1 . ]; "Transparent
[ U, 0, 0, 0  ]    ->     [  Z, 0 . ]; "Disable .oe and latch 0
[ 1, C, 1, X  ]    ->     [  0, 0 . ]; "Latched 0
[ 1, C, 1, X  ]    ->     [  1, 0 . ]; "Latched 0
[ D, C, 1, X  ]    ->     [  0, 0 . ]; "Transparent
[ 0, C, 1, X  ]    ->     [  1, 1 . ]; "Transparent
[ 0, C, 1, X  ]    ->     [  0, 0 . ]; "Transparent
[ U, 0, 0, 1  ]    ->     [  Z, 1 . ]; "Disable .oe and latch 1
[ 1, 0, 1, X  ]    ->     [  0, 1 . ]; "Latched 1
[ 1, C, 1, X  ]    ->     [  1, 1 . ]; "Latched 1
[ 1, C, 1, X  ]    ->     [  0, 1 . ]; "Latched 1
equations
"    CLOCKING OPTIONS
"   There are different methods of clocking the registers in the ATV5000. The clock is
"   best described as either the AND function of (Quadrant Clock & Clock Product term)
"   or the product term by it self. In the following examples the register can be a
"   name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either .t or
"   .d flip-flop.
IO22.d   =    !IO22.fb;
IO22.ck  =    IO18 & !IO19;          "Note there is no .ce equation defined. This is an
IO22.ar  =    IO21;                  "asynchronous clocking method where the quadrant clock
                                     "has no effect.
test_vectors (
[IO18,IO19,IO21      ]      -> [ IO22 ])
[        0, 0, 1     ]      -> [   0 . ];
[        0, 0, 0     ]      -> [   0 . ];
[        C, 0, 0     ]      -> [   1 . ];
[        C, 0, 0     ]      -> [   0 . ];
equations
IO23.d   =    !IO23.fb;
IO23.ck  =    IO18 & !IO19;          "The clock product term (.ck) is used to gate the quadrant
IO23.ce  =    I32;                   "clock pin. Using quadrant clock pin in a synchronous mode
IO23.ar  =    IO21;                  "allows higher clock rate. Pin 32 is the Quadrant 2 clock pin.
test_vectors (
[I32,IO18,IO19,IO21 ]      ->     [ IO23])
[        0, 1, 0,   1       ]   -> [ . 0];
[        C, 0, 0,   0       ]   -> [ . 0]; "Product term blocks quadrant clock
[        C, 1, 0,   0       ]   -> [ . 1]; "Product term enables quadrant clock
[        C, 1, 0,   0       ]   -> [ . 0];
equations
IO24.d   =    !IO24.fb;
IO24.ck  =    1;     "Note that the .ck is defined to 1. The quadrant clock is the only
IO24.ce = I32;       "clocking element. The .ce is Pin 32 because it's the proper quadrant
IO24.ar  =    IO21;  "clock to use for synchronous operation.
test_vectors (
[ I32, IO21 ]  ->   [ IO24 ])
[        0, 1  ]    ->     [  0  ];
[        C, 0  ]    ->     [  1  ];
[        C, 0  ]    ->     [  0  ];
[        C, 0  ]    ->     [  1  ];
"   D-TYPE and T-TYPE REGISTERS
"   All the registers in the ATV5000 can be configured as D or T type. The ISTYPE
"   statement after the PIN or NODE definition tells ABEL which type of register is
"   needed.
```

```
"   ABC  node 122 istype 'reg_t';
"   XYZ  pin  5 istype 'reg_d';
"   Use the .t extension for ABC and .d extension for XYZ when you write the equations.
equations
" 3 Bit Synchronous Counter using T flip-flops
IO38Q2.t = 1;                    IO38Q2.ck = 1;      IO38Q2.ce = I36;    IO38Q2.ar = IO38;
IO39Q2.t = IO38Q2;               IO39Q2.ck = 1;      IO39Q2.ce = I36;    IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;      IO40Q2.ck = 1;      IO40Q2.ce = I36;    IO40Q2.ar = IO38;
test_vectors (
[ I36, IO38 ]              -> [ IO40Q2,IO39Q2,IO38Q2])
[       0, 1       ]       -> [ 0, 0, 0];
[       C, 0       ]       -> [ 0, 0, 1];
[       C, 0       ]       -> [ 0, 1, 0];
[       C, 0       ]       -> [ 0, 1, 1];
[       C, 0       ]       -> [ 1, 0, 0];
[       C, 0       ]       -> [ 1, 0, 1];
[       C, 0       ]       -> [ 1, 1, 0];
[       C, 0       ]       -> [ 1, 1, 1];
[       C, 0       ]       -> [ 0, 0, 0];
equations
" 3 Bit Synchronous Counter using D flip-flops
BLC6.d = !BLC6;                  BLC6.ck = 1;        BLC6.ce = I36;      BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;            BLC7.ck = 1;        BLC7.ce = I36;      BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ck = 1;          BLC8.ce = I36;      BLC8.ar = IO38;
test_vectors (
[ I36, IO38 ]        ->     [BLC8,BLC7,BLC6])
[       0, 1   ]     ->     [   0,  0,  0];
[       C, 0   ]     ->     [   0,  0,  1];
[       C, 0   ]     ->     [   0,  1,  0];
[       C, 0   ]     ->     [   0,  1,  1];
[       C, 0   ]     ->     [   1,  0,  0];
[       C, 0   ]     ->     [   1,  0,  1];
[       C, 0   ]     ->     [   1,  1,  0];
[       C, 0   ]     ->     [   1,  1,  1];
[       C, 0   ]     ->     [   0,  0,  0];
"       UNIVERSAL AND REGIONAL PRODUCT TERMS
"   A Regional product term has inputs from all the feedbacks of its quadrant Buried
"   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal
"   product term has the Pin/B Sum Term Feedbacks.
"       OUTPUTS and FEEDBACKS
"   Combinatorial:
"   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9,
"   or 13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
"   terms to use.
"       IO52               =  up to 5 PRODUCT TERMS (2 UNIVERSAL)
"       IO52.oe            =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.(d or t)    =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
"       IO52Q1.ck          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.ce          =  QUADRANT CLOCK
"       IO52Q1.ar          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q1.ap          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.(d or t)    =  up to 4 PRODUCT TERMS (1 UNIVERSAL)
"       IO52Q2.ck          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce          =  QUADRANT CLOCK
"       IO52Q2.ar          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ap          =  1 PRODUCT TERM (0 UNIVERSAL)
"   ALLOWED FEEDBACKS:            SOURCE:
"   IO52                          --              Pin feedback, after the buffer/inverter.
"   IO52Q1,IO52Q1.FB              --              Q1 register feedback.
"   IO52Q2,IO52Q2.FB              --              Q2 register feedback.
```

```
"   Combinatorial:
"   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
"   terms to use. Q1 will  feedback the A Sum Term portion of the output logic.
"        IO52              =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"        IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"        IO52Q2.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ce         =   QUADRANT CLOCK
"        IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)
"   ALLOWED FEEDBACKS:             SOURCE:
"   IO52,IO52.PIN                  --              Pin feedback, after the buffer/inverter.
"   IO52Q2,IO52Q2.FB,IO52Q2.Q      --              Q2 register feedback.
"   Combinatorial:
"   If the reduced equation requires more than 9 product terms, it leaves no product
"   terms for Q1 and Q2. Q1 feeds back A Sum Term and Q2 feeds back C Sum Term
"        IO52              =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"        IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"   ALLOWED FEEDBACKS:             SOURCE:
"   IO52                           --              Pin feedback, after the buffer/inverter.
"   Registered:
"   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9,
"   or 13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 4 or less product terms, you may define a 5 product term
"   equation for the STF (Sum Term Feedback) and define a 4 product term equation for
"   Q2.
"        IO52.(d or t)     =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"        IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ck           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ce           =   QUADRANT CLOCK
"        IO52.ar           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ap           =   1 PRODUCT TERM (1 UNIVERSAL)
"        STF52             =   up to 5 PRODUCT TERMS (2 UNIVERSAL)
"        IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"        IO52Q2.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ce         =   QUADRANT CLOCK
"        IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)

"        ALLOWED FEEDBACKS:          SOURCE:
"        IO52.FB                --   Register feedback prior to buffer/inverter.
"        IO52Q2,IO52Q2.FB       --   Q2 register feedback.
"        STF52                  --   Sum Term Feedback for logic expansion.
"   Registered:
"   If the reduced equation requires 9 to 5 product terms, you may write a 4 product
"   term equation for Q2.
"        IO52.(d or t)     =   up to 9 PRODUCT TERMS (3 UNIVERSAL)
"        IO52.oe           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ck           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ce           =   QUADRANT CLOCK
"        IO52.ar           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52.ap           =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (1 UNIVERSAL)
"        IO52Q2.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ce         =   QUADRANT CLOCK
"        IO52Q2.ar         =   1 PRODUCT TERM (1 UNIVERSAL)
"        IO52Q2.ap         =   1 PRODUCT TERM (0 UNIVERSAL)
"        ALLOWED FEEDBACKS:          SOURCE:
"        IO52                   --   Pin feedback, after the buffer/inverter.
```

```
"       IO52.FB                 --  Register feedback prior to buffer/inverter.
"       IO52Q2,IO52Q2.FB,       --  Q2 register feedback.
"   Registered:
"   If the reduced equation requires more than 9 product terms, it leaves zero
"   product terms for Q1 and Q2.
"       IO52.(d or t)       =   up to 13 PRODUCT TERMS (4 UNIVERSAL)
"       IO52.oe             =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ck             =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ce             =   QUADRANT CLOCK
"       IO52.ar             =   1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ap             =   1 PRODUCT TERM (1 UNIVERSAL)
"       ALLOWED FEEDBACKS:          SOURCE:
"       IO52,                   --  Pin feedback, after the buffer/inverter.
"       IO52.FB                 --  Register feedback prior to buffer/inverter.
"       AP, AR, and CK
"   Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
"   Reset) and .CK. All ARs and CKs are Universal product terms. The APs are Universal
"   product terms except the APs for Q2.
"   NOTE:     AP and AR should never be active at the same time.
equations
IO10.d      =     !IO10.fb;
IO10.ck  =    IO8;
IO10.ar  =    IO11;
IO10.ap  =    IO12;
test_vectors (
[ IO8, IO11, IO12   ]     -> [ IO10])
[       0, 1, 0     ]     -> [   0  ]; "AR
[       0, 0,  0    ]     -> [   0  ];
[       C, 0,  0    ]     -> [   1  ];
[       C, 0,  0    ]     -> [   0  ];
[       0, 0,  1    ]     -> [  1   ]; "AP
[       0, 1,  0    ]     -> [   0  ]; "AR
"        BURIED LOGIC CELLS
"   Buried Logic Cell can be configured as a register feedback like Q2. It can also be
"   configured as combinatorial feedback to accommodate for logic expansion.
equations
BLC17.t     =     1;            "Registered
BLC17.ck    =     IO9;
BLC17.ar    =     IO21;
BLC14       =     I1;           "Combinatiorial
IO25        =     BLC17;
IO26        =     BLC14;
test_vectors (
[IO9, IO21, I1 ]    ->    [ BLC17,BLC14,IO25,IO26])
[       0, 1, 0     ]     -> [ 0, 0, 0, 0 ];
[       C, 0, 0     ]     -> [ 1, 0, 1, 0 ];
[       0, 0, 1     ]     -> [ 1, 1, 1, 1 ];
[       C, 0, 1     ]     -> [ 0, 1, 0, 1 ];
[       C, 0, 0     ]     -> [ 1, 0, 1, 0 ];
END;
```

Example CUPL™ Description File

```
Name          V5K;
Partno        NA;
Date          7/22/91;
Revision      01;
Designer      Joe Yu;
Company       Atmel Corporation;
Assembly      NA;
Location      U1;
Device        V5000;
Format        j;
/* Compiled with CUPL 386 version */
/* The IOs, registers, inputs, and combinatorial sum terms feedbacks are named with
 * the following prefixes for clarity:
 * Prefix
 * I          -      Quadrant Clocks, Latch Enables.
 * IO         -      IO pins
 * BLC        -      Buried Logic Cells
 * STF        -      Sum Term Feedbacks
 * Valid CUPL HDL identifiers can be used in place of them. */
pin 1    =           I1;           /* Quadrant 1     Latch Enable/Input               */
pin 2    =           I2;           /* Quadrant 1     Synchronous Register Clock/Input */
pin 32   =           I32;          /* Quadrant 2     Synchronous Register Clock/Input */
pin 34   =           I34;          /* Quadrant 2     Latch Enable/Input               */
pin 35   =           I35;          /* Quadrant 3     Latch Enable/Input               */
pin 36   =           I36;          /* Quadrant 3     Synchronous Register Clock/Input */
pin 66   =           I66;          /* Quadrant 4     Synchronous Register Clock/Input */
pin 68   =           I68;          /* Quadrant 4     Latch Enable/Input               */
            /**** Quadrant I ****/
/*  I/O LOGIC CELL  */
/*  ==============  */
pin     [4..9]      =             [IO4..9];
pinnode [209..204]  =             [STF4..9];
pinnode [157..152]  =             [IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1];
pinnode [105..100]  =             [IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2];
pin     [10..15,17] =             [IO10..15,IO17];
pinnode [203..197]  =             [STF10..15,STF17];
pinnode [151..145]  =             [IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1];
pinnode [99..93]    =             [IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2];
/* BURIED LOGIC CELL             */
/* ==================            */
pinnode [69..74]    =             [BLC18..23];
            /**** Quadrant II ****/
/* I/O LOGIC CELL   */
/* ==============   */
pin     [18,19,21..24] =          [IO18,IO19,IO21..24];
pinnode [210..215]  =             [STF18,STF19,STF21..24];
pinnode [158..163]  =             [IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1];
pinnode [106..111]  =             [IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2];
pin     [25..31]    =             [IO25..31];
pinnode [216..222]  =             [STF25..31];
pinnode [164..170]  =             [IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1];
pinnode [112..118]  =             [IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2];
/* BURIED LOGIC CELL             */
/* ==================            */
pinnode [80..75]    =             [BLC12..17];
            /**** Quadrant III ****/
/* I/O LOGIC CELL   */
/* ==============   */
```

```
pin      [38..43]    =              [IO38..43];
pinnode [235..230]   =              [STF38..43];
pinnode [183..178]   =              [IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1];
pinnode [131..126]   =              [IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2];
pin      [44..49,51] =              [IO44..49,IO51];
pinnode [229..223]   =              [STF44..49,STF51];
pinnode [177..171]   =              [IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1];
pinnode [125..119]   =              [IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2];
/* BURIED LOGIC CELL                */
/* =================                */
pinnode [81..86]                                    = [BLC6..11];
             /**** Quadrant IV ****/
/* I/O LOGIC CELL   */
/* ==============   */
pin      [52,53,55..58] =           [IO52,IO53,IO55..58];
pinnode [236..241]   =              [STF52,STF53,STF55..58];
pinnode [184..189]   =              [IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1];
pinnode [132..137]   =              [IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2];
pin      [59..65]    =              [IO59..65];
pinnode [242..248]   =              [STF59..65];
pinnode [190..196]   =              [IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1];
pinnode [138..144]   =              [IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2];
/* BURIED LOGIC CELL                */
/* =================                */
pinnode [92..87]     =              [BLC0..5];
/*           INPUT LATCH
   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high,
   the pin value is latched. When the quadrant latch clock is low, the latch becomes
   transparent.                     */
IO4.d    =    !IO4;
IO4.oe   =    IO8.io;
IO4.ce   =    'B'1;
IO7      =   IO4.IOL; /*     When the latched input is needed in the design, i.e.. IO4.IOL, IO4
                            is configured as having a latched input. */
/*           CLOCKING OPTIONS
   There are different methods of clocking the registers in the ATV5000. The clock is
   best described as either the AND function of (Quadrant Clock & Clock Product term)
   or the product term by it self. In the following examples the register can be a
   name from a pin, Q1, Q2, or Buried Logic Cell. The register can be either  .t or .d
   flip-flop.       */
IO22.d   =   !IO22;
IO22.ck  =   IO18 & !IO19;  /* Note there is no .ce equation defined. This is an      */
IO22.ar  =   IO21;          /* asynchronous clocking method where the quadrant clock  */
                            /* has no effect.        */
IO23.d   =    !IO23;
IO23.ce = IO18 & !IO19;             /* The clock product term is used to gate the quadrant    */
IO23.ar =     IO21;                 /* clock pin.Using quadrant clock pin in a synchronous    */
IO24.d   =    !IO24;                /* mode allows higher clock rate. Pin 32 is the Quadrant  */
                                    /* 2 clock pin.           */
IO24.d   =    !IO24;
IO24.ce =     'B'1;                 /* Note that the .ce is defined to 1. The quadrant clock  */
IO24.ar = IO21;                     /* is the only clocking element. The clock is Pin 32      */
                                    /* because it's the proper quadrant clock to use for      */
                                    /* synchronous operation.        */
/*           D-TYPE and T-TYPE REGISTERS
   All the registers in the ATV5000 can be configured as D or T type. Use the .d
   extension for D type register and .t extension for T type register.*/
/* 3 Bit Synchronous Counter using T flip-flops */
```

```
IO38Q2.t = 'B'1;                    IO38Q2.ce = 'B'1; IO38Q2.ar = IO38;
IO39Q2.t = IO38Q2;                  IO39Q2.ce = 'B'1; IO39Q2.ar = IO38;
IO40Q2.t = IO38Q2 & IO39Q2;         IO40Q2.ce = 'B'1; IO40Q2.ar = IO38;
/* 3 Bit Synchronous Counter using D flip-flops */
BLC6.d = !BLC6;                     BLC6.ce = 'B'1;   BLC6.ar = IO38;
BLC7.d = BLC6 $ BLC7;               BLC7.ce = 'B'1;   BLC7.ar = IO38;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ce = 'B'1;        BLC8.ar = IO38;
/*      UNIVERSAL AND REGIONAL PRODUCT TERMS
   A Regional product term has inputs from all the feedbacks of its quadrant Buried
   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal product
   term has the Pin/B Sum Term Feedbacks.*/
/*           OUTPUTS and FEEDBACKS
   Combinatorial:
   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
   13 product terms depending on the need of the reduced equation. If the reduced
   equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
   terms to use.
        IO52                        = up to 5 PRODUCT TERMS (2 UNIVERSAL)
        IO52.oe                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.(d or t)             = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q1.(ck or ce)           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.ar                   =                 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q1.ap                   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)             =                 up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar                   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap                   = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:               SOURCE:
   IO52,IO52.IO                     --                Pin feedback, after the buffer/inverter.
   IO52Q1                           --                Q1 register feedback.
   IO52Q2                           --                Q2 register feedback. */
/* Combinatorial:
   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product terms to use.
Q1 will feedback the A Sum Term portion of the output logic.
        IO52                        =                 up to 9 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)             = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar                   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap                   = 1 PRODUCT TERM (0 UNIVERSAL)
   ALLOWED FEEDBACKS:               SOURCE:
   IO52,IO52.IO                     --                Pin feedback, after the buffer/inverter.
   IO52Q2                           --                Q2 register feedback. */
/* Combinatorial:
   If the reduced equation requires more than 9 product terms, it leaves no product
   terms for Q1 and Q2. Q1 feeds back A. Sum Term and Q2 feeds back C Sum Term.
        IO52                        =                 up to 13 PRODUCT TERMS (4 UNIVERSAL)
        IO52.oe                     =                 1 PRODUCT TERM (1 UNIVERSAL)
   ALLOWED FEEDBACKS:               SOURCE:
   IO52,IO52.IO                     --                Pin feedback, after the buffer/inverter.*/
/* Registered:
   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
   13 product terms depending on the  need of the reduced equation. If the reduced
   equation requires 4 or less product terms, you may define a 5 product term equation
   for the STF (Sum Term Feedback) and define a 4 product
   term equation for Q2.
        IO52.(d or t)               = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52.oe                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)             = 1 PRODUCT TERM (1 UNIVERSAL)
```

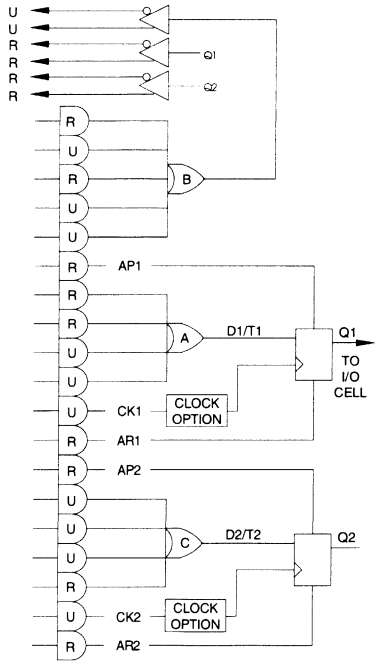
```
        IO52.ar                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap                     = 1 PRODUCT TERM (1 UNIVERSAL)
        STF52       = up to 5 PRODUCT TERMS (2 UNIVERSAL)
        IO52Q2.(d or t)             = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar                   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap                   = 1 PRODUCT TERM (0 UNIVERSAL)
    ALLOWED FEEDBACKS:              SOURCE:
    IO52      --                    Register feedback prior to buffer/inverter.
    IO52Q2    --                    Q2 register feedback.
    STF52     --                    Sum Term Feedback for logic expansion.*/
/*  Registered:
    If the reduced equation requires 9 to 5 product terms, you may write a 4 product
    term equation for Q2.
        IO52.(d or t)               = up to 9 PRODUCT TERMS (3 UNIVERSAL)
        IO52.oe                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.(d or t)             = up to 4 PRODUCT TERMS (1 UNIVERSAL)
        IO52Q2.(ck or ce)           = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar                   = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ap                   = 1 PRODUCT TERM (0 UNIVERSAL)
    ALLOWED FEEDBACKS:              SOURCE:
    IO52.IO   --                    Pin feedback, after the buffer/inverter.
    IO52      --                    Register feedback prior to buffer/inverter.
    IO52Q2    --                    Q2 register feedback.*/
/*  Registered:
    If the reduced equation requires more than 9 product terms, it leaves zero product
    terms for Q1 and Q2.
        IO52.(d or t)               = up to 13 PRODUCT TERMS (4 UNIVERSAL)
        IO52.oe                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.(ck or ce)             = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar                     = 1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ap                     = 1 PRODUCT TERM (1 UNIVERSAL)
    ALLOWED FEEDBACKS:              SOURCE:
    IO52.IO   --                    Pin feedback, after the buffer/inverter.
    IO52      --                    Register feedback prior to buffer/inverter.*/
/*          AP, AR, and CK
    Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
    Reset) and .CK or .CE. All ARs and CKs are Universal product terms. The APs are
    Universal product terms except the APs for Q2.
    NOTE:     AP and AR should never be active at the same time.*/
IO10.d      =     !IO10;
IO10.ck =   IO8;
IO10.ar =   IO11;
IO10.ap =   IO12;
/*          BURIED LOGIC CELLS
    Buried Logic Cell can be configured as a register feedback like Q2. It can also be
    configured as combinatorial feedback to accommodate for logic expansion. */
BLC17.t     =     'B'1;           /*Registered */
BLC17.ck    =     IO9;
BLC17.ar    =     IO21;
BLC14       =     I1;             /*Combinatiorial */
IO25        =     BLC17;
IO26        =     BLC14;
END;
```

Using the ATV5100

The ATV5100 logic cells retain the ATV2500's basic features with two registers, three sum terms and Q1, Q2, and pin feedback options. In addition, these following features make the ATV5100 even more versatile:

1. Input latches are added to every I/O pin. Each latch can be enabled or disabled independently.
2. The ATV5100 can be configured to feedback a combinatorial sum term and send Q1 to the output. Feeding the combinatorial sum term internally makes implementing logic equations with large number of product terms possible without sacrificing an I/O pin.
3. Dedicated clock pins and individual clock product terms create multiple clock options for each flip-flop.
4. The addition of the buried logic cells handles more logic than ever.
5. Each flip-flop can be configured as D- or T-type flip-flop.
6. Asynchronous preset, asynchronous reset and programmable output polarity allow registered outputs using fewer product terms.
7. Same architecture as the ATV5000 with more emphasis on universal routing.

Logic Cell with Buried Sum Term and Register to I/O Cell



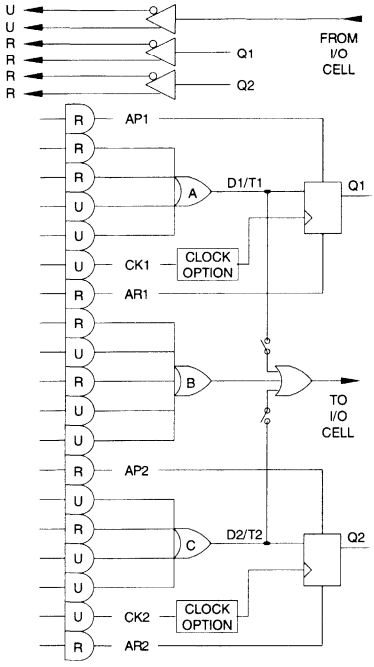
0481A

High Density UV Erasable Programmable Logic Device

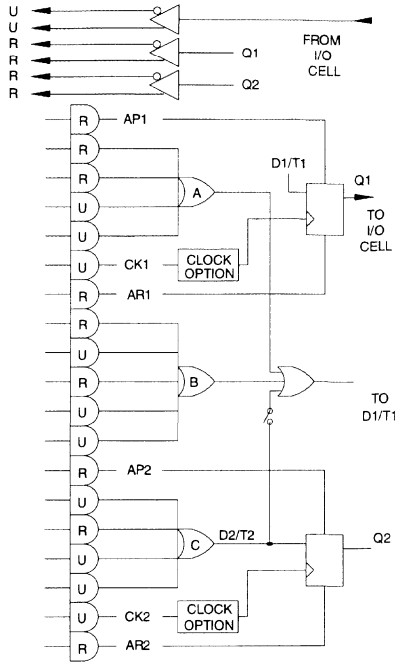
Application Brief

6

Logic Cell, Two Buried Registers, Combinatorial to I/O Cell



Logic Cell with Combinable Sum Terms, Register to I/O Cell



The following are sections of ABEL™ and CUPL™ source files to illustrate how each of these features is described in the ABEL™ and CUPL™ high level description languages.

Pin and Node Assignments

All the buried registers used in the design need to be assigned node numbers. The following tables show the complete set of node numbers by quadrant.

ABEL™ and Atmel-ABEL™

```
LENA,CLOCK pin 1,2;
ACK pin 4
istype 'reg_d,buffer';
OUTA pin 5;
DRAM node 121
istype 'reg_t';
EXPAND node 70;
ACKL node 813;
```

CUPL™

```
pin 1,2 = LENA,CLOCK;
pin 4 = ACK;

pin 5 = OUTA;
pinnode 105 = DRAM;

pinnode 208 = EXPAND;
```

ATV5100 ABEL™ and Atmel-ABEL™ Node Numbers

Quadrant I

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
4	813	761	69	121
5	814	762	70	122
6	815	763	71	123
7	816	764	72	124
8	817	765	73	125
9	818	766	74	126
10	819	767	75	127
11	820	768	76	128
12	821	769	77	129
13	822	770	78	130
14	823	771	79	131
15	824	772	80	132
17	825	773	81	133

6 Buried Logic Cells
B23 - B18 node 173 - 178
LCK1 pin 1;Quadrant Latch clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
18	826	774	82	134
19	827	775	83	135
21	828	776	84	136
22	829	777	85	137
23	830	778	86	138
24	831	779	87	139
25	832	780	88	140
26	833	781	89	141
27	834	782	90	142
28	835	783	91	143
29	836	784	92	144
30	837	785	93	145
31	838	786	94	146

6 Buried Logic Cells
B17 - B12 node 179 - 184
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
38	839	787	95	147
39	840	788	96	148
40	841	789	97	149
41	842	790	98	150
42	843	791	99	151
43	844	792	100	152
44	845	793	101	153
45	846	794	102	154
46	847	795	103	155
47	848	796	104	156
48	849	797	105	157
49	850	798	106	158
51	851	799	107	159

6 Buried Logic Cells
B11 - B6 node 185 - 190
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

Quadrant IV

Pin	Input Latch	Sum Term A	Sum Term B	Sum Term C
52	852	800	108	160
53	853	801	109	161
55	854	802	110	162
56	855	803	111	163
57	856	804	112	164
58	857	805	113	165
59	858	806	114	166
60	859	807	115	167
61	860	808	116	168
62	861	809	117	169
63	862	810	118	170
64	863	811	119	171
65	864	812	120	172

6 Buried Logic Cells
B5 - B0 node 191 - 196
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

ATV5100 CUPL™ Node Numbers

Quadrant I

Pin	Sum Term A	B	C
4	157	209	105
5	156	208	104
6	155	207	103
7	154	206	102
8	153	205	101
9	152	204	100
10	151	203	99
11	150	202	98
12	149	201	97
13	148	200	96
14	147	199	95
15	146	198	94
17	145	197	93

6 Buried Logic Cells
B23 - B18 node 74 - 69
LCK1 pin 1; Quadrant Latch Clock
RCK1 pin 2; Quadrant Synchronous Register Clock

Quadrant II

Pin	Sum Term A	B	C
18	158	210	106
19	159	211	107
21	160	212	108
22	161	213	109
23	162	214	110
24	163	215	111
25	164	216	112
26	165	217	113
27	166	218	114
28	167	219	115
29	168	220	116
30	169	221	117
31	170	222	118

6 Buried Logic Cells
B17 - B12 node 75 - 80
LCK2 pin 34; Quadrant Latch Clock
RCK2 pin 32; Quadrant Synchronous Register Clock

Quadrant III

Pin	Sum Term A	B	C
38	183	235	131
39	182	234	130
40	181	233	129
41	180	232	128
42	179	231	127
43	178	230	126
44	177	229	125
45	176	228	124
46	175	227	123
47	174	226	122
48	173	225	121
49	172	224	120
51	171	223	119

6 Buried Logic Cells
B11 - B6 node 86 - 81
LCK3 pin 35; Quadrant Latch Clock
RCK3 pin 36; Quadrant Synchronous Register Clock

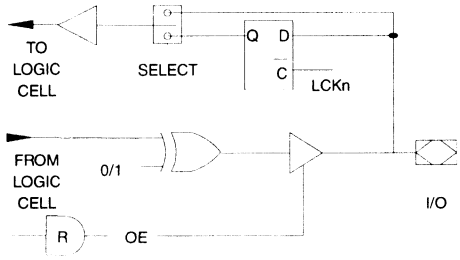
Quadrant IV

Pin	Sum Term A	B	C
52	184	236	132
53	185	237	133
55	186	238	134
56	187	239	135
57	188	240	136
58	189	241	137
59	190	242	138
60	191	243	139
61	192	244	140
62	193	245	141
63	194	246	142
64	195	247	143
65	196	248	144

6 Buried Logic Cells
B5 - B0 node 87 - 92
LCK4 pin 68; Quadrant Latch Clock
RCK4 pin 66; Quadrant Synchronous Register Clock

Input Latch

Each of the 52 I/Os has an input latch that can be enabled and disabled individually. When the latch is enabled and latch clock is high, the pin value is latched. When the quadrant latch clock is low, the latch becomes transparent. When the latch is disabled, an ATV5100 I/O acts like those of the ATV750 and ATV2500 I/Os. The pin input is fed directly to the array (except when sum term B is being used as a buried feedback).



The .D and the .LE (latch enable) equations are required to enable the input latch in ABEL™ AHDL. The only allowed input to the latch is the IO pin with which it is associated. The only allowed .LE input is the quadrant latch clock (pin 1,34, 35, or 68). Notice that CUPL™ does not have node numbers for the input latches. Any pin name used in a feedback with the dot extension IOL tells CUPL™ that particular pin should be a latched pin.

ABEL™ and Atmel-ABEL™	CUPL™
`ACKL.D = ACK;`	
`ACKL.LE = LENA;`	
`OUTA := ACKL;`	`OUTA.D = ACK.IOL;`

Internal Combinatorial Feedback for an I/O Cell

To implement the combinatorial feedback of the B sum term, first define the node name with the corresponding node number. This node will take a five product term equation. Regular syntax describing a combinatorial equation will describe the B sum term.

Note: This B sum term node number is defined only when this feature is needed. When this feature is used, the output is from Q1 through an inverter/buffer. *The I/O pin becomes a output-only pin. It cannot be used as an input or as an input/output.*

ABEL™ and Atmel-ABEL™	CUPL™
`OUTA pin 5;`	`pin 5 = OUTA;`
`EXPAND node 70;`	`pinnode 208 = EXPAND;`
`OUTA.D =`	`OUTA.D =`
`INA&INB# !INC&!IND;`	`INA&INB#!INC&!IND;`
`EXPAND = INA & !INC # IND;`	`EXPAND = INA & !INC # IND;`

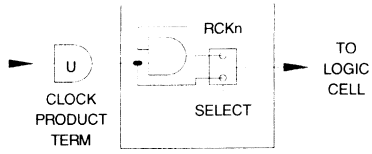
(OUTA and EXPAND are in the same I/O logic cell. OUTA is the Q1 output to pin after the inverter/buffer and EXPAND is the combinatorial sum term feedback. The feedbacks from this logic cell are Q1 before the inverter/buffer, Q2, and the B sum term)

Clocking Options

There are different methods of clocking the registers in the ATV5100. The clock options can best described as either the AND function of (quadrant clock & clock product term) or purely the function of the clock product term (like ATV750 and ATV2500).

Synchronous Operation

The quadrant clock is the only clocking element in this mode of operation. The clock product term must be defined to be equal to 1. In ABEL AHDL, .CK defines the clock product term and .CE is the corresponding quadrant clock.



In CUPL™, .CE has a different implication. The keyword .CE means the user wants the AND function (quadrant clock & clock product term) for the clock.

ABEL™ and Atmel-ABEL™	CUPL™
`OUTA.CK = 1;`	
`OUTA.CE = CLOCK; "CLOCK is pin 2`	`OUTA.CE = 'B'1;`

Gated Synchronous Operation

This clock option still uses the fast quadrant register clock pin, but now it has a gating element. The clock product term enables or disables the clock going to the register.

ABEL™ and Atmel-ABEL™	CUPL™
`OUTA.CK = INX & INY & !INZ;`	
`OUTA.CE = CLOCK; "CLOCK is pin 2`	`OUTA.CE = INX&INY&!INZ;`

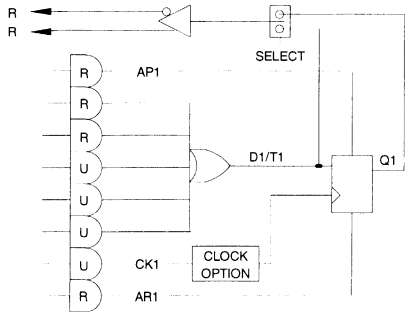
Asynchronous Operation

The quadrant clock has no effect on the register in this mode of clock option. The register is clocked by the clock product term like the ATV750 and ATV2500 registers.

ABEL™ and Atmel-ABEL™	CUPL™
`OUTA.CK =`	`OUTA.CK =`
`INA & !INB & INC;`	`INA & !INB & INC;`

Buried Logic Cells

There are six buried logic cells in each quadrant. Every buried logic cell can be configured as a buried register or as a combinatorial feedback to the quadrant array. In the buried register mode, it's used the same way as Q1 and Q2. In the combinatorial feedback mode, it's used the same way as the B sum term feedback.



ABEL™ and Atmel-ABEL™

```
ADDR,XDATA node 173,174;
ADDR = A16&A15&!A14#RST;
XDATA.T = !A16 & RST;
XDATA.CK = INA & INC;
XDATA.AR = INB;
```

CUPL™

```
pinnode 74,73 =
ADDR,XDATA;
ADDR = A16&A15&!A14#RST;
XDATA.T = !A16 & RST;
XDATA.CK = INA & INC;
XDATA.AR = INB;
```

D-Type and T-Type Registers

All the registers in the ATV5100 can be configured as D- or T-type. The ISTYPE statement after the PIN or NODE definition in ABEL™ AHDL tells ABEL™ which type of register is needed.

ABEL™ and Atmel-ABEL™

```
ABC node 123 istype 'reg_t';
XYZ pin 7 istype 'reg_d';
ABC.T = INA & INB # INC;

XYZ.D = !INA # INC;
```

CUPL™

```
pinnode 103 = ABC;
pin 7 = XYZ;
ABC.T = INA & INB #
INC;
XYZ.D = !INA # INC;
```

In both languages, the .T extension is reserved for T flip-flop and .D extension for D flip-flop.

Asynchronous Preset and Reset

One of the advantanges of having a programmable output polarity I/O is that the same combinatorial output often takes fewer product terms to implement using negative logic rather than positive logic or vice versa.

The same can be done for a registered output provided the power-up state is not crucial (all flip-flops are reset upon power up). With an asynchronous preset and an asynchronous reset, simply swap the two product terms and invert your equation and polarity will let you take advantage of expressing the same logic in a different polarity. The following example shows a four-to-one reduction in product term requirement.

ABEL™ and Atmel-ABEL™

```
OUTC pin 8
istype 'invert,reg_d';
OUTD pin 9
istype 'buffer,reg_d';
OUTC.D =
INA# !INB#INC# !IND;
OUTC.CK = CLK;
OUTC.AR = !INA & RST;
OUTC.AP = INB & PRESET;
OUTD.D =
!INA&INB&!INC&IND;
OUTD.CK = CLK;
OUTD.AR = INB & PRESET;
OUTD.AP = !INA & RST;
```

CUPL™

```
pin 8 = OUTC;

pin 9 = !OUTD;

OUTC.D =
INA#!INB#INC#!IND;
OUTC.CK = CLK;
OUTC.AR = !INA & RST;
OUTC.AP = INB & PRESET;
OUTD.D =
!INA&INB&!INC&IND;
OUTD.CK = CLK;
OUTD.AR = INB & PRESET;
OUTD.AP = !INA & RST;
```

In the ATV5100, all asynchronous reset and preset terms are regional. Hence, their inputs must be from the eight dedicated input pins or from the other regional bus signals (logic cell Q1 and Q2 feedback and buried cell feedback).

Example ABEL™ Description File

```
module  V5100;
title   'Demo ATV5100 features with ATmel-abel (IBM386 or compatible)
        Atmel Corporation PLD        Joe Yu         May 20, 1992'
V5K device 'P5100';
"  The IOs, registers, latches, inputs, and combinatorial sum terms feedbacks are named
"  with the following prefixes for clarity:
"  Prefix
"  I         -      Quadrant Clocks, Latch Enables.
"  IO        -      IO pins
"  IL        -      Input Latches
"  BLC       -      Buried Logic Cells
"  STF       -      Sum Term Feedbacks
"  Valid ABEL AHDL identifiers can be used in place of them.
declarations
I1 pin 1;     " Quadrant 1          Latch Enable/Input
I2 pin 2;     " Quadrant 1          Synchronous Register Clock/Input
I32 pin 32;   " Quadrant 2          Synchronous Register Clock/Input
I34 pin 34;   " Quadrant 2          Latch Enable/Input
I35 pin 35;   " Quadrant 3          Latch Enable/Input
I36 pin 36;   " Quadrant 3          Synchronous Register Clock/Input
I66 pin 66;   " Quadrant 4          Synchronous Register Clock/Input
I68 pin 68;   " Quadrant 4          Latch Enable/Input
"    **** Quadrant I ****
" I/O LOGIC CELL
" ===============
IO4,IO5,IO6,IO7,IO8,IO9                          pin 4,5,6,7,8,9 istype 'buffer,reg_d';
STF4,STF5,STF6,STF7,STF8,STF9                    node 69,70,71,72,73,74;
IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1              node 761,762,763,764,765,766 ;
IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2              node 121,122,123,124,125,126 ;
IO10,IO11,IO12,IO13,IO14,IO15,IO17               pin 10,11,12,13,14,15,17 istype 'buffer,reg_d'
STF10,STF11,STF12,STF13,STF14,STF15,STF17        node 75,76,77,78,79,80,81;
IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1 node 767,768,769,770,771,772,773 ;
IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2 node 127,128,129,130,131,132,133 ;
" INPUT LATCHES
" ===============
IL4,IL5,IL6,IL7,IL8,IL9                          node 813,814,815,816,817,818;
IL10,IL11,IL12,IL13,IL14,IL15,IL17               node 819,820,821,822,823,824,825;
" BURIED LOGIC CELL
" ==================
BLC18,BLC19,BLC20,BLC21,BLC22,BLC23              node 178,177,176,175,174,173 ;
declarations "      **** Quadrant II ****
" I/O LOGIC CELL
" ===============
IO18,IO19,IO21,IO22,IO23,IO24                    pin 18,19,21,22,23,24 istype 'buffer,reg_d';
STF18,STF19,STF21,STF22,STF23,STF24              node 82,83,84,85,86,87;
IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1        node 774,775,776,777,778,779;
IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2        node 134,135,136,137,138,139;
IO25,IO26,IO27,IO28,IO29,IO30,IO31               pin 25,26,27,28,29,30,31 ISTYPE 'BUFFER';
STF25,STF26,STF27,STF28,STF29,STF30,STF31        node 88,89,90,91,92,93,94;
IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1 node 780,781,782,783,784,785,786 ;
IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2 node 140,141,142,143,144,145,146 ;
" INPUT LATCHES
" ===============
IL18,IL19,IL21,IL22,IL23,IL24                    node 826,827,828,829,830,831;
IL25,IL26,IL27,IL28,IL29,IL30,IL31               node 832,833,834,835,836,837,838;
" BURIED LOGIC CELL
" ==================
BLC12,BLC13,BLC14,BLC15,BLC16,BLC17              node 184,183,182,181,180,179;
```

```
declarations "        **** Quadrant III ****
" I/O LOGIC CELL
" ==============•
IO38,IO39,IO40,IO41,IO42,IO43                          pin 38,39,40,41,42,43;
STF38,STF39,STF40,STF41,STF42,STF43                    node 95,96,97,98,99,100;
IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1              node 787,788,789,790,791,792;
IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2              node 147,148,149,150,151,152 istype 'reg_t';
IO44,IO45,IO46,IO47,IO48,IO49,IO51                     pin 44,45,46,47,48,49,51;
STF44,STF45,STF46,STF47,STF48,STF49,STF51              node 101,102,103,104,105,106,107;
IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1       node 793,794,795,796,797,798,799;
IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2       node 153,154,155,156,157,158,159;
" INPUT LATCHES
" ================
IL38,IL39,IL40,IL41,IL42,IL43                          node 839,840,841,842,843,844;
IL44,IL45,IL46,IL47,IL48,IL49,IL51                     node 845,846,847,848,849,850,851;
" BURIED LOGIC CELL
" ==================
BLC6,BLC7,BLC8,BLC9,BLC10,BLC11                        node 190,189,188,187,186,185 ISTYPE 'REG_D';
declarations "        **** Quadrant IV ****
" I/O LOGIC CELL
" ==============
IO52,IO53,IO55,IO56,IO57,IO58                          pin 52,53,55,56,57,58 istype 'buffer';
STF52,STF53,STF55,STF56,STF57,STF58                    node 108,109,110,111,112,113;
IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1              node 800,801,802,803,804,805;
IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2              node 160,161,162,163,164,165;
IO59,IO60,IO61,IO62,IO63,IO64,IO65                     pin 59,60,61,62,63,64,65 istype 'buffer';
STF59,STF60,STF61,STF62,STF63,STF64,STF65              node 114,115,116,117,118,119,120;
IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1       node 806,807,808,809,810,811,812;
IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2       node 166,167,168,169,170,171,172;
" INPUT LATCHES
" ===============
IL52,IL53,IL55,IL56,IL57,IL58                          node 852,853,854,855,856,857;
IL59,IL60,IL61,IL62,IL63,IL64,IL65                     node 858,859,860,861,862,863,864;
" BURIED LOGIC CELL
" ==================
BLC0,BLC1,BLC2,BLC3,BLC4,BLC5                          node 196,195,194,193,192,191;
   H,L,C,D,K,U,X,Z = 1,0,.C.,.D.,.K.,.U.,.X.,.Z.;
"    MACRO (INPUT LATCH)
INPUT_LATCH MACRO (IL,IO,QUAD_LE)
{?IL.D   =    ?IO;
?IL.LE   =    ?QUAD_LE;}
equations
"                    INPUT LATCH
"   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the
"   pin value is latched.
"   When the quadrant latch clock is low, the latch becomes transparent.

IL4.D    =    IO4;    "The .D and the .LE (latch enable) extentions are required to describe a
IL4.LE   =    I1;     "latch in. ABEL AHDL. The only allowed input to the latch is the IO pin
                      "it associates with.The only allowed .LE input is the quadrant latch
                      "enable. They are Pin 1, 34, 35, and 68.
                      "INPUT_LATCH macro is another way to describe the latch.
INPUT_LATCH (IL5,IO5,I1);          "Latch Pin 5
INPUT_LATCH (IL6,IO6,I1);          "Latch Pin 6
IO4.d    =    !IO4.fb; " When .oe is enabled by IO8, IO4 outputs a 1 bit counter.
IO4.oe   =    I34;    " When .oe is disabled by !I34, IO4 latches a data bit  from the bus.
IO4.ck   =    1;
IO4.ce   =    I2;
IO7 =    IL4;
```

```
test_vectors ( "Test the latches...
[I1,I2,I34,IO4]-[IO4,IO7])
[ 0, 0, 1, X ]    ->    [  0, 0 . ]; "Transparent
[ 0, C, 1, X ]    ->    [  1, 1 . ]; "Transparent
[ U, 0, 0, 0 ]    ->    [  Z, 0 . ]; "Disable .oe and latch 0
[ 1, C, 1, X ]    ->    [  0, 0 . ]; "Latched 0
[ 1, C, 1, X ]    ->    [  1, 0 . ]; "Latched 0
[ D, C, 1, X ]    ->    [  0, 0 . ]; "Transparent
[ 0, C, 1, X ]    ->    [  1, 1 . ]; "Transparent
[ 0, C, 1, X ]    ->    [  0, 0 . ]; "Transparent
[ U, 0, 0, 1 ]    ->    [  Z, 1 . ]; "Disable .oe and latch 1
[ 1, 0, 1, X ]    ->    [  0, 1 . ]; "Latched 1
[ 1, C, 1, X ]    ->    [  1, 1 . ]; "Latched 1
[ 1, C, 1, X ]    ->    [  0, 1 . ]; "Latched 1
equations
"   CLOCKING OPTIONS
"   There are different methods of clocking the registers in the ATV5001. The clock is
"   best described as either the AND function of (Quadrant Clock & Clock Product term)
"   or the product term by it self. In the following examples the register can be a name
"   from a pin, Q1, Q2, or Buried Logic Cell. The register can be either .t or.d
"   flip-flop.
IO22.d  =    !IO22.fb;
IO22.ck =    IO18 & !IO19;          "Note there is no .ce equation defined.This is an asynchronous
IO22.ar =    I66;                   "clocking method  where the quadrant clock  has no effect.


test_vectors (
[IO18,IO19,I66 ]    ->    [ IO22 ])
[       0, 0, 1          ]  -> [ . 0];
[       0, 0, 0          ]  -> [ . 0];
[       C, 0, 0          ]  -> [ . 1];
[       C, 0, 0          ]  -> [ . 0];
equations
IO23.d      =  !IO23.fb;
IO23.ck =  IO18 & !IO19;   "The clock product term (.ck) is used to gate the quadrant
                           "clock pin.
IO23.ce =  I32;            "Using quadrant clock pin in a synchronous mode allows higher
                           "clock rate.
IO23.ar =  I66;            "Pin 32 is the Quadrant 2 clock pin.
test_vectors (
[I32,IO18,IO19,I66  ]      -> [ IO23])
[       0, 1, 0,   1          ]  -> [0];
[       C, 0, 0,   0          ]  -> [0]; "Product term blocks quadrant clock
[       C, 1, 0,   0          ]  -> [1]; "Product term enables quadrant clock
[       C, 1, 0,   0          ]  -> [0];
equations
IO24.d      =  !IO24.fb;
IO24.ck =  1;              "Note that the .ck is defined to 1. The quadrant clock is the only
                           "clocking element.
IO24.ce =  I32;            "The .ce is Pin 32 because it's the proper quadrant clock to use for
IO24.ar =  I66;            "synchronous  operation.


test_vectors (
[ I32, I66  ]  ->   [ IO24 ])
[       0, 1       ]      -> [  0 . ];
[       C, 0       ]      -> [  1 . ];
[       C, 0       ]      -> [  0 . ];
[       C, 0       ]      -> [  1 . ];
"    D-TYPE and T-TYPE REGISTERS
"   All the registers in the ATV5001 can be configured as D or T type. The ISTYPE
"   statement after the PIN or NODE definition tells ABEL which type of register is
"   needed.
```

```
"   ABC        node   122 istype 'reg_t';
"   XYZ        pin    5 istype 'reg_d';
"   Use the .t extension for ABC and .d extension for XYZ when you write the equations.

equations
" 3 Bit Synchronous Counter using T flip-flops
IO38Q2.t = 1;                  IO38Q2.ck = 1;IO38Q2.ce = I36;IO38Q2.ar = I68;
IO39Q2.t = IO38Q2;             IO39Q2.ck = 1;IO39Q2.ce = I36;IO39Q2.ar = I68;
IO40Q2.t = IO38Q2 & IO39Q2;    IO40Q2.ck = 1;IO40Q2.ce = I36;IO40Q2.ar = I68;


test_vectors (
[ I36, I68  ]  ->   [ IO40Q2,IO39Q2,IO38Q2])
[        0, 1  ]    ->     [    0,  0,   0  ];
[        C, 0  ]    ->     [    0,  0,   1  ];
[        C, 0  ]    ->     [    0,  1,   0  ];
[        C, 0  ]    ->     [    0,  1,   1  ];
[        C, 0  ]    ->     [    1,  0,   0  ];
[        C, 0  ]    ->     [    1,  0,   1  ];
[        C, 0  ]    ->     [    1,  1,   0  ];
[        C, 0  ]    ->     [    1,  1,   1  ];
[        C, 0  ]    ->     [    0,  0,   0  ];

equations
" 3 Bit Synchronous Counter using D flip-flops

BLC6.d = !BLC6;                 BLC6.ck = 1;BLC6.ce = I36;BLC6.ar = I68;
BLC7.d = BLC6 $ BLC7;           BLC7.ck = 1;BLC7.ce = I36;BLC7.ar = I68;
BLC8.d = BLC8 $ (BLC6 & BLC7); BLC8.ck = 1;BLC8.ce = I36;BLC8.ar = I68;


test_vectors (
[ I36, I68  ]  ->   [BLC8,BLC7,BLC6])
[        0, 1  ]    ->     [   0,  0,   0  ];
[        C, 0  ]    ->     [   0,  0,   1  ];
[        C, 0  ]    ->     [   0,  1,   0  ];
[        C, 0  ]    ->     [   0,  1,   1  ];
[        C, 0  ]    ->     [   1,  0,   0  ];
[        C, 0  ]    ->     [   1,  0,   1  ];
[        C, 0  ]    ->     [   1,  1,   0  ];
[        C, 0  ]    ->     [   1,  1,   1  ];
[        C, 0  ]    ->     [   0,  0,   0  ];
"        UNIVERSAL AND REGIONAL PRODUCT TERMS
"   A Regional product term has inputs from all the feedbacks of its quadrant Buried
"   Logic Cells, Q1's, Q2's,and the dedicated Inputs. In addition, a Universal product
"   term has the Pin/B Sum Term Feedbacks.
"   OUTPUTS and FEEDBACKS
"   Combinatorial:
"   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
"   13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 5 or less product terms, it leaves Q1 and Q2 each with 4 product
"   terms to use.
"           IO52               =   up to 5 PRODUCT TERMS (3UNIVERSAL)
"           IO52.oe            =   1 PRODUCT TERM (REGIONAL)
"           IO52Q1.(d or t)    =   up to 4 PRODUCT TERMS (2 UNIVERSAL)
"           IO52Q1.ck          =   1 PRODUCT TERM (1 UNIVERSAL)
"           IO52Q1.ce          =   QUADRANT CLOCK
"           IO52Q1.ar          =   1 PRODUCT TERM  (REGIONAL)
"           IO52Q1.ap          =   1 PRODUCT TERM  (REGIONAL)
"           IO52Q2.(d or t)    =   up to 4 PRODUCT TERMS (3 UNIVERSAL)
"           IO52Q2.ck          =   1 PRODUCT TERM (1 UNIVERSAL)
"           IO52Q2.ce          =   QUADRANT CLOCK
```

```
"       IO52Q2.ar          =  1 PRODUCT TERM  (REGIONAL)
"       IO52Q2.ap          =  1 PRODUCT TERM (REGIONAL)
"       ALLOWED FEEDBACKS:        SOURCE:
"       IO52               --     Pin feedback, after the buffer/inverter.
"       IO52Q1,IO52Q1.FB   --  Q1 register feedback.
"       IO52Q2,IO52Q2.FB   --     Q2 register feedback.
"   Combinatorial:
"   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
"   terms to use. Q1 will feedback the A Sum Term portion of the output logic.
"       IO52               =  up to 9 PRODUCT TERMS (5 UNIVERSAL)
"       IO52.oe               =  1 PRODUCT TERM (REGIONAL)
"       IO52Q2.(d or t)    =  up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce          =  QUADRANT CLOCK
"       IO52Q2.ar          =  1 PRODUCT TERM (REGIONAL)
"       IO52Q2.ap          =  1 PRODUCT TERM (REGIONAL)
"       ALLOWED FEEDBACKS:        SOURCE:
"       IO52               --     Pin feedback, after the buffer/inverter.
"       IO52Q2,IO52Q2.FB   --     Q2 register feedback.
"       Combinatorial:
"       If the reduced equation requires more than 9 product terms, it leaves no product
"       terms for Q1 and Q2. Q1 feeds back A Sum Term and Q2 feeds back C Sum Term.
"       IO52               =  up to 13 PRODUCT TERMS (8 UNIVERSAL)
"       IO52.oe            =  1 PRODUCT TERM (REGIONAL)
"       ALLOWED FEEDBACKS:        SOURCE:
"       IO52               --     Pin feedback, after the buffer/inverter.
"   Registered:
"   Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
"   13 product terms depending on the need of the reduced equation. If the reduced
"   equation requires 4 or less product terms, you may define a 5 product term equation
"   for the STF (Sum Term Feedback) and define a 4 product term equation for Q2.
"       IO52.(d or t)      =  up to 4 PRODUCT TERMS (2 UNIVERSAL)
"       IO52.oe            =  1 PRODUCT TERM (REGIONAL)
"       IO52.ck            =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52.ce            =  QUADRANT CLOCK
"       IO52.ar            =  1 PRODUCT TERM (REGIONAL)
"       IO52.ap            =  1 PRODUCT TERM (REGIONAL)
"       STF52              =  up to 5 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.(d or t)    =  up to 4 PRODUCT TERMS (3 UNIVERSAL)
"       IO52Q2.ck          =  1 PRODUCT TERM (1 UNIVERSAL)
"       IO52Q2.ce          =  QUADRANT CLOCK
"       IO52Q2.ar          =  1 PRODUCT TERM (REGIONAL)
"       IO52Q2.ap          =  1 PRODUCT TERM (REGIONAL)

"       ALLOWED FEEDBACKS:        SOURCE:
"       IO52.FB,IO52.Q     --     Register feedback prior to buffer/inverter.
"       IO52Q2             --     Q2 register feedback.
"       STF52              --     Sum Term Feedback for logic expansion.
"   Registered:
"   If the reduced equation requires 9 to 5 product terms, you may write a 4 product
"   term equation for Q2.
"          IO52.(d or t)  =  up to 9 PRODUCT TERMS (5 UNIVERSAL)
"          IO52.oe        =  1 PRODUCT TERM (REGIONAL)
"          IO52.ck        =  1 PRODUCT TERM (1 UNIVERSAL)
"          IO52.ce        =  QUADRANT CLOCK
"          IO52.ar        =  1 PRODUCT TERM (REGIONAL)
"          IO52.ap        =  1 PRODUCT TERM (REGIONAL)
"          IO52Q2.(d or t)=  up to 4 PRODUCT TERMS (3 UNIVERSAL)
"          IO52Q2.ck      =  1 PRODUCT TERM (1 UNIVERSAL)
"          IO52Q2.ce      =  QUADRANT CLOCK
```

```
"           IO52Q2.ar       =   1 PRODUCT TERM (REGIONAL)
"           IO52Q2.ap       =   1 PRODUCT TERM (REGIONAL)
"       ALLOWED FEEDBACKS:          SOURCE:
"       IO52                --      Pin feedback, after the buffer/inverter.
"       IO52.FB             --      Register feedback prior to buffer/inverter.
"       IO52Q2              --      Q2 register feedback.
"   Registered:
"   If the reduced equation requires more than 9 product terms, it leaves zero product
"   terms for Q1 and Q2.
"           IO52.(d or t)   =   up to 13 PRODUCT TERMS (8 UNIVERSAL)
"           IO52.oe         =   1 PRODUCT TERM (REGIONAL)
"           IO52.ck         =   1 PRODUCT TERM (1 UNIVERSAL)
"           IO52.ce         =   QUADRANT CLOCK
"           IO52.ar         =   1 PRODUCT TERM (REGIONAL)
"           IO52.ap         =   1 PRODUCT TERM (REGIONAL)
"       ALLOWED FEEDBACKS:          SOURCE:
"       IO52                --      Pin feedback, after the buffer/inverter.
"       IO52.FB             --      Register feedback prior to buffer/inverter.
"       AP, AR, and CK
"       Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
"       Reset) and .CK. AlL CKs are Universal product terms. The ARs and APs are Regional
"       product terms.
"       NOTE:  AP and AR should never be active at the same time.

equations
IO10.d       =      !IO10.fb;
IO10.ck =    IO8;
IO10.ar =    I66;
IO10.ap =    I35;

test_vectors (
[ IO8, I66, I35     ]      -> [ IO10 ])
[       0,  1,  0   ]      -> [  0 . ]; "AR
[       0,  0,  0   ]      -> [  0 . ];
[       C,  0,  0   ]      -> [  1 . ];
[       C,  0,  0   ]      -> [  0 . ];
[       0,  0,  1   ]      -> [  1 . ]; "AP
[       0,  1,  0   ]      -> [  0 . ]; "AR
"       BURIED LOGIC CELLS
"       Buried Logic Cell can be configured as a register feedback like Q2. It can also be
"       configured as  combinatorial feedback to accommodate for logic expansion.

equations
BLC17.t     =   1;   "Registered
BLC17.ck    =   IO9;
BLC17.ar    =   I66;
BLC14       =   I1;  "Combinatiorial
IO25        =   BLC17;
IO26        =   BLC14;

test_vectors (
[IO9, I66,  I1 ]    ->     [ BLC17,BLC14,IO25,IO26])
[       0,  1,  0   ]      -> [  0,  0,  0,  0  ];
[       C,  0,  0   ]      -> [  1,  0,  1,  0  ];
[       0,  0,  1   ]      -> [  1,  1,  1,  1  ];
[       C,  0,  1   ]      -> [  0,  1,  0,  1  ];
[       C,  0,  0   ]      -> [  1,  0,  1,  0 ] ;
END;
```

Example CUPL™ Description File

```
Name          V5100CU;
Partno        NA;
Date          5/20/92;
Revision      01;
Designer      Joe Yu;
Company       Atmel Corporation;
Assembly      NA;
Location      U1;
Device        V5100;
Format        j;
/* Compiled with CUPL 386 version */
/* The IOs, registers, inputs, and combinatorial sum terms feedbacks are named with
/* the following prefixes for clarity:

*   Prefix
 * I          -      Quadrant Clocks, Latch Enables.
 * IO         -      IO pins
 * BLC        -      Buried Logic Cells
 * STF        -      Sum Term Feedbacks
 * Valid CUPL HDL identifiers can be used in place of them. */

pin 1    =   I1;      /* Quadrant 1 Latch Enable/Input*/
pin 2    =   I2;      /* Quadrant 1 Synchronous Register Clock/Input*/
pin 32   =   I32;     /* Quadrant 2 Synchronous Register Clock/Input*/
pin 34   =   I34;     /* Quadrant 2 Latch Enable/Input*/
pin 35   =   I35;     /* Quadrant 3 Latch Enable/Input*/
pin 36   =   I36;     /* Quadrant 3 Synchronous Register Clock/Input*/
pin 66   =   I66;     /* Quadrant 4 Synchronous Register Clock/Input*/
pin 68   =   I68;     /* Quadrant 4 Latch Enable/Input*/
             /**** Quadrant I ****/
/* I/O LOGIC CELL     */
/* ==============    */
pin         [4..9]          = [IO4..9];
pinnode  [209..204]         = [STF4..9];
pinnode  [157..152]         =   [IO4Q1,IO5Q1,IO6Q1,IO7Q1,IO8Q1,IO9Q1];
pinnode  [105..100]         =   [IO4Q2,IO5Q2,IO6Q2,IO7Q2,IO8Q2,IO9Q2];
pin      [10..15,17]        = [IO10..15,IO17];
pinnode  [203..197]         = [STF10..15,STF17];
pinnode  [151..145]         = [IO10Q1,IO11Q1,IO12Q1,IO13Q1,IO14Q1,IO15Q1,IO17Q1];
pinnode  [99..93]           = [IO10Q2,IO11Q2,IO12Q2,IO13Q2,IO14Q2,IO15Q2,IO17Q2];
/* BURIED LOGIC CELL                */
/* ==================               */
pinnode  [69..74]           =   [BLC18..23];
             /**** Quadrant II ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin      [18,19,21..24]     =   [IO18,IO19,IO21..24];
pinnode  [210..215]         =   [STF18,STF19,STF21..24];
pinnode  [158..163]         =   [IO18Q1,IO19Q1,IO21Q1,IO22Q1,IO23Q1,IO24Q1];
pinnode  [106..111]         =   [IO18Q2,IO19Q2,IO21Q2,IO22Q2,IO23Q2,IO24Q2];
pin             [25..31]    = [IO25..31];
pinnode  [216..222]         = [STF25..31];
pinnode  [164..170]         = [IO25Q1,IO26Q1,IO27Q1,IO28Q1,IO29Q1,IO30Q1,IO31Q1];
pinnode  [112..118]         = [IO25Q2,IO26Q2,IO27Q2,IO28Q2,IO29Q2,IO30Q2,IO31Q2];
/* BURIED LOGIC CELL                */
/* ==================               */
pinnode  [80..75]           = [BLC12..17];
             /**** Quadrant III ****/
```

```
/* I/O LOGIC CELL    */
/* ==============    */
pin      [38..43]          =   [IO38..43];
pinnode  [235..230]        =   [STF38..43];
pinnode  [183..178]        =   [IO38Q1,IO39Q1,IO40Q1,IO41Q1,IO42Q1,IO43Q1];
pinnode  [131..126]        =   [IO38Q2,IO39Q2,IO40Q2,IO41Q2,IO42Q2,IO43Q2];
pin      [44..49,51]       =   [IO44..49,IO51];
pinnode  [229..223]        =   [STF44..49,STF51];
pinnode  [177..171]        =   [IO44Q1,IO45Q1,IO46Q1,IO47Q1,IO48Q1,IO49Q1,IO51Q1];
pinnode  [125..119]        =   [IO44Q2,IO45Q2,IO46Q2,IO47Q2,IO48Q2,IO49Q2,IO51Q2];
/* BURIED LOGIC CELL              */
/* ==================             */
pinnode  [81..86]          =   [BLC6..11];
            /**** Quadrant IV ****/
/* I/O LOGIC CELL    */
/* ==============    */
pin      [52,53,55..58]    =   [IO52,IO53,IO55..58];
pinnode  [236..241]        =   [STF52,STF53,STF55..58];
pinnode  [184..189]        =   [IO52Q1,IO53Q1,IO55Q1,IO56Q1,IO57Q1,IO58Q1];
pinnode  [132..137]        =   [IO52Q2,IO53Q2,IO55Q2,IO56Q2,IO57Q2,IO58Q2];
pin      [59..65]          =   [IO59..65];
pinnode  [242..248]        =   [STF59..65];
pinnode  [190..196]        =   [IO59Q1,IO60Q1,IO61Q1,IO62Q1,IO63Q1,IO64Q1,IO65Q1];
pinnode  [138..144]        =   [IO59Q2,IO60Q2,IO61Q2,IO62Q2,IO63Q2,IO64Q2,IO65Q2];
/* BURIED LOGIC CELL              */
/* ==================             */
pinnode  [92..87]          =   [BLC0..5];
/*          INPUT LATCH
   Each of the 52 I/Os has an input latch. When the quadrant latch enable is high, the
   pin value is latched.  When the quadrant latch clock is low, the latch becomes
   transparent.                   */
IO4.d      =       !IO4;
IO4.oe     =       I34;
IO4.ce     =       'B'1;
IO7        =       IO4.IOL;  /* When the latched input is needed in the design, i.e.,  */
                             /*IO4.IOL, IO4 is  configured as  having a latched input. */
/*          CLOCKING OPTIONS
   There are different methods of clocking the registers in the ATV5100. The clock is
   best described as either the AND function of (Quadrant Clock & Clock Product term) or
   the product term by it self. In the following examples the register can be a name
   from a pin, Q1, Q2, or Buried Logic Cell. The register can be either  .t or .d
   flip-flop.      */
IO22.d     =       !IO22;
IO22.ck    =     IO18 & !IO19;  /* Note there is no .ce equation defined. This is an   */
IO22.ar    =     I66;           /* asynchronous clocking method where the quadrant     */
                                /* clock has no effect.              */
IO23.d     =       !IO23;
IO23.ce    =     IO18 & !IO19;  /* The clock product term is used to gate the quadrant */
IO23.ar    =     I66;           /* clock pin.Using quadrant clock pin in a synchronous */
                                /* mode allows higher clock rate. Pin 32 is the        */
                                /* Quadrant 2 clock pin.              */

IO24.d   =  !IO24;
IO24.ce  =  'B'1;              /* Note that the .ce is defined to 1. The quadrant     */
IO24.ar  =  I66;               /* clock is the only clocking element. The clock is    */
                               /* Pin 32 because it's the proper quadrant clock to    */
                               /* use for synchronous operation.             */
/*          D-TYPE and T-TYPE REGISTERS
   All the registers in the ATV5100 can be configured as D or T type. Use the .d
```

```
   extension for D type register and .t extension for T type register.*/
/* 3 Bit Synchronous Counter using T flip-flops */
IO38Q2.t = 'B'1;                  IO38Q2.ce = 'B'1;IO38Q2.ar = I68;
IO39Q2.t = IO38Q2;                IO39Q2.ce = 'B'1;IO39Q2.ar = I68;
IO40Q2.t = IO38Q2 & IO39Q2;       IO40Q2.ce = 'B'1;IO40Q2.ar = I68;
/* 3 Bit Synchronous Counter using D flip-flops */
BLC6.d = !BLC6;                    BLC6.ce = 'B'1;BLC6.ar = I68;
BLC7.d = BLC6 $ BLC7;              BLC7.ce = 'B'1;BLC7.ar = I68;
BLC8.d = BLC8 $ (BLC6 & BLC7);     BLC8.ce = 'B'1;BLC8.ar = I68;
/*       UNIVERSAL AND REGIONAL PRODUCT TERMS
   A Regional product term has inputs from all the feedbacks of its quadrant Buried
   Logic Cells, Q1's, Q2's, and the dedicated Inputs. In addition, a Universal product
   term has the Pin/B Sum Term Feedbacks.                */
/*            OUTPUTS and FEEDBACKS
   Combinatorial:
   Use IO pin name to define the equation. The sum terms may combine to allow 5, 9, or
   13 product terms  depending on the need of the reduced equation. If the reduced
   equation requires 5 or less product terms,it leaves Q1 and Q2 each with 4 product
   terms to use.
            IO52                = up to 5 PRODUCT TERMS (3 UNIVERSAL)
            IO52.oe             =  1 PRODUCT TERM (REGIONAL)
            IO52Q1.(d or t)     =  up to 4 PRODUCT TERMS (2 UNIVERSAL)
            IO52Q1.(ck or ce)   =  1 PRODUCT TERM (1 UNIVERSAL)
            IO52Q1.ar           =  1 PRODUCT TERM (REGIONAL)
            IO52Q1.ap           =  1 PRODUCT TERM (REGIONAL)
            IO52Q2.(d or t)     = up to 4 PRODUCT TERMS (3 UNIVERSAL)
            IO52Q2.(ck or ce)   =  1 PRODUCT TERM (1 UNIVERSAL)
            IO52Q2.ar           =  1 PRODUCT TERM (REGIONAL)
            IO52Q2.ap           =  1 PRODUCT TERM (REGIONAL)
         ALLOWED FEEDBACKS:        SOURCE:
         IO52,IO52.IO           -- Pin feedback, after the buffer/inverter.
         IO52Q1                 -- Q1 register feedback.
         IO52Q2                 -- Q2 register feedback. */
/* Combinatorial:
   If the reduced equation requires 6 to 9 product terms, it leaves Q2 with 4 product
   terms to use. Q1 will feedback the A Sum Term portion of the output logic.
         IO52                =  up to 9 PRODUCT TERMS (5 UNIVERSAL)
         IO52.oe             =  1 PRODUCT TERM (REGIONAL)
         IO52Q2.(d or t)     =  up to 4 PRODUCT TERMS (3 UNIVERSAL)
         IO52Q2.(ck or ce)   =  1 PRODUCT TERM (1 UNIVERSAL)
         IO52Q2.ar           =  1 PRODUCT TERM (REGIONAL)
         IO52Q2.ap           =  1 PRODUCT TERM (REGIONAL)
         ALLOWED FEEDBACKS:        SOURCE:
         IO52,IO52.IO           -- Pin feedback, after the buffer/inverter.
         IO52Q2                 -- Q2 register feedback. */
/* Combinatorial:
   If the reduced equation requires more than 9 product terms, it leaves no product
   terms for Q1 and Q2. Q1 feeds back A. Sum Term and Q2 feeds back C Sum Term.
         IO52                =  up to 13 PRODUCT TERMS (8UNIVERSAL)
         IO52.oe             =  1 PRODUCT TERM (REGIONAL)
         ALLOWED FEEDBACKS:        SOURCE:
         IO52,IO52.IO           -- Pin feedback, after the buffer/inverter.*/
/*       Registered:
         Use IO pin name to define the equation. The sum terms may combine to allow 4, 9, or
         13 product terms depending on the  need of the reduced equation. If the reduced
         equation requires 4 or less product terms, you may define a 5 product term equation
         for the STF (Sum Term Feedback) and define a 4 product term equation for Q2.
         IO52.(d or t)       = up to 4 PRODUCT TERMS (3 UNIVERSAL)
         IO52.oe             =  1 PRODUCT TERM (REGIONAL)
         IO52.(ck or ce)     =  1 PRODUCT TERM (1 UNIVERSAL)
```

```
        IO52.ar           =   1 PRODUCT TERM (REGIONAL)
        IO52.ap           =   1 PRODUCT TERM (REGIONAL)


        STF52                 = up to 5 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(d or t)       =  up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce)     =  1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar             =  1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap             =  1 PRODUCT TERM (REGIONAL)
        ALLOWED FEEDBACKS:        SOURCE:
        IO52                  -- Register feedback prior to buffer/inverter.
        IO52Q2                -- Q2 register feedback.
        STF52                 -- Sum Term Feedback for logic expansion.*/
/* Registered:
   If the reduced equation requires 9 to 5 product terms, you may write a 4 product term
   equation for Q2.
        IO52.(d or t)     =   up to 9 PRODUCT TERMS (5 UNIVERSAL)
        IO52.oe           =   1 PRODUCT TERM (REGIONAL)
        IO52.(ck or ce)   =   1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar           =   1 PRODUCT TERM (REGIONAL)
        IO52.ap           =   1 PRODUCT TERM (REGIONAL)
        IO52Q2.(d or t)   =   up to 4 PRODUCT TERMS (3 UNIVERSAL)
        IO52Q2.(ck or ce) =   1 PRODUCT TERM (1 UNIVERSAL)
        IO52Q2.ar         =   1 PRODUCT TERM (REGIONAL)
        IO52Q2.ap         =   1 PRODUCT TERM (REGIONAL)
        ALLOWED FEEDBACKS:        SOURCE:
        IO52.IO           -- Pin feedback, after the buffer/inverter.
        IO52              -- Register feedback prior to buffer/inverter.
        IO52Q2            -- Q2 register feedback.*/
/* Registered:
   If the reduced equation requires more than 9 product terms, it leaves zero product
   terms for Q1 and Q2.
        IO52.(d or t)     =   up to 13 PRODUCT TERMS (8 UNIVERSAL)
        IO52.oe           =   1 PRODUCT TERM (REGIONAL)
        IO52.(ck or ce)   =   1 PRODUCT TERM (1 UNIVERSAL)
        IO52.ar           =   1 PRODUCT TERM (REGIONAL)
        IO52.ap           =   1 PRODUCT TERM (REGIONAL)
        ALLOWED FEEDBACKS:        SOURCE:
        IO52.IO           --      Pin feedback, after the buffer/inverter.
        IO52              --      Register feedback prior to buffer/inverter.*/
/*            AP, AR, and CK
   Each of the 128 registers has its own .AP (Asynchronous Preset), .AR (Asynchronous
   Reset) and .CK or .CE. All CKs are Universal product terms. The ARs and APs are
   Regional product terms.
   NOTE:     AP and AR should never be active at the same time.*/
IO10.d      =   !IO10;
IO10.ck     =        IO8;
IO10.ar     =        I66;
IO10.ap     =        I35;
/*            BURIED LOGIC CELLS
   Buried Logic Cell can be configured as a register feedback like Q2. It can also be
   configured as combinatorial feedback to accommodate for logic expansion. */
BLC17.t     =        'B'1;  /*Registered */
BLC17.ck    =        IO9;
BLC17.ar    =        I66;
BLC14       =        I1;       /*Combinatiorial */
IO25        =        BLC17;
IO26        =        BLC14;
END;
```

Saving Power with Atmel PLDs

Introduction

Many designers today are looking for ways to reduce power consumption in their designs, to meet expanding market demands for portable and battery-operated products. With the push to add more features to these products while maintaining the same board size and power budget, Programmable Logic Devices with the low power consumption are playing a larger role in design of these products. These devices allow the designer to add more features in the same board space, yet be able to maintain or decrease the overall power consumption of the system. Atmel offers a variety of PLDs in several density classes with pin counts ranging from 20 to 68 pins that have this low power consumption or "L" feature.

Power Consumption for PLDs

Before discussing the detailed features of Atmel's low power PLDs, it is important to point out the two components for PLD power consumption.

1. $P_{average} = nC_{Load} F_{op} (V_{supply})^2$
2. $P_{standby} = I_{cc,sb} * V_{supply}$ = Standby Power when the device is powered down

Where:

$P_{average}$ = average power consumed while outputs are switching

C_{load} = load capacitance on each output pin

n = number of output pins switching

F_{op} = Frequency of operation

V_{supply} = supply voltage.

As shown in equation 1, a designer may be able to reduce the overall power consumption of his or her design by reducing the supply voltage, pin capacitive loading, or operating frequency. However, these alternatives are usually not practical. Another alternative a designer can choose, as equation 2 shows, is to use parts that consume as little standby power as possible during idle periods when the device is not responding to input stimulus. Atmel's Low Power PLDs are ideally suited for this purpose.

Power Consumption Savings with Atmel Low Power ("L") PLDs

Atmel Low Power PLDs save power by powering down automatically to a "standby" or "sleep" mode when no signal transitions occur on the inputs or internal feedbacks of the device. When an input signal transition occurs, the device responds by "waking up" to an active mode. Figure 1 shows the Average Icc vs. Frequency characteristics for Atmel's Standard and Low Power PLDs. For frequencies less than F_{active}, a Low Power device will automatically go through active and standby cycles to reduce the average current consumption. Compared with a Standard Power device, which always remains active, Low Power PLDs offer significant power savings. As the input signal frequency increases, the percentage of time a Low Power device is active will also increase proportionally until F_{active} is approached. For frequencies greater than or equal to F_{active}, a Low Power device will consume about the same amount of current as a Standard Power device.

Standby Mode

When a Low Power device is in the standby mode, the internal fuse array powers down and the device draws standby current, $I_{cc,sb}$ from the system's supply. The device will enter the "standby" mode automatically when no inputs or internal feedbacks have switched within a time period of T_{active}.

Equation 3 shows how to calculate T_{active} for a ATF16V8BL PLD device.

3. $T_{active} = 1/(2* F_{active})$

Where:

T_{active} = Active time period

F_{active} = Cutoff Frequency

For example, on the ATF16V8BL,

$I_{active} = 50mA$, $F_{active} = 40MHz$, and $I_{cc,sb} = 5mA$.

So, $T_{active} = 1/(2 * 40Mhz) = 12.5nsec$.

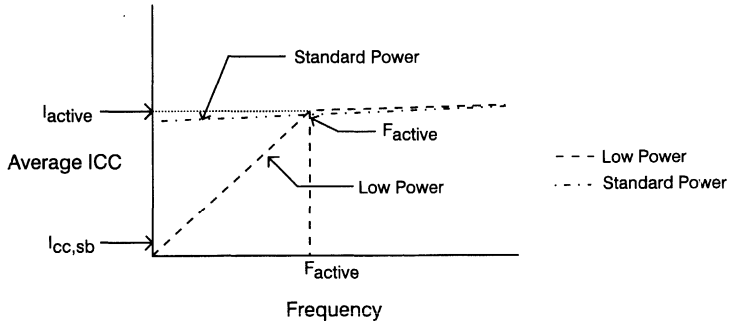
Therefore, if no inputs or feedbacks have switched for 12.5ns, the ATF16V8B will power down to the standby mode and only draw 5mA from the supply.

During the standby mode all logic signals are latched so all outputs and internal feedbacks will remain valid. Since the device powers down to this mode automatically, no separate power down pin is required.

The Active Mode

An Atmel Low Power PLD automatically wakes up to the active mode when it senses an input change from either Low to High or High to Low. When waking up, the internal fuse array is powered up and transient current increases from $I_{cc,sb}$ to a peak value of I_{active}. The current remains at the peak value while the device is awake. The time required for the device to change current from $I_{cc,sb}$ to I_{active} during wake-up or vice versa during power down is called the "wake-up" time or Twake. The wake-up time is already included within the Propagation Delay (Tpd) specification in the Atmel datasheet. Figure 2 shows what happens while the device is awake. In Figure 2(i), the device awoke by a single input transition and saw no additional transitions. Hence, the device will stay awake for T_{active} before entering the standby mode. In Figure 2(ii), the device sees several input transitions after the first transition that woke the device up. Therefore, it will stay awake for T_{active} after the *last* input transition occurs before powering down.

Figure 1. Average Icc vs. Frequency for Atmel Standard and Low Power Devices



Where: $I_{cc,sb}$ = Icc in standby mode.

I_{active} = Icc at Cutoff Frequency

F_{op} = Frequency of operation

F_{active} = Cutoff Frequency

The slopes on Figure 2 show the transient current slew rate required for an Atmel Low Power device to change current from $I_{cc,sb}$ to I_{active} during the wake up time for both the wake-up and power down process. This slew rate can be calculated by equation 4 below,

4. Icc Slew Rate during wake up = $\frac{dI}{dt} = \frac{Iactive - Icc,sb}{T_{wake}}$

during power down = $\frac{-dI}{dt} = \frac{Iactive - Icc,sb}{T_{wake}}$

For example, for a ATF16V8BL device,

I_{active} = 50mA, $I_{cc,sb}$ = 5mA, and *T_{wake} = 3 nsec.*

Therefore, during wake up,

dI/dt = (50mA - 5mA)/(3ns) = 15mA/ns.

During power down the slew rate is negative or -15mA/ns.

Average Icc vs. Peak Icc

The total current required for a low power device to complete an active cycle is the sum of transient and peak currents. Since the transient current cancels during the wake up and power down portions of the active cycle, its total contribution is zero. Therefore, the total current required is the peak current.

The average current required by the device when operating at a particular operating frequency can be approximately related to the peak current in the active cycle by,

5. For $F_{op} = 0$ Average $I_{cc} = I_{cc,sb}$

For $F_{op} < F_{active}$ Average $I_{cc} \sim [F_{op}/F_{active}] * I_{peak} + [1 - (F_{op}/F_{active})] * I_{cc,sb}$

For $F_{op} >= F_{active}$ Average $I_{cc} \sim I_{active}$,

Where:

F_{op} = Frequency of Operation

$I_{peak} = I_{active}$ = Peak Current or current at the cutoff frequency

F_{active} = Cutoff frequency

For example, with an ATF22V10BL device,

For *F_{op} = 30Mhz; F_{active} = 60MHz*, *$I_{peak} = I_{active}$ = 70mA,* and *$I_{cc,sb}$ = 8mA.*

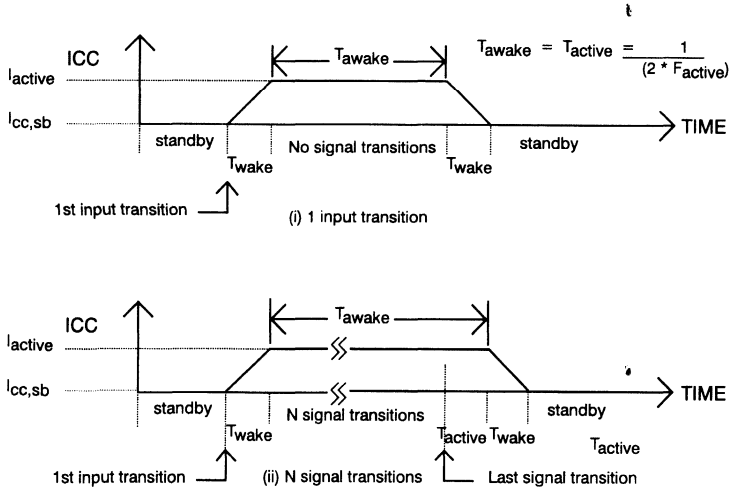
F_{active}, I_{peak}, and $I_{cc,sb}$ are determined from the ICC vs. Frequency curves in the databook,

*Average ICC ~ (30Mhz/60Mhz) * (70mA) + (1 - (30Mhz/60Mhz)) * 8mA = 39mA.*

Therefore, at an operating frequency of 30MHz, the average current drawn by a ATF22V10BL device should be about 39mA.

6

Figure 2. Active Cycle



Supplying Transient and Peak Currents

In many applications with limited power sources, such as battery supplied or portable systems, the transient and peak currents required by the active cycle can be generated by the existing decoupling capacitors on the board. Decoupling capacitors act as a temporary power source to the PLD's supply, supplying a Low Power device with the necessary amount of current so it can undergo active cycles automatically to save power.

To calculate the mininum decoupling capacitance needed, we first need to compute the total amount of charge required during an active cycle and use this amount to derive the capacitance. The total charge needed is ,

6. $Q_{total} = Q_{active} + Q_{transient}$

$I_{transient}$ cancels during the active mode so $I_{transient} = 0$. Therefore, $Q_{transient} = 0$ as well. Substituting this result into equation 6 gives,

7. $Q_{total} = Q_{active} = (I_{active}) * [1/(2*F_{active})]$

The decoupling capacitance required can then be calculated as Q_{total}/dV and is,

8. $$Creq = \frac{I_{active} * [1/(2* F_{active})]}{dV}$$

Where dV is the maximum droop allowed in the supply voltage caused by draining this charge from the capacitors.

For example, with a ATF16V8BL device,

Assume *dV = 100mV maximum, I_{active} = 50mA,* and *T_{active} = 12.5ns.*

Therefore, Q_{active} *= (50mA) * (12.ns) = .63nC* and *Creq = (.63nC)/(100mV) = 6.3nF.*

This is the minimum decoupling capacitance needed to supply the peak and transient currents required for the active time period, in this case 12.5ns.

A .22µF ceramic or tantalum decoupling capacitor placed as close to the supply pin(s) as possible is adequate for supplying both the transient and peak current needs of a Low Power device.

How Duty Cycle affects Power Consumption

A Low Power device normally wakes up twice for each clock input cycle. For example, with a 50% duty cycle input (Case 1, Figure 3), the device wakes up on the rising edge and falling edges of the input. If the input signal width, T_{wh}, is less than or equal to T_{active}, as shown in Case 2 Figure 3, the device will wake up once during each input cycle. From Case 2 Figure 3, we see that the input duty cycle affects the power consumption of a Low Power device by reducing the time it is awake. If the input duty cycle is greater than 50%, the device will consume the same power as in Case 2 Figure 3.

Figure 3. Awake Time vs. Input Duty Cycle

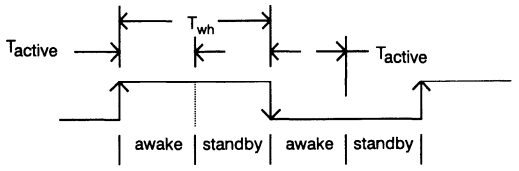


Figure 3 (i) 50% Duty Cycle

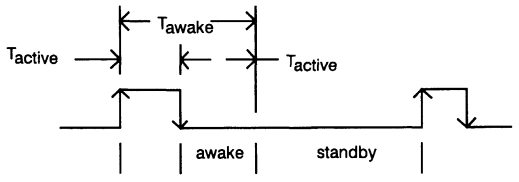


Figure 3 (ii) < 50% Duty Cycle

CASE 1

$T_{wh} => T_{active}$

$T_{awake} = 2 * T_{active}$

2 "Wake-up" cycles per second

CASE 2

$T_{active} > T_{wh} => T_w$,

$T_{awake} = T_{wh} + T_{active}$

1 "Wake-up" cycle per second

T_w = Minimum input width (specified in the Atmel datasheet)

T_{wh} = Input "high" signal width

Atmel PLD Product Selections

In addition to Standard and Low Power PLDs, Atmel also offers Quarter Power and Low Voltage products. These versions are also available with the Low Power feature. Figure 4 shows the Average Icc vs Frequency characteristics for all Atmel PLDs.

Atmel Standard Power and Low Power PLDs.

Atmel Standard Power PLDs are high performance devices whose power consumption remains about the same with frequency. Low Power products approach Standard Power PLD power consumption at higher frequencies but save power at lower frequencies and when the device is idle.

Quarter Power PLDs

Atmel Quarter Power PLDs are available in two versions, a Standard Power Quarter Power part ("Q" suffix) and a Quarter Power device, which has the Low Power feature ("QL" suffix). Both versions have approximately one half the average Icc of a Standard power PLD and consume a quarter of the power of a comparable Bipolar part. The "QL" devices have the Quarter Power active current, plus the Low Power feature.

Atmel Low Voltage PLDs

Atmel Low Voltage PLDs are capable of operating down to 3.0 V. Low Voltage PLDs include the letters "LV" in the device name. These devices save power because they can operate at a reduced supply voltage compared to Standard Power PLDs. Low Voltage PLDs are also available with the Low Power feature and include the "LV" in the part name along with an "L" suffix.

Summary

We have discussed the features of Atmel's Low Power PLD products and have seen that these devices can offer the system designer many benefits for applications where power consumption is a critical requirement. These benefits include:

- ***Low Power Feature in ALL PLD and CPLD products.***

  Designers can use any Atmel PLD or CPLD product, from 20 up to 68 pins, and still take advantage of the Low Power feature.

- ***High Performance AND Power Consumption Savings.***

  Designers can save power in their designs yet not sacrifice overall system operation speed. There is *no* separate delay for the Low Power feature. All delays are included in the Tpd specification in the Atmel datasheet.

- ***No separate Power Down Pin.***

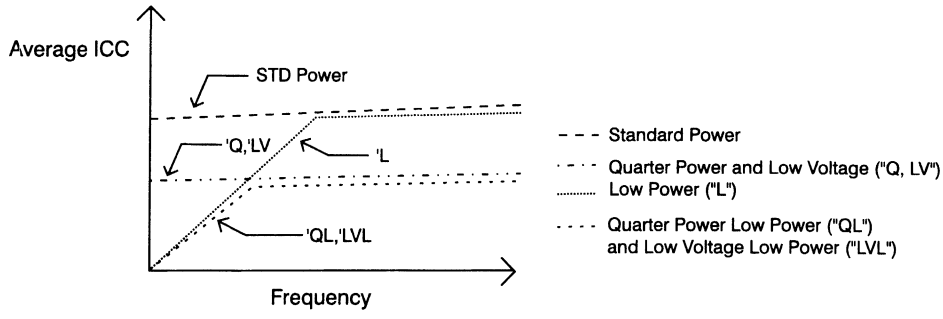
  Atmel's patented "Low Power" feature automatically powers down the device to a low power mode when no inputs or internal feedbacks are switching. Therefore, no separate power down pin is needed, since power down is automatic.

- ***Increased System Reliability.***

  Atmel Low Power parts consume less power, and operate cooler. So thermal related issues are less of a concern in the overall system design.

6

Figure 4. Average Icc vs. Frequency for all Atmel PLDs



Using Programmable Logic Devices

Introduction

This application note covers three areas:

- Where and *why* do I use Programmable Logic Devices (*PLDs*)?
- *How* do I use PLDs?
- Software and hardware *support* for Atmel PLDs.

Where Do I Use PLDs?

Any digital logic design can be done using PLDs. If you normally begin your design by:

- Using AND and OR functions
- Thinking of 7400 series components
- Using truth tables, or
- State diagrams

you are already on the path to using PLDs.

Designing a microprocessor based system, with memory and I/O? How about all that "glue" logic you use to interface with the bus, provide chip selects, and any unusual signals required by special chips? Most of these functions are currently done with 7400 series TTL. *How about using a PLD instead?*

Designing a stand-alone PC board which uses a state machine to control multiple output signals? Using latches to synchronize signals? Using counters to divide down master clock frequencies? Converting parallel-to-serial and back again? All of these functions fit easily in modern PLDs. *Most anything found in your TTL Databook can be replaced with your own, PERSONALIZED, programmable logic device.*

PLD Applications

- **Glue Logic**
- **State Machines**
- **Synchronization**
- **Decoders**
- **Counters**
- **Bus Interfaces**
- **Parallel-to-Serial**
- **Serial-to-Parallel**
- **Subsystems**
- **and Many Others**

Why PLDs?

Maybe you have already heard all the wonderful reasons for using PLDs. Well, they're true! First, let's review some of the more important ones:

- **Increased Integration.** You can reduce the package count of your designs while simultaneously increasing the features offered by your product.
- **Lower Power.** CMOS and fewer packages combine to reduce power consumption.
- **Improved Reliability.** Lower power plus fewer interconnections and packages translate into greatly improved system reliability.
- **Lower Cost.** PLDs reduce inventory costs, too.
- **Easier To Use!** Yes, believe it or not, once you get past the initial learning period, PLDs are easier to use than discrete logic functions.
- **Easier to Change.** Oops! Need to make a change? You won't need "blue wire" when you use a PLD— all changes are internal, and can be done quickly. ECNs are a snap— and system reliability is maintained!

UV Erasable Programmable Logic Device

Application Note

6

0485A

Let's Get Started!

Figure 1 describes the PLD design process. After having read the first part of this application note, you now have the perfect application for a PLD, right? So here you go!

How do you translate your idea into a working prototype? *First, you need a computer with an editor of some kind.* If you have a workstation with a schematic editor, you may input your design using familiar logic blocks. Otherwise, a line or full screen text editor, used in the non-document mode will do. An example of an ABEL™ text file is on the next page.

Next, turn the **logic compiler** loose on your design. First it will *check for typographical errors* and any inconsistencies in your specification. Most compilers then attempt to *reduce your logic* using standard logic reduction theory. Then, a **simulator** will check the test vectors you input, comparing your logic description against the predicted responses. This is an excellent way to verify your design. Check with the appropriate software manuals for more information.

At the end of the compilation process, a *JEDEC* file is output. This file is a standard format accepted by most programming hardware. Next *download this file* to your chosen programmer.

At this point you are ready to "build" your **prototype**. Make sure the programmer has the correct information to program the device you have chosen (an Atmel PLD, of course), plug in your device, and go! Most programmers will even functionally test your prototype for you if you include test vectors in your JEDEC file.

Take your configured PLD, and *plug it into your system.* If you find any errors, just use your editor to make the necessary changes, and repeat the process. It's easy!

Example Design

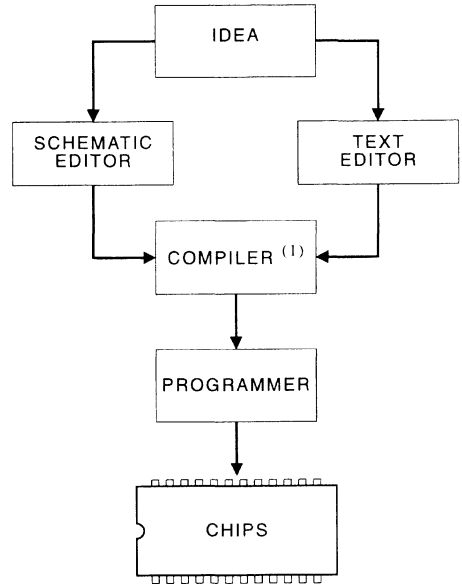
The following design is a simple example using ABEL™ to process the logic description file and an AT22V10 as the target device. The equations are on the next page, and are a direct reproduction of the actual ABEL input file.

Each of the three allowable input formats are shown. A truth table is used to describe a simple 2-to-4 decoder, as is often used to decode chip selects in a microprocessor system. Next, the state machine format is used to describe a divide-by-4 counter. And finally, Boolean equations are used to describe some random logic.

Note the test vectors used to test the device. The "c" nomenclature means that this pin has a low to high to low series of transitions for this vector. Each time this happens, the counter should increment. Also note that the counter starts in the reset condition, which is both outputs "1" for an active low output.

Now you're ready to go - Have fun!

Figure 1. PLD Design Process



Note: 1. Examples of compilers are ABEL™, CUPL™, PLDesigner XL™, and LOG/iC. Each of these products contains modules which allow simulation of your design. They also minimize your logic equations, which gives you flexibility in describing your design.

Example ABEL™ Description File

```
module X3;
title 'Example using 22V10 - KHG 1/6/88';
X310 device 'P22V10';
"
Clk,A12,A13          pin        1,2,3;
CE0,CE1,CE2,CE3      pin        20,21,22,23;
Q1,Q2,CarOut         pin        17,18,14;
CarEn,A,B,C,D        pin        6,7,8,9,10;
Out1,Out2            pin        15,16;
"
X,Z,c          =      .X. , .Z. , .C.;
"
"Counter States
State1         =  ^b00;     State2    =  ^b01;
State3         =  ^b10;     State4    =  ^b11;
"
"The following truth table defines the 2 to 4 decoder, which decodes
"   A13 and A12 into CE0, CE1, CE2, and CE3.
truth_table ([A13,A12] -> [CE0,CE1,CE2,CE3])
[ 0, 0 ]  ->  [ 0, 1, 1, 1 ];
[ 0, 1 ]  ->  [ 1, 0, 1, 1 ];
[ 1, 0 ]  ->  [ 1, 1, 0, 1 ];
[ 1, 1 ]  ->  [ 1, 1, 1, 0 ];
"The following state description defines the divide by 4 counter
state_diagram [Q2,Q1]
State State1:   GOTO   State2;
State State2:   GOTO   State3;
State State3:   GOTO   State4;
State State4:   GOTO   State1;
"   The following equations are general in nature to illustrate Boolean input
"   format.  The CarOut equation uses state 4 above to produce a carry.
Equations
CarOut   =    Q2  &  Q1  &  CarEn;     "& = AND
Out1     =    A &  B +  C &  D;   "+ = OR, AND takes precedence
Out2     =    A &  C +  B &  D;
"The following are the appropriate test vectors
test_vectors
"
([Clk, CarEn, A13,A12, A, B, C, D] - > [CE0,CE1,CE2,CE3,Q2,Q1,CarOut,Out1,Out2]);
[ 0, 0, 0, 0, 0, 0, 0, 0 ]          - > [ 0, 1, 1, 1, 1, 1, 0, 0, 0 ];
[ c, 0, 0, 1, 1, 1, 0, 0 ]          - > [ 1, 0, 1, 1, 0, 0, 0, 1, 0 ];
[ c, 0, 1, 0, 1, 0, 1, 0 ]          - > [ 1, 1, 0, 1, 0, 1, 0, 0, 1 ];
[ c, 0, 1, 1, 0, 0, 1, 1 ]          - > [ 1, 1, 1, 0, 1, 0, 0, 1, 0 ];
[ c, 0, 0, 0, 0, 1, 0, 1 ]          - > [ 0, 1, 1, 1, 1, 1, 0, 0, 1 ];
[ 0, 1, 0, 1, 1, 1, 1, 1 ]          - > [ 1, 0, 1, 1, 1, 1, 1, 1, 1 ];

end X3;
```

Selecting Decoupling Capacitors for Atmel's PLDs

Introduction

This application note provides a summary of information needed when selecting decoupling capacitors for Atmel Programmable Logic Devices. A 0.22-µF, multi-layer ceramic or plastic dielectric capacitor is recommended for such use. Either surface-mount (SMD) or radial-leaded devices should be used. Because of their high parasitic resistance and/or inductance, tantalum, aluminum electrolytic, and axially leaded capacitors are not recommended.

When is a Capacitor Not a Capacitor

Unfortunately, capacitors are not the perfect charge storage devices we would like them to be. Their lead wires and internal construction create parasitic resistance and inductance in series with the capacitance. These parasitics are usually referred to as ESR (equivalent series resistance) and ESL (equivalent series inductance), respectively. As will be shown, these parasitics can seriously reduce the ability of many types of capacitors to decouple supply noise in high-speed systems. Table 1 gives typical ESR and ESL values for various types of capacitors.

As shown, ESR values range from 0.01 ohm to as high as 9 ohms. ESL varies from 2 nH for typical surface mount devices to 20 nH for electrolytic capacitors. These numbers are typical values, taken from data from several manufacturers. As expected, there is some variation between manufacturers. Also, worst case specification values will be significantly higher, especially for ESR values.

How ESR and ESL can Affect High Speed Operation

The effects of these parasitics may be best illustrated by a simple example. Consider the case of a 22V10L. In the standby mode, Icc current is typically only 5 mA. When an input switches, Icc may temporarily go as high as 100 mA. This increase in current draws charge from the local decoupling capacitor. This capacitor current will create voltage drops across the ESR and ESL parasitic elements. To see how these voltage drops can cause problems in a system, look at a typical decoupling application.

In this example the design goal of the capacitor is to keep local supply noise below 0.2 volts, a reasonable expectation. This immediately sets an upper limit on ESR of 2 ohms.

$$ESR_{max} = V_{noise} / I_{max}$$

Imax= Highest Expected Capacitor Current

The upper limit on ESL is determined by how quickly the capacitor's current must change, as well as how much supply noise will be tolerated during that change. For high-speed logic devices, Icc must be able to switch from standby to active levels within 2 to 3 nanoseconds.

$$ESL_{max} = V_{noise} \cdot I_{max} / \Delta t$$

Δt = Time allowed for capacitor current to switch

In this example, an upper limit on ESL of 4 to 6 nH is set.

Consider what can happen if these limits are exceeded. If an axially leaded multi-layer ceramic capacitor with ESR of 0.15 ohm is used, the resistance drop in our application

will not be significant (100 mA X .15 Ohm = 15 mV). However, the inductance will not allow the current to reach 100 mA in 6 nanoseconds. This can slow the logic device switching by several nanoseconds.

What Types to Use: Multi-layered Ceramic and Plastic Dielectrics

From this example, it is apparent that the parasitic elements on capacitors can easily limit their decoupling ability. Therefore, users of high-speed logic need to pick their capacitors with care. The data in Table 1 shows that the best bets are surface-mount, multi-layered ceramic (MLC) or plastic dielectrics. Of the leaded devices, only radial types are recommended.

Within the MLCs, there are different classes of dielectric. Class I has the best characteristics, but its small dielectric constant makes it impractical for decoupling values. Class II is highly recommended, as it has good temperature stability (percent variation -55°C to 125°C) and aging characteristics (10 percent in ten years). Class III, on the other hand, drops to less than 50 percent of its rated capacitance at 85°C, and to only 25 percent at -55°C. Class III dielectric also loses 20 percent of its rated value in ten years. Therefore, Class III MLCs are only recommended for applications where temperature excursions are minimal.

Plastic dielectric capacitors in general offer performance as good as Class II MLCs. Among the dielectrics available today are polypropylene, polyester, polycarbonate, polystyrene and teflon. Capacitance variation with temperature depends on the particular material, but is generally less than ±20 percent from -55°C to 125°C. Aging is minimal, usually less than 2 percent in 10 years. Unfortunately, not many manufacturers make surface-mount plastic dielectric capacitors. That should change soon, as surface-mount technology advances and becomes more common.

When using radial leaded cases, be sure to minimize lead lengths, as ESL increases quickly with longer leads. For example, if a capacitor has 6 nH of inductance with 2 mm leads, extending leads to 5 mm will increase ESL to 10 nH.

What Types Not to Use: Aluminum Electrolytic, Tantalum, and Anything Axial

The design example above together with the numbers given in Table 1 show that some types are not suitable at all for decoupling high-speed devices. Specifically, the high inductance of axially leaded capacitors puts them on the "don't use" list. Also, tantalum and aluminum electrolytic devices are generally not recommended, as they have high ESR and/or ESL, even in radial and surface-mount configurations.

In Any Case, Know Your ESL and ESR

ESR data is often found in catalogs. However, this will normally be only low-frequency data, and ESR is frequency dependent (dropping at higher f). ESL data is not usually given in catalogs. The best thing to do is get Z versus frequency data from the manufacturer. From such a graph (with frequency up to at least 10 MHz), you can extract high frequency ESR and ESL.

How Much Capacitance Do You Need

For decoupling Atmel's PLDs a 0.22-µF capacitor is recommended. In many cases, this will be overkill. However, determining how much less you could get by with for a particular application is dependent upon several factors. The number of PC board supply planes, the board's dielectric thickness and dielectric constant, the value (*and* ESR *and* ESL!) of power entry decoupling capacitors, among other things, will determine just how much is really needed. The best bet is to use a good 0.22-µF and be safe. Besides, the more decoupling is taken care of by local capacitors, the lower the board's HF emissions will be.

Summary

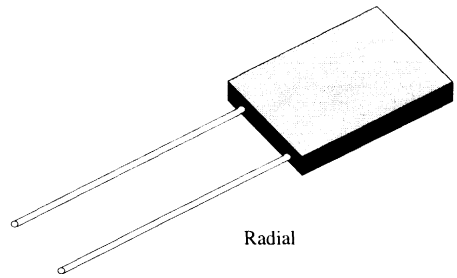
Choosing the right decoupling capacitor is an important part of high-speed circuit design. Choosing the wrong one can introduce supply noise that can slow down signal switching or even end up giving incorrect data. For decoupling Atmel PLDs, 0.22-µF capacitors are recommended. These should be of either multi-layer ceramic or plastic dielectric type. Surface-mount devices are best, with radial leaded cases also being acceptable.

Table 1. Capacitor Types and Recommendation Ratings

Dielectric	Body	L (nH,typ)	R (ohm,typ)	Rating	Comments
Ceramic II	SMD	2	.02	E	Highly recommended
	Radial	6	.07	G	Keep leads short
	Axial	12	.07	S	Axial always = Higher L
Ceramic III	SMD	2	.04	G	C loss hot/cold/old
	Radial	6	.15+	S	
	Axial	12	.15+	X	
Plastics	SMD	2	.03	E	Hard to find
	Radial	5+	.01+	G	Get R and L data
	Axial	12+	.01+	X	
Aluminum Electrolytic	SMD	13	9.0	X	Forget it
	Radial	15+	1.5+	X	
	Axial	20	1.5	X	
Tantalum	SMD	?	3.0	X	
	Radial	10+	1.0	X	
	Axial	15+	1.0	X	

Ratings code:
E Excellent; highly recommended
G Good; will perform well in most applications
S Satisfactory; be aware of specific vendor's device performance
X Not recommended

Axial



Radial

SMD

Using a Programmable Logic Device As a System Controller In an I/O Bus Based System [1]

Summary

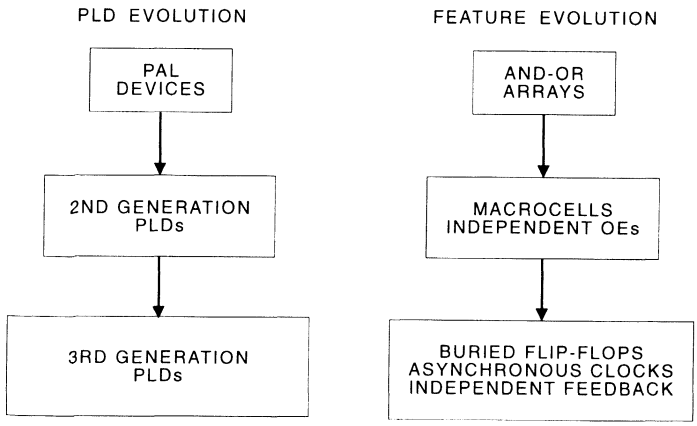
As Programmable Logic Devices (PLDs) become more complex, the amount of logic that can be placed in one device is rapidly increasing. Complete controllers and subsystems now fit into one or two PLDs. As a result, the PLD may now be connected directly to the system bus as an independent peripheral. First generation PAL® devices are difficult to use in these applications. However, recent innovations in PLD architecture enable them to be easily designed into bus-based systems.

PLD Evolution

The driving force behind PLD usage has been to integrate as much of the Small Scale Integration (SSI) logic on a packed PC board as possible. The first level of integration was made possible by the invention of the PAL device. First generation products were usually in 20-pin packages with a typical device having nine dedicated inputs and eight dedicated outputs. One input pin was a dedicated output enable, and one pin a dedicated, common clock for up to eight flip-flops. Making one of these devices work on an I/O bus was difficult and typically was used as little more than a simple latch.

In the mid-eighties, second generation devices appeared. These PLDs are generally in 24 or more pins, have independent output enable controls and *output macrocells*. The macrocells allow the designer to configure each output independently as registered or combinatorial. However, there are still too few registers in these devices to allow the design of complex state machines. Also, these circuits lack independent feedback paths, which further reduce the usable number of registers. This also complicates the use of the output pins as true I/O structures.

Note: 1. This article originally appeared in Northcon '86
®PAL is the registered trademark of Monolithic Memories



Recently several third generation devices (such as the Atmel ATV750) have appeared. These devices are differentiated by the following features:

Extra Registers

Up to twice the usual number. The ATV750 has 20 flip-flops.

Independent Feedbacks

Feedback paths for the registers are independent of the output configuration. In addition, there are separate input paths from the I/O pads.

Asynchronous Clocks

Product terms for each flip-flop's clock allows the designer to break up the registers into different functional blocks.

Control function outputs that have no other use than to manage the other resources inside the PLD need not be brought outside the device, allowing implementation of complex state machines internally.

As PLDs have evolved, so have the applications for them. Initially, PLDs could only integrate a few SSI functions. A typical application was a special-purpose decoder or encoder. With the introduction of more flip-flops, Medium Scale Integration (MSI) functions such as state machines could be designed. Third generation devices are the first true Large Scale Integration (LSI) devices, and are capable of integrating several of the previous generation devices into one package. Now state machines can be combined with an output decoder to control peripheral functions, and still have adequate resources to interface directly to the microprocessor.

System Application

The following example is an application of the Atmel ATV750 as a peripheral resource controller. The design required a state machine, a bus interface unit and a peripheral control interface. All ten outputs of the ATV750 are used, most in the combinatorial mode. However, the 17 required flip-flops were still available to latch the address and data buses, provide a status register, and a two-bit counter. This design would require three second generation, 24-pin PLDs, or five first generation 20-pin devices and at least two other discrete devices. In all, more than 80% of the ATV750 is utilized. The number of gates alone integrated into the ATV750 in this application is more than other 24-pin PLD's have to offer.

The System

The system described is a peripheral controller/bus interface for connecting a special-purpose, custom encryption / exponentiation chip to an 80186 microprocessor (Figure 1). The custom chip has a serial interface, and only one bi-directional pin to indicate its "busy" status. All chip functions are controlled with a set of single-purpose input pins. While simple, this interface is not directly compatible with a modern microprocessor, such as the 80186. The PLD system described not only combines the required glue logic, but also off-loads the parallel-to-serial conversion from the processor. This application note will only touch on the salient features of the design, and why a third generation device is so useful.

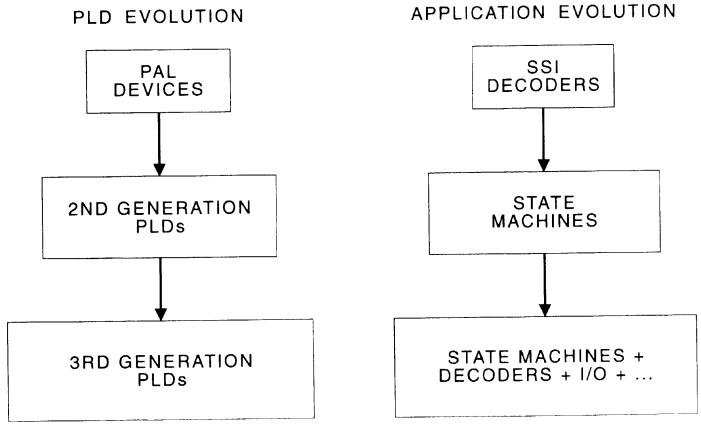
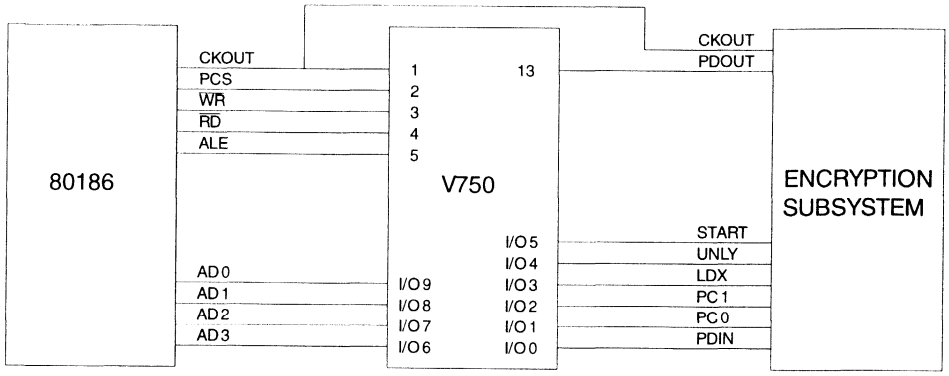


Figure 1. System Diagram



6

The Microprocessor Bus

The 80186 uses a multiplexed address and data bus. Several control signals, such as ALE, $\overline{RD}$ and $\overline{WR}$ tell the system when to get what type of data from the bus. The 80186 also has some internally decoded chip selects, and one is used here for convenience. The system clock is an 8-MHz signal, which is appropriate for the encryption chip and well within this PLD's timing specification. The lower four bits of the address are latched into the PLD to define the upcoming operation, which then allows the PLD to output the requested data in one read cycle of the microprocessor. These address bits are decoded to define the instruction to be executed by the PLD subsystem.

Tackling the I/O Bus

Using first and second generation PLDs, the equations for the I/O bus interface are shown in Figure 2. These equations consume twelve sum terms, eight flip-flops, and twelve output pins. Since this requires two PLDs, another ten input pins are required as well. When rewritten for the ATV750, only four macrocells are required, and eight sum terms and flip-flops. No extra inputs are required, as the ATV750's I/Os are true input/output pins.

The equations for the ATV750 are in Figure 3. This compaction is possible for three reasons:

1. The individual product terms for OE permit the pin to be used as both an input and output.
2. The three feedback paths allow both registers to be used while the pin status is still available to the array.
3. The product term for the flip-flop clock means that the sum term for one of the flip-flops can be shared between the D input and the output pin. A single ATV750 macrocell can incorporate logic which would require up to three output pins and one input pin in other PLDs.

Figure 2.

```
ad0 =    adp0 & !pcs & !rd & ai0 & !ai2                " output data
   #     !pc0 & !pcs & !rd & !ai0 & !ai2               " status "
   #     yst & !pcs & !rd & !ai0 & !ai2;               " status unly

ad1 =    adp1 & !pcs & !rd & ai0 & !ai2                " output data
   #     !pc1 & !pcs & !rd & !ai0 & !ai2;              " status "

ad2 =    adp2 & !pcs & !rd & ai0 & !ai2                " output data
   #     xst & !pcs & !rd & !ai0 & !ai2                " status "
   #     !pc0 & !pcs & !rd & !ai0 & !ai2               " status  "
   #     !pc1 & !pcs & !rd & !ai0 & !ai2;              " status  "

ad3 =    adp3    & !pcs & !rd & ai0 & !ai2             "  output data
   #     startqb & !pcs & !rd & !ai0 & !ai2;           "  status "

adp0     :=   ad0 & !pcs & !wr                         "  load data
   #     pdout & !ystb                                 "  circulate y"
   #     pdout & !xstb                                 "  circulate x"
   #     pdout & !pcs0                                 "  circulate load"
   #     pdout & !pcs1                                 "  circulate load"
   #     adp0 & ystb & xstb & pcs0 & pcs1 & pcs        "  hold data"
   #     adp0 & ystb & xstb & pcs0 & pcs1 & wr;        "  hold data"

adp1     :=   ad1 & !pcs & !wr                         "  load data
   #     adp0 & !ystb                                  "  circulate y"
   #     adp0 & !xstb                                  "  circulate x"
   #     adp0 & !pcs0                                  "  circulate load"
   #     adp0 & !pcs1                                  "  circulate load"
   #     adp1 & ystb & xstb & pcs0 & pcs1 & pcs        "  hold data"
   #     adp1 & ystb & xstb & pcs0 & pcs1 & wr;        "  hold data"

adp2     :=   ad2 & !pcs & !wr                         "  load data
   #     adp1 & !ystb                                  "  circulate y"
   #     adp1 & !xstb                                  "  circulate x"
   #     adp1 & !pcs0                                  "  circulate load"
   #     adp1 & !pcs1                                  "  circulate load"
   #     adp2 & ystb & xstb & pcs0 & pcs1 & pcs        "  hold data"
   #     adp2 & ystb & xstb & pcs0 & pcs1 & wr;        "  hold data"

adp3     :=   ad3 & !pcs & !wr                         "  load data
   #     adp2 & !ystb                                  "  circulate y"
   #     adp2 & !xstb                                  "  circulate x"
   #     adp2 & !pcs0                                  "  circulate load"
   #     adp2 & !pcs1                                  "  circulate load"
   #     adp3 & ystb & xstb & pcs0 & pcs1 & pcs        "  hold data"
   #     adp3 & ystb & xstb & pcs0 & pcs1 & wr;        "  hold data"

ai0 :=   ad0 & pcs                                     "  idle state "
   #     ad0 & ale                                     "  idle state "
   #     ai0 & !pcs & !ale;                            "  hold instruction"

ai1 :=   ad1 & pcs                                     "  idle state "
   #     ad1 & ale                                     "  idle state "
   #     ai1 & !pcs & !ale;                            "  hold instruction"

ai2 :=   ad2 & pcs                                      idle state "
   #     ad2 & ale                                     "  idle state "
   #     ai2 & !pcs & !ale;                            "  hold instruction"

ai3 :=   ad3 & pcs                                     "  idle state "
   #     ad3 & ale                                     "  idle state "
   #     ai3 & !pcs & !ale;                            "  hold instruction"
```

Figure 3.

```
ai0.ck  =    clk2 & !ale; ai2.ck  =      clk2 & !ale;"clock instruction
ai1.ck  =    clk2 & !ale; ai3.ck  =      clk2 & !ale;"clock instruction

ai0 =    ad0 & !pcs & ale                          "load instruction"
   #     adp0 & !pcs & !rd & ai0 & !ai2            "output data
   #     !pc0 & !pcs & !rd & !ai0 & !ai2           "status "
   #     yst & !pcs & !rd & !ai0 & !ai2            "status unly

ai1 =    ad1 & !pcs & ale                          "load instruction"
   #     adp1 & !pcs & !rd & ai0 & !ai2            "output data
   #     !pc1 & !pcs & !rd & !ai0 & !ai2;          "status "

ai2 =    ad2 & !pcs & ale                          "load instruction"
   #     adp2 & !pcs & !rd & ai0 & !ai2            "output data
   #     xst & !pcs & !rd & !ai0 & !ai2            "status "
   #     !pc0 & !pcs & !rd & !ai0 & !ai2           "status  "
   #     !pc1 & !pcs & !rd & !ai0 & !ai2;          "status  "

ai3 =    ad3 & !pcs & ale                          "load instruction"
   #     adp3    & !pcs & !rd & ai0 & !ai2         "output data
   #     startqb & !pcs & !rd & !ai0 & !ai2;       "status "

enable ad0   =      !pcs & !rd;   enable ad2  =      !pcs & !rd;
enable ad1   =      !pcs & !rd;   enable ad3  =      !pcs & !rd;
(adp equations remain the same as before, but are now buried in the macrocell)
```

Figure 4.

```
!pc0    =    !clk22 & !pcs0;

!pc1    =    !clk22 & !pcs1;

!pcs0   :=   ai2 & ai0 & start
   #    !cn0 & count & !pcs0
   #    !cn1 & count & !pcs0

 !pcs1  :=   ai1 & ai2 & start
   #    !cn0 & count & !pcs1
   #    !cn1 & count & !pcs1;
   #    !cn1 & count & !pcs1;
```

The Chip Interface

The encryption chip is loaded and unloaded serially, four bits at a time in this design. The equations for the interface logic are in Figure 4. Also in this figure is a simple state diagram for the two-bit counter required for this design. This state machine is buried, and its decoded outputs are used to control the serial transfers.

Starting the Peripheral Chip

To begin execution in the peripheral chip, a bi-directional signal named *start* is asserted. This is an active low signal. The controller must assert this signal low for four clock cycles. Then the exponentiation chip will hold this line low until it has completed its operations. An external pull up resistor is required. The internal flip-flop, whose output is named *stint*, contains the state of the peripheral. This is used to signal the microprocessor that the subsystem is busy when the processor reads the ATV750's status.

Multiplexing Flip-Flop Inputs and I/O Pins

One I/O pin / flip-flop combination can be used to store the state of the encryption chip and to output this to the peripheral. This is accomplished by multiplexing the sum term output between the flip-flop's D input and the output buffer. The sum term and the OE product term are active to begin the encryption chip's exponentiation cycle. After the state machine counter finishes counting, the output is put into the high impedance state. If the external chip has begun its operation correctly, it will then hold the pin low. Now the state of the I/O pin is used as the D input to the flip-flop, but not output because the OE term is off. The multiplexed macrocell is in Figure 7. The following simple equations are all that is required to implement this logic:

```
enable start              =!count;
stint                     :=!coun
# !start & count;
start.c                   =clk2;
```

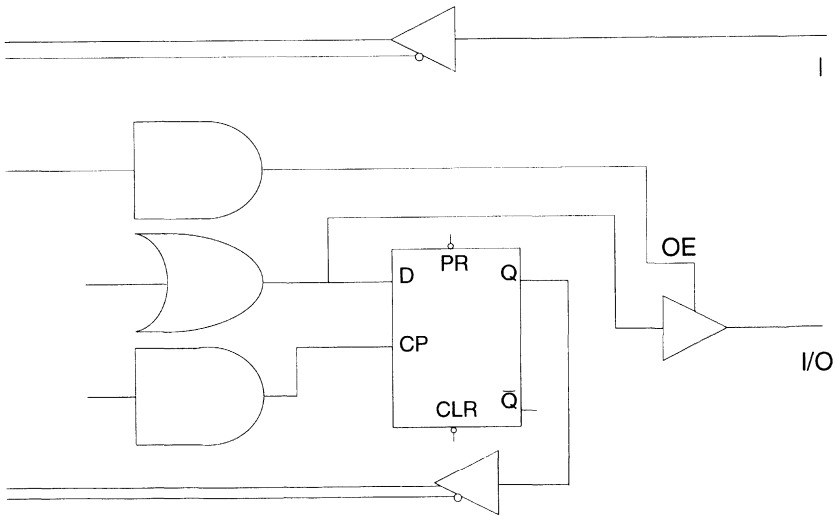
Conclusion

The application of a third generation EPLD in an I/O bus based system demonstrates the usefulness of the following features:

- **Buried Registers**
- **Independent Feedback Paths**
- **Asynchronous Register Clocks**

This design consists of roughly 600 gates, which fit into a ATV750 gate complexity PLD with 80% utilization factor. Due to the usefulness of the new features and their implementation in the macrocell of the ATV750, this design, which would have required three second generation devices, could easily fit into one ATV750.

Mulitplexed "D" Input



Testing Non-Windowed OTP PLDs

Atmel's testing of non-windowed OTP PLDs is comprehensive and thorough. It is sufficient to guarantee programmability and performance. The wafer-probe test checks 100% of all memory elements for programmability. Final test of packaged units checks programming a second time. Performance testing on the *Quality Test Array* (QTA) guarantees AC test parameters. This data shows a high degree of correlation with standard array performance data.

Introduction

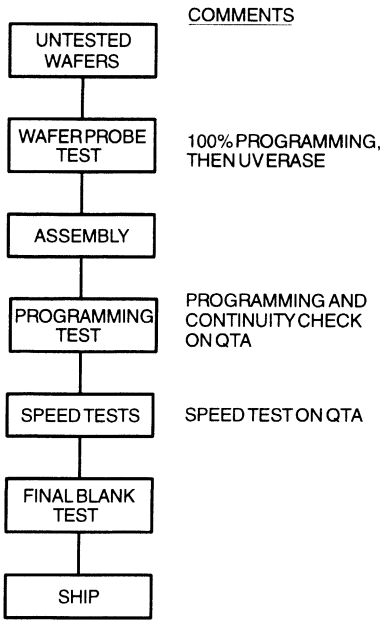
Atmel's corporate goal is to meet or exceed our customers' requirements 100% of the time. This means we must prove to ourselves that each product shipped will perform as specified or better.

PLDs must meet two different device requirements: they must program as a memory device, and they must function as a logic device. This requires testing all devices in two very different ways.

The programmable elements in Atmel's OTP PLDs are UV EPROM memory cells. The AND array programs like an EPROM. UV light cannot penetrate non-windowed packages (e.g., any plastic package or solid lid ceramic package). Erasing a non-windowed EPROM element is not possible. Any testing by Atmel before shipment cannot program the main AND array or the customer cannot enter his own pattern.

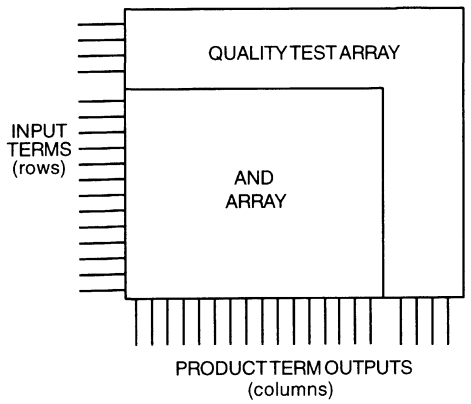
Atmel's test methodology guarantees our PLDs will program and perform to the data sheet, even without programming this main AND array.

Figure 1. Non-Windowed OTP Test Flow



0486A

Figure 2. PLD Topography



Programming

After wafer fabrication, the first test is wafer-probe (Figure 1). All PLD dice manufactured by Atmel use a similar wafer test program. This test programs one-hundred percent of the memory bits used to implement the AND array in our PLDs. This programming algorithm is more aggressive than that implemented by programming manufacturers. After verifying all bits, the wafer is then UV erased before proceeding further.

Package assembly is next. If the packaging used does not have a UV translucent window, the customer is the only one who can program the device. Atmel must guarantee performance and programming by testing other EPROM cells in the device.

These other EPROM cells are next to the main AND array. A discussion of the PLD AND array topography clarifies how to test the extra EPROM cells (Figure 2).

Product term inputs enter the AND array from one end, and form the *rows* of the matrix. Product term outputs leave from the bottom— product terms form the *columns* of the matrix. On the far right of Figure 2 are the Quality Test Array product terms (columns). At the top of the array are the QTA input terms (rows).

Even though wafer-probe tests all units' programming, packaged units also have their QTA terms tested. Since these terms are physically at the ends of the inputs and outputs, this test checks the integrity of these lines. The test detects any shorts or opens on the inputs or outputs. Programming these locations also provides a thorough test of the programming circuitry.

The wafer-probe test programs one-hundred percent of all locations, and the package test checks the programming circuitry for continuity and programmability.

Performance Testing

The logic test parameters divide into two groups: DC and AC test values. All of the DC test parameter tests are independent of the logic programmed into the device. This means that DC testing is the same for every PLD sold by Atmel, independent of the package used.

Every different logic implementation results in different AC performance. Atmel measures AC performance using a "worst case" pattern. This pattern is slightly different in nature for each PLD. This pattern uses every resource available in the device. Outputs can be made to switch in the same direction at the same time. The test program applies worst case combinations of input term and product term patterns to the device. Atmel collects AC data with this pattern on each UV erasable device shipped.

Non-erasable devices cannot use their main array for this test. Atmel programs a special speed test pattern into the QTA. Tests on this array measure all of the same AC characteristics as those done on erasable units. Correlations between the main array and the QTA follow.

Correlation

Three parameters measured on 26 units show a high degree of correlation between windowed PLD testing and non-windowed PLD testing. Measurements of T_{CO}, T_S, and T_{PD} show little difference between performance testing on the standard array versus performance testing on the QTA.

T_{CO} (clock to output) is independent of the memory array. The signal path is directly from the clock input buffer to all ten flip-flops in the AT22V10, and then straight to the output buffer. The data shows a very tight distribution, and the difference in the two measurement techniques is within the accuracy of the setup (see Table 1).

T_S (setup time) and T_{PD} (propagation delay) are dependent on the EPROM array. The data shows an excellent correlation, with the non-windowed test actually measuring slower than the windowed test. Atmel engineers carefully designed the quality test array to use the worst case paths for all conditions. This combination is not available to the user, but guarantees that the QTA speed path will be slower than the user's speed path (see Table 2).

Summary

Atmel thoroughly tests all its PLDs independent of the package used. Programming tests check one-hundred percent of the memory elements on all units shipped. Performance testing on the Quality Test Array measures all AC test parameters with "worse than" worse case conditions. Data taken with both the non-windowed and the windowed performance tests demonstrates that the non-windowed test is accurate and has extra guardband. Customers can feel confident that Atmel's PLDs meet their performance criteria independent of the package chosen.

Table 1. T_{CO} Performance Testing Comparison

Parameter Test	T_{CO} Window	T_{CO} Non-Window	Delta
Average	8.91 ns	8.68 ns	+0.23 ns
Std. Dev.	0.18 ns	0.15 ns	0.06 ns

Table 2. T_S and T_{PD} Performance Testing Comparison

Parameter Test	T_S Window	T_S Non-Window	Delta	T_{PD} Window	T_{PD} Non-Window	Delta
Average	6.80 ns	6.97 ns	-0.17 ns	13.92 ns	14.17 ns	-0.25 ns
Std. Dev.	0.09 ns	0.11 ns	0.09 ns	0.25 ns	0.25 ns	0.18 ns

Designing with the Atmel-ViewPLD Development Tool

Like the Atmel-ABEL™ software, the Atmel-ViewPLD development tool uses a popular industry-standard CAE development system. The development tool integrates the Viewlogic Workview software as the design environment with Data I/O's back-end technology of device fitting and fusemapping. With this development tool, a designer can use schematic capture and/or the ABEL™ Hardware Description Language (ABEL HDL) to functionally describe his or her design requirements. Additionally, the development tool also allows the designer's previous PLD designs in the form of JEDEC files to be read and modelled so that the schematic representations of the designs can be generated.

In this application note, the Atmel-ViewPLD features developed specifically for Atmel PLDs are discussed. Also included are the design hints which allow your designs to be efficiently fitted into your favorite Atmel PLD, and the Schematic-to-JEDEC and ABEL-to-JEDEC compilation process flows. Below is a listing of the topics covered in this application note:

- The Atmel-ViewPLD Menu Commands "Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)"
- The DIO and DSTD symbols
- Using the IN.1 and OUT.1 symbols for your design input and output pins
- Setting your input signal to a constant logic level
- Applying the D_LATCH.1 and IN_LATCH.1 symbols for the ATV5000 or ATV5100 devices
- What to do with the unused pins of a DSTD symbol
- Creating a Viewdraw schematic from an ABEL™ or a JEDEC file
- Simulating your design using worst-case timing values

For your reference, the DIO primitive and DSTD symbols are listed at the end of this application note.

The Atmel-ViewPLD Menu Commands

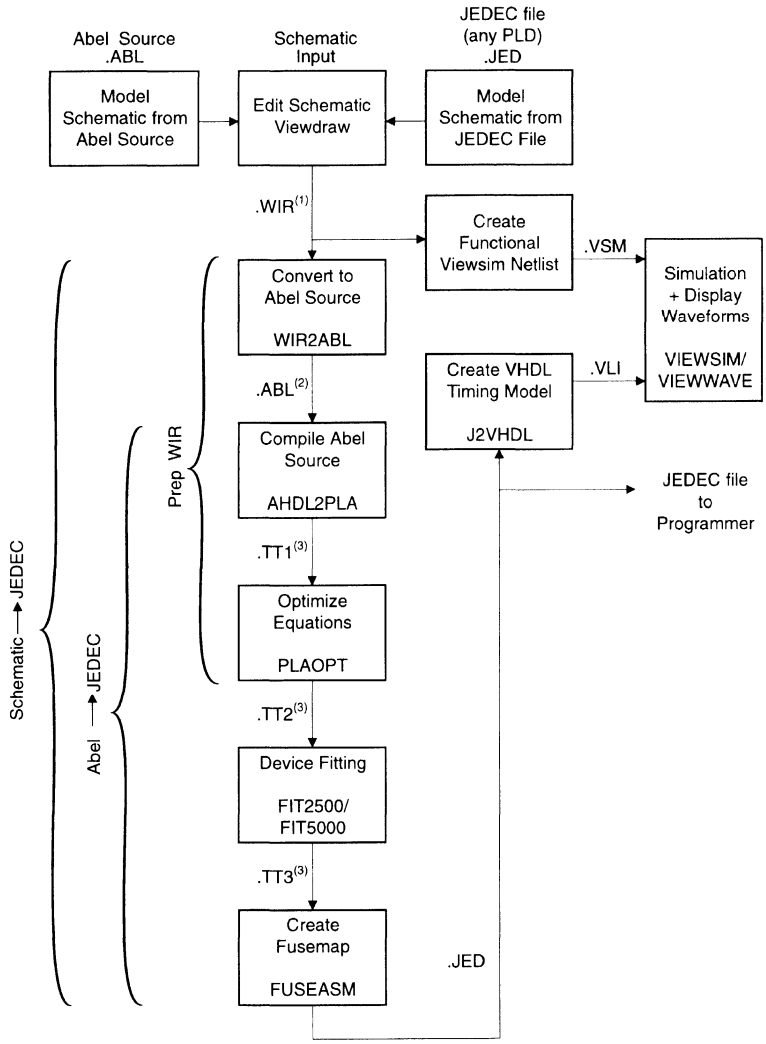
"Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)"

These commands are set up so a device-independent design can be optimized by taking into account the architecture of a specific Atmel PLD selected by the designer. In short, the design optimization procedure enables a more efficient device fitting process to be performed. Using menu commands such as the "Schematic → JEDEC" and "ABEL → JEDEC" commands, a designer can create the JEDEC files for his or her designs with a single click of the mouse button.

Like many ViewPLD menu commands in the WORKVIEW design environment, the "Schematic → JEDEC," "ABEL → JEDEC," and "Prep WIR (Device)" commands execute the WORKVIEW macros (refer to the "Workview Reference" section in Volume 1 of your WORKVIEW manual), which in turn run one or more executable files (.EXE) to generate some type of output files. For instance, if you select the "Schematic → JEDEC" menu command for P2500 (ATV2500 DIP), the command executes the macro file SCH2500.MAC in the WORKVIEW\STANDARD or WORKVIEW\ATMEL directory. The process of compiling the schematic to the JEDEC file is then displayed on the screen. If the design does not encounter any errors during the compilation process, the designer may not be required to know the details of the process. However, it would be advantageous for the designer to understand each process step, especially when the design encounters some compilation errors.

Note that prior to executing the "Schematic → JEDEC" or "Prep WIR (Device)" menu command, you would first need to open your design schematic via Viewdraw. These commands will read in the schematic file name that is currently opened. For the "ABEL → JEDEC" menu command, the design file name will be prompted for immediately after execution of the command.

Figure 1. The Atmel-ViewPLD Compilation Process



Notes:
1. A WIR file is created by Viewdraw only after executing a "File Write" command in Viewdraw.
2. Before generating the Abel™ (.ABL) file, the WIR2ABL (WIR-to-ABEL) generates an intermediate file with extension .VNT. If an error occurs in the WIR-to-ABEL conversion specifying that there is an intermediate file error, then the error description will listed in this .VNT file.
3. The files .TT1, .TT2, and .TT3 are in the Open ABEL PLA format.

The DIO and DSTD Symbols

Like all other CAE primitive symbols, the DIO primitive symbols provide the building blocks for implementing an Atmel-ViewPLD design. In the Atmel-ViewPLD development tool, all of the functional DIO symbols such as AND2, AND4, DFF, and TFFC, are logically described using Boolean equations in the functional library files. These files, which include V2500.FLB, V5000.FLB, and VIEWLOGI.FLB, are located in the WORKVIEW\STANDARD\LIB4 or WORKVIEW\ATMEL\LIB4 directory. Figure 2 illustrates the AND2 and TFF symbols and their logic representations in the functional library file.

As shown in Figure 2, the architectural capabilities in each Atmel PLD determine the type of equation in the function library file. In fact, there are some DIO symbols which are not applicable for some of the Atmel PLDs because of their architecture limitations. For instance, the DFFPC symbol, which is a D-type flip-flop with asynchronous preset and clear controls, is applicable for the ATV5000 and ATV5100 devices, but not for the ATV750 and ATV2500 devices. Please refer to the DIO Library listing for the complete information on the applicabilities of the DIO symbols.

Table 1 shows the three functional library files included with the Atmel-ViewPLD development tool:

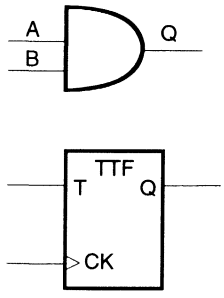
Table 1. Function Library Files

FLB File	Description
V2500.FLB	Logic equations optimized for ATV750 and ATV2500 devices
V5000.FLB	Logic equations optimized for ATV5000 and ATV5100 devices
Viewlogi.FLB	Generic library called by the "PREP WIR" command, not the "Prep WIR (Device)" command

The first two library files are optimized for the ATV750, ATV2500, and ATV5000/5100 device families. The third file, VIEWLOGI.FLB, is used by the "Prep WIR" menu command. This command is designed for use if the designer wishes to partition his or her design into multiple designs which are optimized for the devices selected by the designer. Since each functional library file is in ASCII format, the logic equations representing the DIO symbols can easily be modified by the designer. This flexibility allows the designer to generate his or her own DIO primitive symbols.

For more information on the DIO and DSTD symbols, please refer to the DSTD listings. Note that the DSTD symbols are the 74-Series TTL symbols which are made up of the DIO primitive symbols.

Figure 2. The AND2 and TFF DIO Symbols and their Logic Equations in the V2500.FLB and V5000.FLB Files



Using the IN.1 and OUT.1 Symbols for your Design Input and Output Pins

For creating the input and output pins for your design, you would need to add the IN.1 and OUT.1 symbols (see Figure 3) from the DIO library to your design. Simply use the "Add Comp" menu command to add the IN.1 or OUT.1 symbol to the dangling input nodes. Pin labels must also be assigned to these symbols, and not assigned to the nets or nodes. For a design to be compiled successfully, you must have at least one input pin defined. Note that a design will simulate properly via Viewsim without any IN.1 and OUT.1 symbols (see Figures 3-4).

Figure 3. IN.1 and OUT.1 DIO Symbols[1]

Symbols

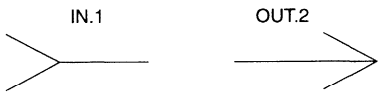
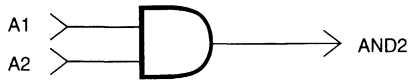


Figure 4. Design Example using IN.1 and OUT.1 Symbols

Schematic



ABEL™ Source File

```
AND2, A2, A1 pin;
AND2 istype 'com';
Equations
AND2 = A1 & A2;
```

Setting your Input Signal to a Constant Logic Level

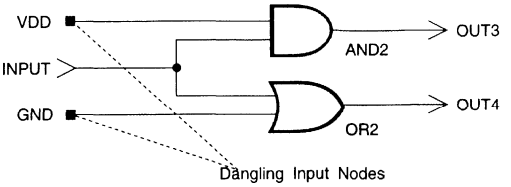
There are two methods which you can use to set your input signals to a constant logic level:

Method 1. Label your input nodes using the VDD and GND labels (see Figure 5).

Method 2. Use the PWR.1 and GND.1 symbols from the DIO library (see Figure 6).

Figure 5. Design Example using VDD and GND Labels[2]

Schematic

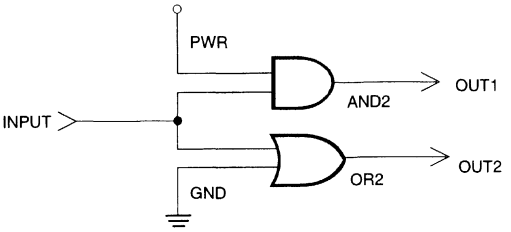


ABEL™ Source File

```
OUT3,OUT4,INPUT pin;
OUT3,OUT4 istype 'com';
Equations
OUT3 = 1 & INPUT;
OUT4 = 0 # INPUT;
```

Figure 6. Design Example using PWR.1 and GND.1 DIO Symbols

Schematic



ABEL™ Source File

```
OUT2,OUT1,INPUT pin;
OUT2,OUT1 istype 'com';
Equations
OUT2 = INPUT # 0;
OUT1 = 1 & INPUT;
```

Notes:

1. Please refer to the next section when you are asssigning the VDD and GND labels to the IN.1 and OUT.1 symbols.
2. Do not use the IN.1 and OUT.1 symbols when using the VDD and GND labels to create a constant logic level. If you use these input and output symbols, then the external pins with labels "VDD" and "GND" will be generated.

Applying the D_LATCH.1 and IN_LATCH.1 Symbols for the ATV5000 or ATV5100 Device

The D_LATCH.1 symbol can be used in a design for latching internal or external signals. This symbol uses a D-type flip-flop with asynchronous preset and reset controls to emulate the latch function (the logic equations are specified in the functional library files; refer to "The DIO and DSTD Symbols" section for more information). This symbol can be used as an output or buried latch. The data flows through when $\overline{G}$ is HIGH. Once $\overline{G}$ goes LOW, the data is latched (see Figure 7).

The IN_LATCH.1 symbol is only used for latching inputs in the ATV5000 or ATV5100 design. Unlike the D_LATCH.1 symbol, this symbol is implemented in the ATV5000 or ATV5100 using a real latch circuitry in each I/O pin. The data flows through when C is LOW, and data is captured on the rising edge of the C signal (see Figure 8).

What to Do with the Unused Pins of a DSTD Symbol[1]

For DSTD symbols consisting of combinatorial logic such as the DSTD155 or DSTD156, the unused pins can be left unconnected. The unused logic will be automatically removed from the ABEL™ source file as illustrated by Design Example 1 in Figure 9.

On the other hand, careful attention must be paid to the unused pins if the symbols have registered or latched logic. With symbols that have registered or latched logic, pins and nodes are automatically assigned to the unused inputs and outputs respectively. With the limited number of pins and nodes in the most devices, the assigned pins and nodes may prevent your final design from fitting into the selected device. Design Example 2 in Figure 10 illustrates the problem in which three pins and nodes are unnecessarily created.

In Design Example 2 (Figure 10), a total of three unnecessary pins were assigned and three unnecessary nodes generated.

To eliminate all the unnecessary assigned pins, we recommend grounding the unused inputs. To reduce the unnecessary assigned nodes to a single node, all the unused outputs of the symbol should be connected together to form a single node with an easily identifiable label such as NC or DUMMY. With these modifications implemented, instead of three pins and three nodes wasted as illustrated in Design Example 2, the efficiency of your design improved with:

- no additional pins generated, and
- only one additional node created. Usually this single node would not inhibit the design from fitting into the selected device. But if it does, then it can be manually deleted off the ABEL™ source file.

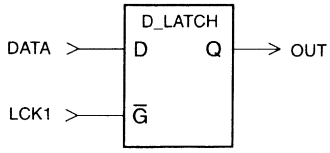
In Design Example 3 (Figure 11), only one node (i.e., node NC1) was created and no additional input pins assigned.

Note:
1. This restriction for the unused pins of the DSTD symbols will be eliminated in the future versions of the Atmel-ViewPLD development tool.

6

Figure 7. Design Example using D_LATCH.1 DIO Symbol

Schematic

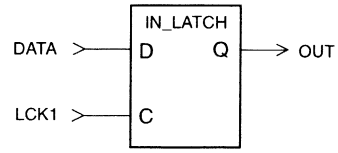


ABEL™ Source File

```
OUT1,LCK1,DATA pin;
OUT istype 'buffer,reg_d';
Equations
OUT.D = 1
OUT.AP = (LCK1 & DATA);
OUT.AR = (LCK1 & !DATA);
OUT.C = 1;
```

Figure 8. Design Example using IN_LATCH.1 DIO Symbol

Schematic

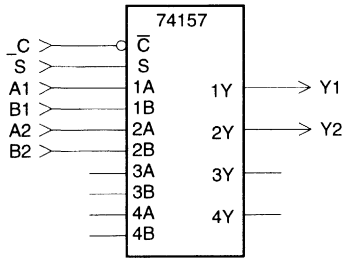


ABEL™ Source File

```
OUT,LCK1,DATA pin;
OUT istype 'buffer,reg_d';
Equations
OUT.D = DATA;
OUT.LE = LCK1;
```

Figure 9. Design Example 1, A DSTD Symbol with Combinatorial Logic in which the unused pins are left unconnected.

Schematic

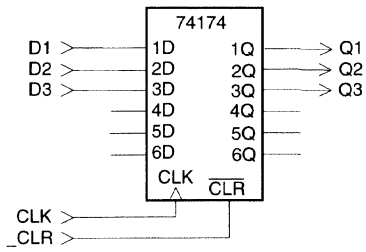


ABEL™ Source File

```
_C,Y2,Y1,S,B2,B1,A2,A1 pin ;
Y1    istype    'com';
Y2    istype    'com';
Equations
Y1 = !((!(A1 & !S) & !(B1 & S)) # _C);
Y2 = !((!(A2 & !S) & !(B2 & S)) # _C);
```

Figure 10. Design Example 2, A DSTD Symbol with Registered Logic in which the unused pins are left unconnected generated.

Schematic

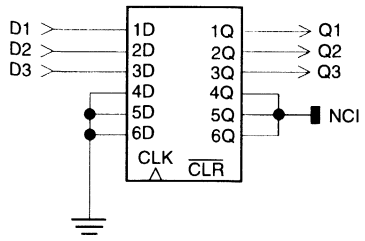


ABEL™ Source File

```
S10,S7,S4 pin ; "Unused inputs
S3,S6,S9 node ; "Unused outputs
_CLR, Q3, Q2, Q1, D3, D2, D1, CLK pin ;
S9,S6,S3 istype 'buffer, reg, reg_d';
Q3,Q2,Q1 istype 'buffer, reg, reg_d';
Equations
"Unnecessary logic equations
S9.d = S10;
S9.ar = (!(_CLR)) ;
S9.c = CLK ;
S6.d = S7;
S6.ar = (!(_CLR)) ;
S6.c = CLK ;
S3.d = S4;
S3.ar = (!(_CLR)) ;
S3.c = CLK ;
"Actual logic equations in use
Q2.d = D2;
Q2.ar = (!(_CLR)) ;
Q2.c = CLK ;
Q3.d = D3;
Q3.ar = (!(_CLR)) ;
Q3.c = CLK ;
Q1.d = D1;
Q1.ar = (!(_CLR)) ;
Q1.c = CLK ;
```

Figure 11. Design Example 3, A DSTD Symbol with Registered Logic (same as in Design Example 2), but with the unused inputs grounded and unused outputs connected together to form a single node.

Schematic



ABEL™ Source File

```
NC1 node ; "Unused node
_CLR,Q3,Q2,Q1,D3,D2,D1,CLK pin ;
NC1   istype   'buffer, reg, reg_d';
Q2    istype   'buffer, reg, reg_d';
Q3    istype   'buffer, reg, reg_d';
Q1    istype   'buffer, reg, reg_d';
Equations
"Unused logic equations
NC1.d = 0;
NC1.ar = (!(_CLR)) ;
NC1.c = CLK ;
"Actual logic equations in use
Q2.d = D2;
Q2.ar = (!(_CLR)) ;
Q2.c = CLK ;
Q3.d = D3;
Q3.ar = (!(_CLR)) ;
Q3.c = CLK ;
Q1.d = D1;
Q1.ar = (!(_CLR)) ;
Q1.c = CLK ;
```

Creating a Viewdraw Schematic from an ABEL™ or a JEDEC File

One of the valuable features of the Atmel-ViewPLD development tool is the ability to generate a Viewdraw schematic from an ABEL™ or a JEDEC file. With this feature, you can use both the schematic capture and ABEL HDL design entries in the same design. In addition, old designs which consist of PLDs or TTL devices that are already in production can easily be integrated into a single design so that it can be compiled to fit into a single PLD like the Atmel ATV5000 or ATV5100 device.

The command for generating a Viewdraw schematic from an ABEL™ or a JEDEC file is the "Window Open ViewPLD Model_Device Schematic" menu command. Once this command is executed, the dialog box shown in Figure 12 will open. After selecting your options, click the middle button of the mouse to begin executing the command.

Use the left button of the mouse to select the options or to enter the project name which is the ABEL™ or JEDEC filename. Note that you must not enter the file extension (.ABL or .JED) when entering the project name.

Figure 13 shows the process flow for generating a schematic from an ABEL™ file or a JEDEC file.

Figure 12. Dialog Box for Modelling an ABEL™, JEDEC, or PLA File to Create a Viewdraw Schematic

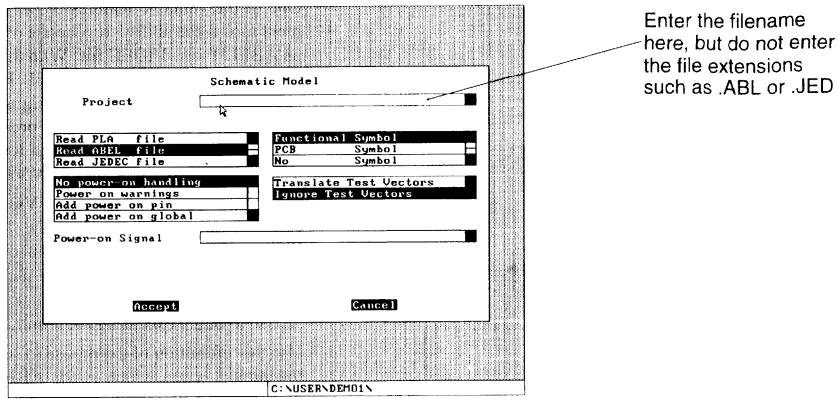
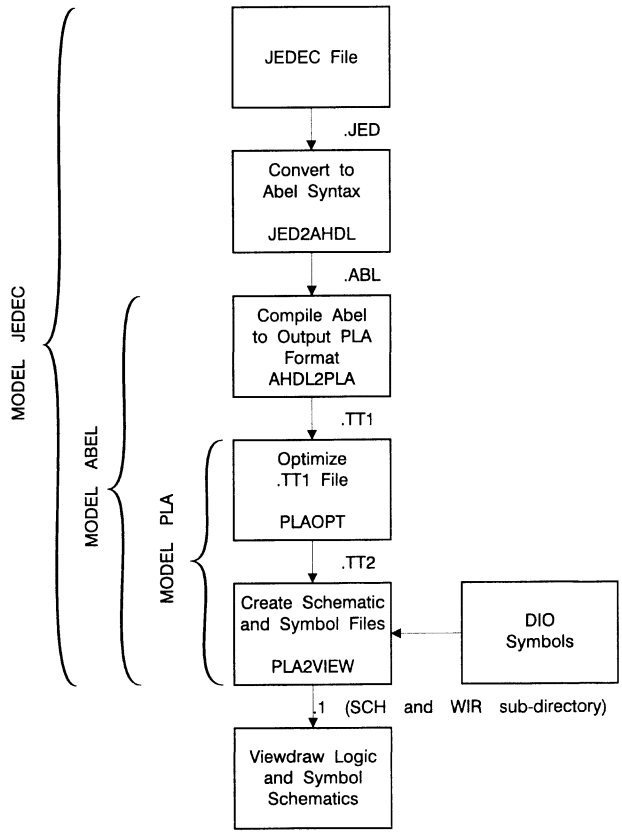


Figure 13. Process Flow for Modelling a Viewdraw Schematic



Simulating Your Design Using Worst-Case Timing Values

After you have created a JEDEC file for your design, you can further verify your design by simulating your design using the worst-case timing values of the selected device. Simulating your design using worst-case timing values provides significant benefits such as predicting the performance of your design, providing information on timing violations, and etc.

Prior to creating a timing model, you must first run the menu command "Window Open ViewPLD Search_TimBase." This command will extract the timing data of the selected device from the global timing database and store them locally in the .TIM file (same filename as your design file but with extension .TIM). Note that the ASCII timing data in the .TIM file can be modified by the users if the new timing data for a new speed version device is available from Atmel.

After creating the local timing database, execute the "Window Open ViewPLD Model_Device Timing_Model" menu command to open the JEDEC Modeller dialog box as shown in Figure 14. Select your options and click the middle button of the mouse to start executing the command (see Figure 15).

Figure 14. JEDEC Modeller Dialog Box for Creating a Timing Model with Worst-Case Timing Values

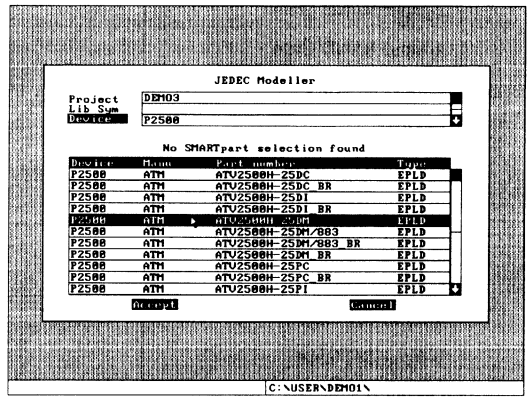
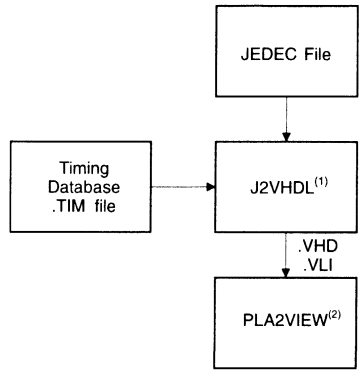


Figure 15. Process Flow for Creating a Timing Model



Notes:
1. Converts the JEDEC file to a timing model in VHDL format. The VHDL Analyzer is then executed to convert the VHDL model to a VLI model which can be read by Viewsim.
2. Creates a symbol schematic of the modelled device, i.e., only used pins will be generated.

Table 2. Atmel-ViewPLD/ProPLD DIO and DSTD Primitive Symbols

Primitive	Device Supported	Description
Basic Gates		
AND2	All	2-Input AND Gate
AND4	All	4-Input AND Gate
AND8	All	8-Input AND Gate
BUF	All	Buffer
GND	All	Ground
IN	All	Input Pin
NAND2	All	2-Input NAND Gate
NAND4	All	4-Input NAND Gate
NAND8	All	8-Input NAND Gate
NOT	All	Inverter
NOR2	All	2-Input NOR Gate
NOR4	All	4-Input NOR Gate
NOR8	All	8-Input NOR Gate
OR2	All	2-Input OR Gate
OR4	All	4-Input OR Gate
OR8	All	8-Input OR Gate
OUT	All	Output Pin
PWR	All	Power
TRST	All	Tri-State Buffer, Output Enabled on High
TRIBUF	—	Viewlogic Built-in Primitive – DO NOT USE IN SCHEMATIC. Refer to Appendix A of the Viewsim/SD Reference Guide.
XNOR2	All	Exclusive NOR Gate
XOR2	All	Exclusive OR Gate
Block (Sheet) Size		
ASHEET.1	All	8.5" X 11"
ASHEET.2	All	11" X 8.5"
BSHEET	All	17" X 11"
CSHEET.1	All	17" X 22"
CSHEET.2	All	22" X 17"
DSHEET	All	34" X 22"
ESHEET.1	All	34" X 44"
ESHEET.2	All	44" X 34"

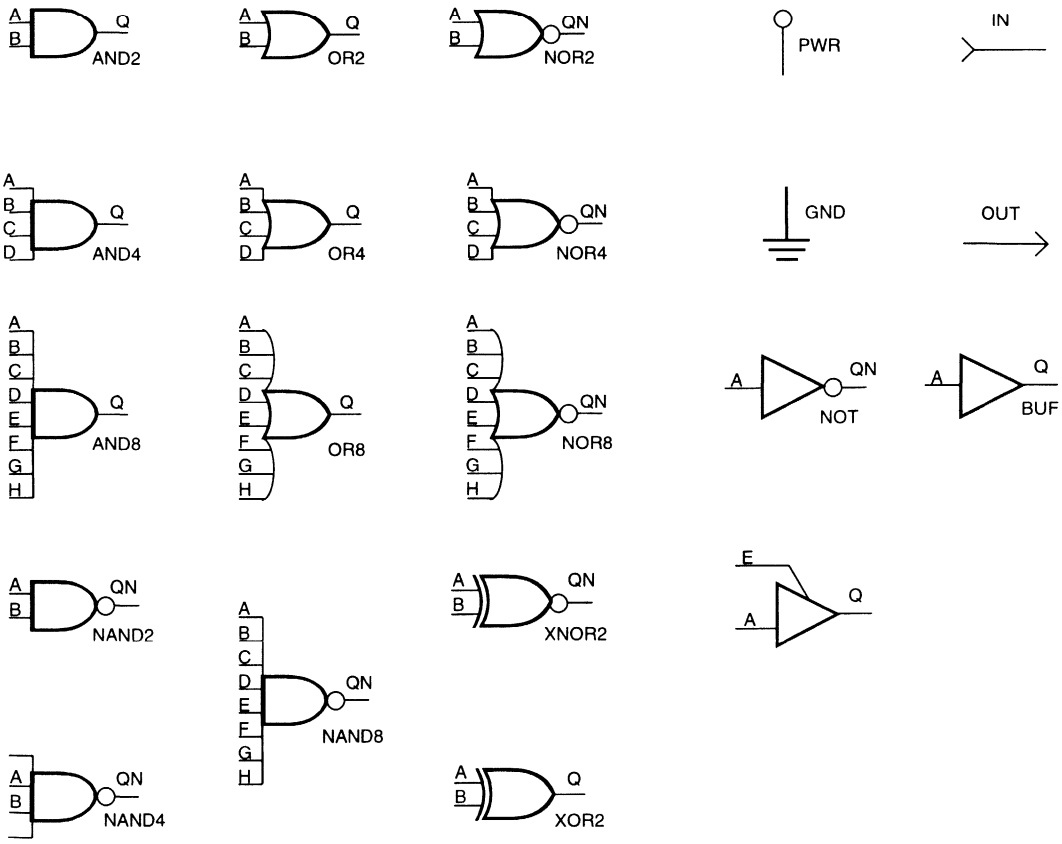
Table 2. Atmel-ViewPLD/ProPLD DIO and DSTD Primitive Symbols (continued)

Primitive	Device Supported	Description
Generic Device Symbol (For Design Partitioning)		
ANY_20		20-Pin Generic Device
ANY_24		24-Pin Generic Device
ANY_28		28-Pin Generic Device
ANY_40		40-Pin Generic Device
ANY_44		44-Pin Generic Device
ANY_68		68-Pin Generic Device
Latches		
DLATCH	ATV5000 ATV5100	Standard D Latch with Data Flow-Through when G Input is High. Data is latched when G goes LOW. This latch can be used as a buried latch.
IN_LATCH	ATV5000 ATV5100	Input D Latch. The data flow-through occurs when the C input is LOW. Data is latched on the rising edge of C.
RSLATCH	All	RS Latch. In ATV750 and ATV2500 devices, the RS latch is emulated via two cross-coupled NAND gates. In the ATV5000 devices, a flip-flop with asynchronous preset and reset is used.
RS_FF	All	RS Flip-Flop. A D flip-flop is used to emulate the RS flip-flop.
Flip-flops		
DFF	All	D Flip-Flop with no Preset or Reset Function. Flip-flop is reset upon device power-up.
DFFC	All	D Flip-Flop with Asynchronous Reset
DFFP	ATV5000 ATV5100	D Flip-Flop with Asynchronous Preset
DFFPC	ATV5000 ATV5100	D Flip-Flop with Asynchronous Preset and Reset
DFFSP	All	D Flip-Flop with Synchronous Preset
DFFSPC	All	D Flip-Flop with Synchronous Preset and Ssynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops. In the ATV5000/ATV5100 devices, the preset term can be independently controlled.
JKFF	All	JK Flip-Flop with no Preset or Reset
JKFFC	All	JK Flip-Flop with Asynchronous Reset
JKFFP	ATV5000 ATV5100	JK Flip-Flop with Asynchronous Preset
JKFFPC	ATV5000 ATV5100	JK Flip-Flop with Asynchronous Preset and Reset
JFFSP	All	JK Flip-Flop with Synchronous Preset

Table 2. Atmel-ViewPLD/ProPLD DIO and DSTD Primitive Symbols (continued)

Primitive	Device Supported	Description
JKFFSPC	All	JK Flip-Flop with Synchronous Preset and Asynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops. In the ATV5000/ATV5100 devices, the preset term can be independently controlled.
TFF	All	T Flip-Flop with no Preset or Reset
TFFC	All	T Flip-Flop with Asynchronous Reset
TFFP	ATV5000 ATV5100	T Flip-Flop with Asynchronous Preset
TFFPC	ATV5000 ATV5100	T Flip-Flop with Asynchronous Preset and Reset
TFFSP	ATV750/B ATV2500/B	T Flip-Flop with Synchronous Preset
TFFSPC	ATV750/B ATV2500/B	T Flip-Flop with Synchronous Preset and Asynchronous Reset. In the ATV750 and ATV2500 devices, the synchronous preset is a global preset product term, i.e., a single product term presets a group of flip-flops.
UDFDL	—	Viewlogic Built-In Primitive – DO NOT USE IN SCHEMATIC

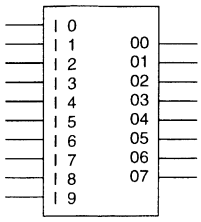
Atmel's DIO Primitives, Sheet 1 of 4



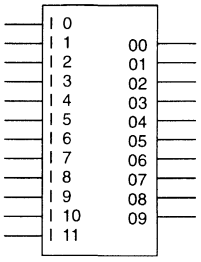
6

Atmel's DIO Primitives, Sheet 2 of 4

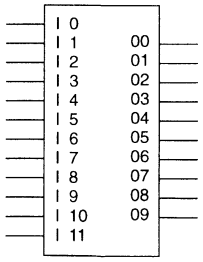
ANY _ 20



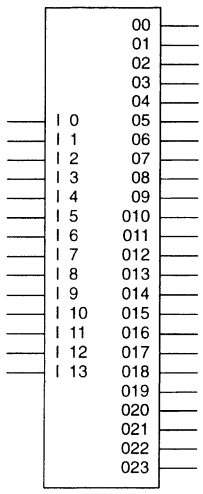
ANY _ 24



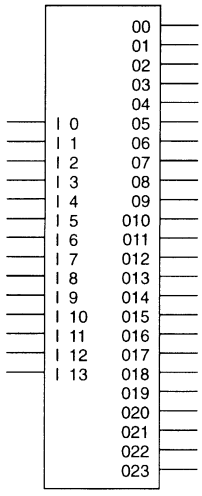
ANY _ 28



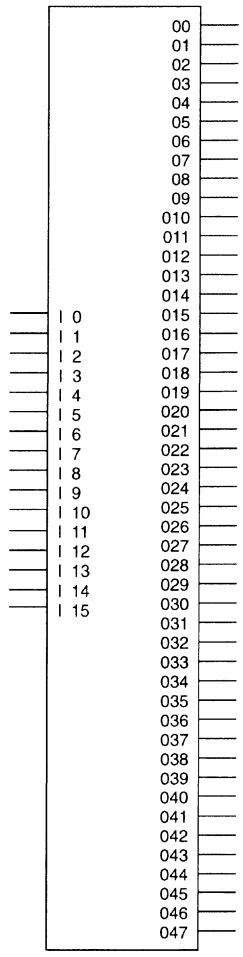
ANY _ 40



ANY _ 44



ANY _ 68



ASHEET . 1
8.5 X 11"

ASHEET . 2
11 X 8.5"

BSHEET . 1
17 X 11"

CSHEET . 1
17 X 22"

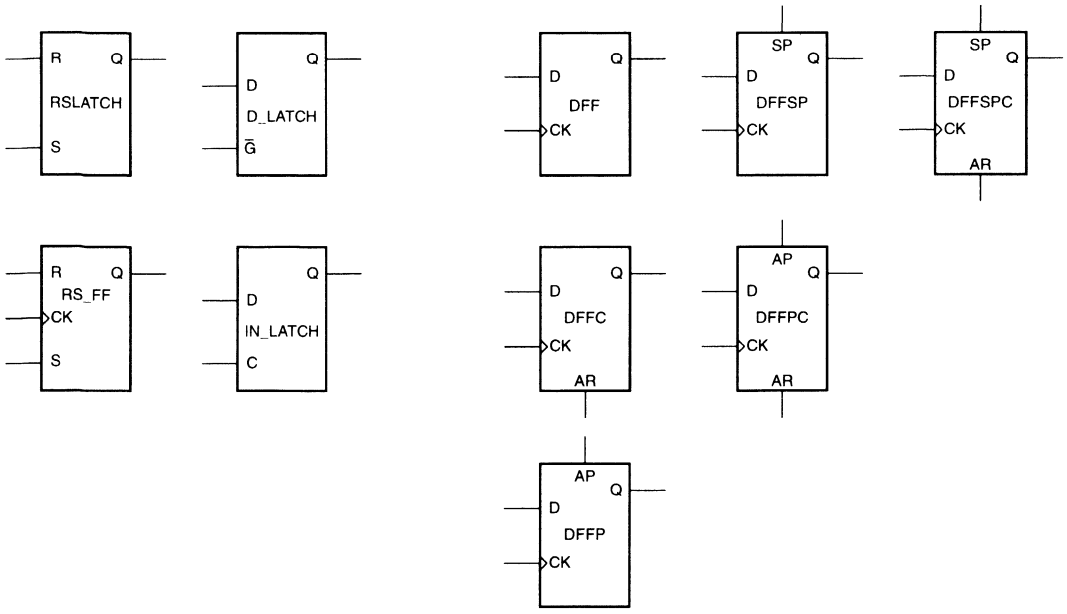
CSHEET . 2
22 X 17"

DSHEET . 1
34 X 22"

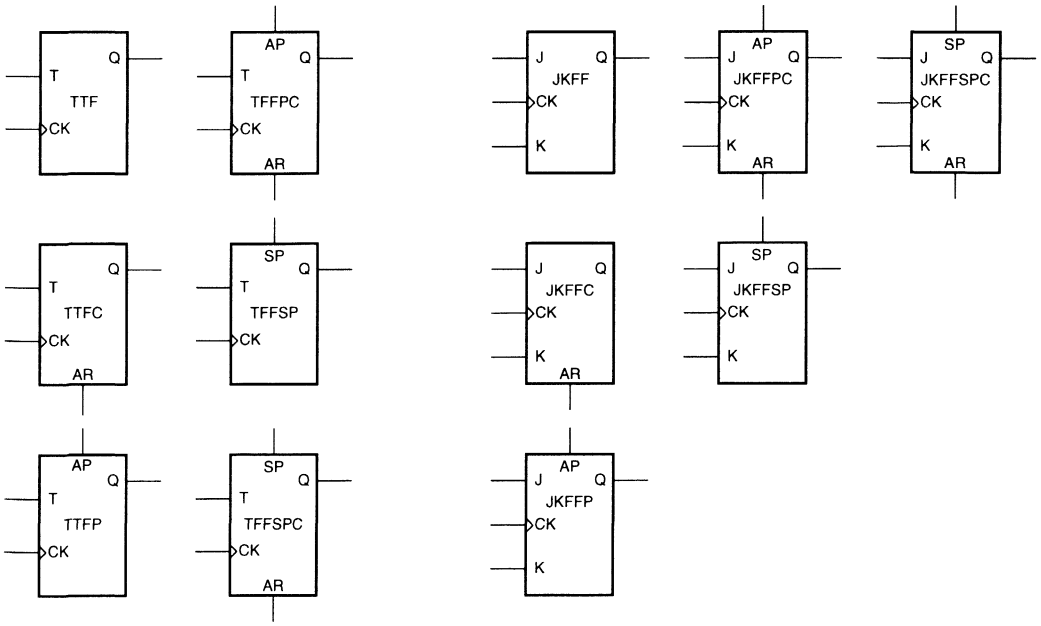
ESHEET . 1
34 X 44"

ESHEET . 2
44 X 34"

Atmel's DIO Primitives, Sheet 3 of 4



Atmel's DIO Primitives, Sheet 4 of 4



6

Table 3. DSTD TTL Symbols

Component	Device Supported	Function Description
DSTD00	All	2-Input NAND Gate
DSTD02	All	2-Input NOR Gate
DSTD04	All	Inverter
DSTD08	All	2-Input AND Gate
DSTD10	All	3-Input NAND Gate
DSTD107	All	JK Flip-Flop with Async. Clear
DSTD109	All	JK Flip-Flop with Async. Preset and Clear
DSTD11	All	3-Input AND Gate
DSTD112	ATV5000 ATV5100	JK Flip-Flop (Negative-Edge Triggered) with Async. Preset and Clear
DSTD113	ATV5000 ATV5100	JK Flip-Flop (Negative-Edge Triggered) with Async. Preset
DSTD114	ATV5000 ATV5100	Dual JK Flip-Flops (Negative-Edge Triggered) with Async. Preset, Common Clear, and Common Clock
DSTD125	All	Tri-State Buffer with LOW to OE
DSTD126	All	Tri-State Buffer with HIGH to OE
DSTD128	All	2-Input NOR Gate
DSTD133	All	13-Input NAND Gate
DSTD134	All	12-Input NAND Gate with LOW to Output Enable Tri-State Buffer
DSTD135	All	Quad Exclusive-OR/NOR Gates
DSTD137	ATV5000 ATV5100	3-to-8 Line Decoder with Address Latches
DSTD138	All	3-to-8 Line Decoder
DSTD139	All	2-to-4 Line Decoder
DSTD140	All	4-Input NAND Gate
DSTD147	All	10-to-4 Line Priority Encoder
DSTD148	All	8-to-3 Line Priority Encoder
DSTD150	All	1-of-16 Line Data Selector/Multiplexer
DSTD151	All	1-of-8 Line Data Selector/Multiplexer with Compl. Output
DSTD152	All	1-of-8 Line Data Selector/Multiplexer
DSTD153	All	Dual 4-to-1 Line Data Selector/Multiplexers
DSTD154	All	4-to-16 Line Decoder
DSTD155	All	Dual 2-to-4 Line Decoders
DSTD157	All	Quad 2-to-1 Line Data Selector/Multiplexers
DSTD158	All	Quad 2-to-1 Line Data Selector/Multiplexers with Compl. Output

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD160	All	Sync. 4-Bit Decade Counter with Async. Clear
DSTD161	All	Sync. 4-Bit Binary Counter with Async. Clear
DSTD162	All	Sync. 4-Bit Decade Counter with Sync. Clear
DSTD163	All	Sync. 4-Bit Binary Counter with Sync. Clear
DSTD164	ATV5000 ATV5100	8-Bit Serial In/Parallel Out Shift Register with Async. Clear
DSTD165	ATV5000 ATV5100	8-Bit Parallel In/Serial Out Shift Register with Compl. Output
DSTD168	All	Synchronous 4-Bit Up/Down Decade Counter
DSTD169	All	Synchronous 4-Bit Up/Down Binary Counter
DSTD174	All	Hex D Flip-Flops with Async. Clear
DSTD175	All	Quad D Flip-Flops with Async. Clear and Compl. Output
DSTD176	ATV5000 ATV5100	4-Bit Presetable Decade Counter
DSTD177	ATV5000 ATV5100	4-Bit Presetable Binary Counter
DSTD180	All	9-Bit Parity Generator/Checker
DSTD181	ATV5000 ATV5100	Arithmetic Logic Unit/Function Generator
DSTD182	All	Look-Ahead Carry Generator
DSTD183	All	Carry-Save Full Address
DSTD190	ATV5000 ATV5100	Sync. 4-Bit Up/Down Decade Counter with Mode Control
DSTD191	ATV5000 ATV5100	Synchronous 4-Bit Up/Down Binary Counter with Mode Control
DSTD192	ATV5000 ATV5100	Synchronous 4-Bit Up/Down Decade Counter with Dual Clock
DSTD194	All	4-Bit Bidirectional Universal Shift Register
DSTD196	ATV5000 ATV5100	4-Bit Presettable Decade Counter
DSTD197	ATV5000 ATV5100	4-Bit Presettable Binary Counter
DSTD198	All	8-Bit Bidirectional Universal Shift Register
DSTD20	All	4-Input NAND Gate
DSTD21	All	4-Input AND Gate
DSTD226	ATV5000 ATV5100	4-Bit Parallel Latched Bus Tranceivers

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD23	All	Dual 4-Input NOR Gates with Strobe
DSTD237	All	3-to-8 Line Decoder with Address Latches
DSTD240	All	Quad Tri-State Inverting Buffers
DSTD241	All	Octal Tri-State Buffers
DSTD242	All	Quad Tri-State Inverting Bus Transceivers
DSTD243	All	Quad Tri-State Bus Transceivers
DSTD244	All	Octal Tri-State Buffers
DSTD245	All	Octal Tri-State Bus Transceivers
DSTD25	All	4-Input NOR Gate with Strobe
DSTD251	All	Tri-State 1-to-8 Line Data Selector/Multiplexer with Compl. Output
DSTD253	All	Dual Tri-State 1-to-4 Multiplexers
DSTD257	All	Quad Tri-State 2-to-1 Multiplexers
DSTD258	All	Quad Tri-State 2-to-1 Inverting Multiplexers
DSTD260	All	5-Input NOR Gate
DSTD27	All	3-Input NOR Gate
DSTD273	All	Octal D Flip-Flops with Clear and Buffer Outputs
DSTD279	All	Dual SR Latches
DSTD28	All	2-Input NOR Buffer
DSTD280	All	9-Bit Odd/Even Parity Generators/Checkers
DSTD283	All	4-Bit Binary Full Adders with Fast Carry
DSTD290	All	Decade Counter
DSTD293	All	4-Bit Binary Counter
DSTD295	All	4-Bit Right/Left Shift Registers with Tri-State Outputs
DSTD298	All	Quad 2-Input Multiplexers with Storage
DSTD299	All	8-Bit Universal Shift/Storage Registers
DSTD30	All	8-Input NAND Gate
DSTD31	All	Delay Elements
DSTD32	All	2-Input OR Gate
DSTD323	All	8-Bit Universal Shift/Storage Registers
DSTD348	All	8-to-3 Line Priority Encoders with Tri-State Outputs
DSTD353	All	Dual 4-to-1 Line Data Selectors/Multiplexers with Tri-State Outputs
DSTD354	ATV5000 ATV5100	8-to-1 Multiplexer/Register (Transparent)

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD356	All	8-to-1 Multiplexer/Register (Edge-Triggered)
DSTD365	All	Hex Bus Drivers with Tri-State Outputs
DSTD366	All	Hex Inverting Bus Drivers with Tri-State Outputs
DSTD367	All	Hex Bus Drivers with Tri-State Outputs with Two Tri-State Controls
DSTD368	All	Hex Inverting Bus Drivers with Tri-State Outputs with Two Tri-State Controls
DSTD37	All	2-Input NAND Buffers
DSTD373	ATV5000 ATV5100	Octal Transparent D Latches
DSTD374	All	Octal Edge-Triggered D Flip-Flops
DSTD376	All	Quad JK Flip-Flops
DSTD377	All	Octal D Flip-Flops with Enable
DSTD378	All	Hex D Flip-Flops with Enable
DSTD379	All	Quad D Flip-Flops with Enable
DSTD390	All	4-Bit Decade Counter
DSTD393	All	4-Bit Binary Counter
DSTD398	All	Quad 2-Input Multiplexer with Storage
DSTD399	All	Quad 2-Input Multiplexer with Storage
DSTD40	All	4-Input NAND Buffers
DSTD4002	All	4-Input NOR Gate
DSTD4016	All	Bilateral Switch
DSTD4017	All	Decade Counter/Divider
DSTD4020	All	14-Stage Ripple-Carry Binary Counter/Divider
DSTD4024	All	7-Stage Ripple-Carry Binary Counter/Divider
DSTD4040	All	12-Stage Ripple-Carry Binary Counter/Divider
DSTD4049	All	Inverting Buffer
DSTD4066	All	Bilateral Switch
DSTD4075	All	3-Input OR Gate
DSTD4078	All	8-Input NOR Gate with Compl. Output
DSTD42	All	BCD to Decimal Decoder
DSTD4514	ATV5000 ATV5100	8-Bit Static Shift Register
DSTD51	All	Dual 2-Wide 2-Input AND-OR-INVERT Gates
DSTD520	All	Octal 8-Bit Identity Comparator

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD521	All	Octal 8-Bit Identity Comparator
DSTD533	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD534	All	Octal Tri-State Inverting Edge-Triggered D Flip-flops
DSTD538	All	3-to-8 Line Decoders with Tri-State Outputs
DSTD54	All	4-Wide 2-Input AND-OR-INVERT Gates
DSTD540	All	Octal Buffers with Tri-State Outputs
DSTD541	All	Octal Inverting Buffers with Tri-State Outputs
DSTD55	All	2-Wide 4-Input AND-OR-INVERT Gates
DSTD563	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD564	All	Octal Tri-State Inverting Edge-Triggered D Flip-Flops
DSTD568	All	Synchronous 4-Bit Up/Down Decade Counter with Tri-State Outputs
DSTD569	All	Synchronous 4-Bit Up/Down Binary Counter with Tri-State Outputs
DSTD573	ATV5000 ATV5100	Octal Tri-State Transparent D Latches
DSTD574	All	Octal Tri-State Edge-Triggered D Flip-Flops
DSTD575	All	Octal Tri-State Edge-Triggered D Flip-Flops with Sync. Clear
DSTD576	All	Octal Tri-State Inverting Edge-Triggered D Flip-Flops
DSTD580	ATV5000 ATV5100	Octal Tri-State Inverting Transparent D Latches
DSTD623	All	Octal Tri-State Bus Transceivers
DSTD638	All	Octal Inverting Bus Transceivers with Tri-State and Open-Collector Outputs
DSTD64	All	4-2-3-2-Input AND-OR-INVERT Gates
DSTD640	All	Octal Tri-State Inverting Bus Transceivers
DSTD643	All	Octal Tri-State True and Inverting Bus Transceivers
DSTD645	All	Octal Tri-State Bus Transceivers
DSTD646	All	Octal Bus Transceivers and Registers with AllTri-State Outputs
DSTD652	All	Octal Bus Transceivers and Registers
DSTD668	All	Synchronous 4-Bit Up/Down Decade Counters
DSTD669	All	Synchronous 4-Bit Up/Down Binary Counters
DSTD670	ATV5000 ATV5100	4-by-4 Register Files with Tri-State Outputs
DSTD677	All	16-to-4 Bit Address Comparator with Enable
DSTD684	All	8-Bit Magnitude/Identity Comparator

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD688	All	8-Bit Identity Comparator
DSTD70	ATV5000 ATV5100	AND-Gated Edge-Triggered JK Flip-Flop with Async. Preset and Clear
DSTD73	ATV5000 ATV5100	JK Flip-Flop with Async. Clear
DSTD74	ATV5000 ATV5100	D Flip-Flop (Edge-Triggered) with Async. Preset and Clear
DSTD75	ATV5000 ATV5100	4-Bit Bistable Latches
DSTD76	ATV5000 ATV5100	JK Flip-Flop with Async. Preset and Clear
DSTD77	ATV5000 ATV5100	Dual Transparent D Latches
DSTD78	ATV5000 ATV5100	Dual JK Flip-Flops (Edge-Triggered) with Async. Preset, Common Clear, and Common Clock
DSTD80	All	Gated Full Adders
DSTD804	All	2-Input NAND Line Driver
DSTD805	All	2-Input NOR Line Driver
DSTD808	All	2-Input AND Line Driver
DSTD82	All	2-Bit Binary Full Adders
DSTD83	All	4-Bit Binary Full Adders with Fast Carry
DSTD832	All	2-Input OR Line Driver
DSTD85	All	4-Bit Magnitude Comparators
DSTD857	All	Hex 2-to-1 Universal Multiplexers
DSTD86	All	2-Input Exclusive-OR Gate
DSTD867	All	Synchronous 8-Bit Up/Down Counter with Async. Clear
DSTD869	All	Synchronous 8-Bit Up/Down Counter with Sync. Clear
DSTD874	All	4-Bit Edge-Triggered D Flip-Flop
DSTD878	All	4-Bit Edge-Triggered D Flip-Flop with Tri-State Outputs
DSTD882	All	32-Bit Look-Ahead Carry Generators
DSTD90	All	Decade Counter
DSTD91	All	8-Bit Shift Registers
DSTD92	All	Divide-by-12 Counter
DSTD93	All	4-Bit Binary Counter
DSTD94	ATV5000 ATV5100	4-Bit Shift Registers

Table 3. DSTD TTL Symbols (continued)

Component	Device Supported	Function Description
DSTD96	ATV5000 ATV5100	5-Bit Shift Registers
DSTDK	All	2-Input NAND Gate
DSTDK2	All	2-Input NOR Gate
DSTDK4	All	Inverter
DSTDK8	All	2-Input AND Gate
DSTD34	All	Buffer
DSTDK34	All	Buffer

Glossary

Term	Description
Async.	Asynchronous
Sync.	Synchronous
Compl.	Complementary

Using the ATV5000/ATV5100 Atmel-ABEL™ Fitter

Introduction

The ATV5000/ATV5100 Atmel-ABEL Fitter is an automatic pin and node assignment program specifically written for ATV5000/ATV5100 designs implemented in the ABEL Hardware Design Language (ABEL HDL). The fitter utilizes the ATV5000 or ATV5100 device architecture resources to perform partial or complete pin and node signal assignments. For many designs, the fitter automatically assigns the pins and nodes efficiently without any manipulations by the designer. However, for very complex designs, some "steering" by the designer may be necessary in order to achieve high efficiency and performance.

This application note offers some hints that enable the ATV5000/ATV5100 fitter to achieve a higher design efficiency and performance. To maximize your understanding of these hints, you should read the Atmel ATV5000/ATV5100 Device Fitter manual. This manual contains a brief overview of the ATV5000 and ATV5100 architectures, the fitting process and fitter command options.

Interpreting the Fitter Log File (.FIT)

The ATV5000/ATV5100 fitter writes the pin and node assignments, device utilization, and any fitting errors the fitter encountered to the log file with the file extension `.FIT`. This fitter log file can be accessed via the `Fitter Assignments` command in the `View` menu window in the ABEL Design Environment. Figure 1 shows an example of a fitter log file.

```
 Atmel P5000/P5100 fitter run on  4-Feb-94 10:25 AM.
============================================================
Warnings
============================================================
Fitting Device P5000.
Fitter mode=KEEP
Converting cluster toggle pin feedback to registered feedback.
============================================================
 The Design Fits.
============================================================
Overall Summary.

  Type                    UsedFreeUtilization
 ----------
Cell Usage
   Macrocells             2.25 72.75 4.3% (1.00 Wasted)
Pins Usage
   Inputs                 0 8 0.0%
   Outputs                ----N/A
   IO                     646 11.5%
   Summary                65410.0%
============================================
 Chip assignments summary.
Quadrant(1).
  toggle on 761
```

Figure 1. The `UR_RU.FIT` file for the ATV500 device (`KEEP` fitter option) *(continues)*

0318B

```
   RESET on 5
   clock_pin on 6
   input_pin on 7
   tog1 on 8
   toggle_RU_2 on 69
Quadrant(2).
   tog2 on 134
   toggle_UR_1 on 179
   tog3 on 18
Quadrant(3).
Quadrant(4).
=========================================
  Quadrant by Quadrant Macrocell Usage.
.
.
.Node 196 (Buried_node) -> <none>
   (has_A has_upper_reg )
=========================================
$DEVICE P5000 fit ur_ru.tt3
$PINS 4 clock_pin:6 input_pin:5 tog1:7 tog3:18
$NODES 3 toggle:122 tog2:123 toggle_RU_1:72
```

Figure 1. *(continued)* The `UR_RU.FIT` file for the ATV500 device (`KEEP` fitter option)

When reviewing the fitter log file, you should pay special attention to the Chip Assignments Summary because it contains the information on how the fitter implemented the pin and node assignments. In addition to the pin and node assignments, the fitter may generate additional combinatorial nodes to route regional signals from one quadrant to another. The additional nodes generated contain suffixes such as `_UR_n`, `_RU_n`, and `_n`, where `n` is the total number of occurrences of the nodes.

Suffix	Description
`_UR_n`	Universal-to-Regional (UR) converters. These converters are used to convert the universal signals to regional signals. These conversions are sometimes necessary because of the limited number of universal product terms. Only the Buried Cells can be used for the UR conversion. This means that you can have up to a maximum of six UR converters in a quadrant of the ATV5000 or ATV5100 device.
`_RU_n`	Regional-to-Universal (RU) converters. These converters are used to route regional signals to other quadrants. The sum-term-feedbacks or B Nodes (nodes 69 to 120) are used for the RU conversion. Since the sum-term-feedback shares the same feedback path as the I/O pin, the sum-term-feedback is only available if the I/O pin is not used as an input, bidirectional I/O, combinatorial output, or a registered output with more than four product terms (or more than one universal product term for the ATV5000 device and two universal product terms for the ATV5100 device).
`_n`	These combinatorial nodes function similarly to the UR converters. They are generated for the ATV5100 regional control terms such as the Asynchronous Reset (AR) and Asynchronous Preset (AP) terms of the registers in the macrocells, and the Output Enable (OE) terms in the I/O cells. Like the UR converters, only the Buried Cells can be used for converting the universal signals to regional signals.

1. Universal signals are signals originating from the Universal Bus. Universal signals include signals from the I/O pins or sum-term-feedbacks (combinatorial nodes 69 to 120).
2. Regional signals are signals originating from the Regional Bus of quadrants 1, 2, 3, and 4. Regional signals include signals from the eight dedicated Clock/Latch Enable pins (also can be used as inputs), the buried Q1 and Q2 registers, and the Buried Cells.
3. Universal product terms are the product terms that are connected to both the Universal and Regional Buses.
4. Regional product terms are the product terms that are connected only to the Regional Bus in a quadrant.

```
"Inputs
RESET     pin 5;          "Reset for everybody
clock_pin  pin 6;         "Clock for everybody

"Quadrant 1
toggle                    node 761  istype 'reg_t,buffer';   "A_node of pin 4
input_pin  pin 7          "Input to Universal bus
tog1                      pin 8istype 'reg_t,buffer';

"Quadrant 2
tog2                      node 134istype 'reg_t,buffer';
tog3                      pin 18istype 'reg_t,buffer';

equations
"Quadrant 1 node 'toggle' wiggles when 'input_pin' is 1
toggle.t = input_pin;
toggle.clk = clock_pin;
toggle.ar = RESET;

"Quadrant 1 pin 'tog1' wiggles when toggle is 1
tog1.t = toggle;
tog1.clk = clock_pin;
tog1.ar = RESET;

"Quadrant 2 node 'tog2' wiggles when 'toggle' or 'tog1' is 1
tog2.t = toggle # tog1;
tog2.clk = clock_pin;
tog2.ar = RESET;

"Quadrant 2 pin 'tog3' wiggles when 'tog1' and 'tog2' are 1
tog3.t = tog1 & tog2;
tog3.clk = clock_pin;
tog3.ar = RESET;
```

Figure 2. The UR_RU.ABL ABEL file

In the UR_RU.FIT fitter log file in Figure 1, toggle_RU_2 and toggle_UR_1 are Regional-to-Universal (RU) and Universal-to-Regional (UR) converters. This is because the "toggle" signal is accessed by both the tog1 and tog2 output pins (see Figure 2 for the equations).

Note that the fitter option KEEP was used for the UR_RU design to illustrate the generation of the UR and RU converters. If there are no pin or node pre-assignments or if the IGNORE fitter option was used instead, then the fitter will make more efficient pin and node assignments.

Please refer to your Atmel ATV5000/ATV5100 Device Fitter manual for more information on the fitter log file.

Fitter Hints

The fitter hints described in this section help you fit your designs into an ATV5000 or ATV5100 device more efficiently. To implement these fitter hints, some modifications to your ABEL design files may be necessary.

If you are an Atmel-ViewPLD user, you can modify your schematics to bring about similar ABEL design modifications. If pin or node pre-assignments are recommended, they can be specified in the *design*.PN file. For more information on the .PN file, refer to the ATMPIN.DOC file. (The ATMPIN feature is supported in Atmel-ViewPLD Version 4.42 or higher).

Fitter Hint 1: Let the fitter makes its own pin and node assignments (IGNORE fitter option).

To allow maximum fitting efficiency, minimize the number of pre-assigned pins and nodes. With fewer constraints, the fitter can use its own pin and node assignments to its maximum capability. If you require pin pre-assignments to keep the fitter from changing the assignments (using the fitter option KEEP), then minimize the node pre-assignments. Note that in some designs, some pre-assignments may be able to "steer" the fitter to form or place signal groups that will lead to a higher fitting efficiency.

Figure 3 shows the UR_RU fitter log file with the IGNORE fitter option (ignore all pin and node pre-assignments). By ignoring the pre-assignments, the fitter was able to eliminate the use of the UR and RU converters, producing a more efficient and higher performance design fit.

Fitter Hint 2: Use the pin clock feature to break up large signal groups.

Atmel-VIewPLD Users: Use the symbols from the PDFF or CDFF primitive family in the DIO library. The PDFF primitives implement the pin clocking features, whereas the CDFF primitives allow the gated pin clocking functions.

If you have a large signal group (a function group that cannot fit into a single quadrant), then using the pin clocking or clock-enable feature (that is, using `signal.CE = pin_clk` equations) may help the fitter break up the large signal group into smaller, more efficient groups. Figures 4 and 5 show the `CNT10.ABL` 10-bit counter equations utilizing the product term and pin clocking features, respectively.

```
 Atmel P5000/P5100 fitter run on  4-Feb-94 03:28 PM.
==========================================
Warnings
==========================================
Fitting Device P5000.
Fitter mode=IGNORE
Converting cluster tog1 pin feedback to
registered feedback.
Converting cluster toggle pin feedback to registered feedback.
Converting cluster tog2 pin feedback to
registered feedback.
The Localized inputs are:
 RESET clock_pin input_pin
==========================================
 The Design Fits.
==========================================
  Overall Summary.
    Type                    Used  Free  Utilization
 Cell Usage
    Macrocells               1.00  75.00  1.3%  (0.00
                             Wasted)
 Pins Usage
    Inputs                   3 5  37.5%
    Outputs                  --  --  N/A
    IO                      2 50  3.8%
    Summary                 5 55  8.3%
==========================================
 Chip assignments summary.
Quadrant(1).
  clock_pin on 1
  RESET on 2
  tog3 on 15
  tog1 on 17
  tog2 on 133
  toggle on 132
Quadrant(2).
  input_pin on 32
Quadrant(3).
Quadrant(4).
```

Figure 3. The `UR_RU.FIT` file for the ATV5000 device (`IGNORE` fitter option)

```
CNTA.T = ((CNTA.FB + 1) $ CNTA.FB) & CE                    "CNTA = [A9..A0], Counter A
    # (INPUT $ CNTA.FB) & LD;                              "INPUT = [I9..I0]
CNTA.C = CLK1;                                             "Independent product term
                                                           "clocking
CNTA.AR = RST;
```

Figure 4. `CNT10.ABL` counter equations with product term clocking

```
CNTA.T = ((CNTA.FB + 1) $ CNTA.FB) & CE                    "CNTA = [A9..A0], Counter A
    # (INPUT $ CNTA.FB) & LD;                              "INPUT = [I9..I0]
CNTA.CE = CLK1;   CNTA.CK = ^h3FF;                         ".CE equation to
                                                           "implement pin clocking
CNTA.AR = RST;
```

Figure 5. `CNT10.ABL` counter equations with pin clocking

Figures 6 and 7 show the chip assignments summary of the CNT10 fitter log files for the designs with product term and pin clocking options. The CNT10 design consists of four 10-bit loadable counters in which the outputs of one counter are loaded into the next counter. Since the outputs of the counters are inputs for the next counters, the fitter will form a single large

```
 Chip assignments summary.
Quadrant(1).
  CE on 1
  LD on 2
  CLK on 4                <clock for counters A, B, C and D via product terms>
  RST on 5
  I6 on 6
  A9 on 7
  A8 on 8
  A7 on 9
  A6 on 10
  A5 on 11
  A4 on 12
  A3 on 13
  A2 on 14
  A1 on 15
  A0 on 17
Quadrant(2).
  I7 on 18
  I8 on 19
  C9 on 21
  C8 on 22
  C7 on 23
  C6 on 24
  C5 on 25
  C4 on 26
  C3 on 27
  C2 on 28
  C1 on 29
  C0 on 30
  B0 on 31                <Counter B output in Quadrant 2>
    I0 on 32
    I1 on 34
Quadrant(3).
    I3 on 35
    I2 on 36
    I9 on 38
    D9 on 40
    D8 on 41
    D7 on 42
    D6 on 43
    D5 on 44
    D4 on 45
    D3 on 46
    D2 on 47
    D1 on 48
    D0 on 49
    B1 on 51              <Counter B output in Quadrant 3>
Quadrant(4).
    B9 on 58
    B8 on 59
    B7 on 60
    B6 on 61
    B5 on 62
    B4 on 63
    B3 on 64
    B2 on 65
    I4 on 66    I5 on 68
```

Figure 6. Fitter log file for CNT10.ABL with product term clocking

```
Chip assignments summary.
Quadrant(1).
    LD on 1
    CLK1 on 2              (clock for counter A)
    RST on 4
    I2 on 5
    I3 on 6
    A9 on 7
    A8 on 8
    A7 on 9
    A6 on 10
    A5 on 11
    A4 on 12
    A3 on 13
    A2 on 14
    A1 on 15
    A0 on 17
Quadrant(2).
    I4 on 18
    I5 on 19
    I6 on 21
    B9 on 22
    B8 on 23
    B7 on 24
    B6 on 25
    B5 on 26
    B4 on 27
    B3 on 28
    B2 on 29
    B1 on 30
    B0 on 31
    CLK2 on 32             (clock for counter B)
    CE on 34
Quadrant(3).
    I0 on 35
    CLK3 on 36
    I7 on 38
    I8 on 39
    I9 on 40
    C9 on 41
    C8 on 42
    C7 on 43
    C6 on 44
    C5 on 45
    C4 on 46
    C3 on 47
    C2 on 48
    C1 on 49
    C0 on 51               (clock for counter C)
Quadrant(4).
    D9 on 56
    D8 on 57
    D7 on 58
    D6 on 59
    D5 on 60
    D4 on 61
    D3 on 62
    D2 on 63
    D1 on 64
    D0 on 65
    CLK4 on 66             (clock for counter D)
    I1 on 68
```

Figure 7. Fitter log file for `CNT10.ABL` with pin clocking

group for these counters. As illustrated by the fitter log files, the fitter separated each counter more efficiently in the design with the pin clocking option. In Figure 6, some of the counter B outputs were scattered to other quadrants instead of being grouped together in a single quadrant. For this design example, these scattered placements of the counter B outputs pose no performance penalty. But for a very complex design, the scattered pin or node placements may inhibit efficient fitting.

```
 Atmel P5000/P5100 fitter run on  7-Feb-94 10:41 PM.
==========================================
Warnings
==========================================
Fitting Device P5000.
Fitter mode=IGNORE
Converting cluster Ace pin feedback to registered feedback.
Converting cluster S3 pin feedback to registered feedback.
Converting cluster S2 pin feedback to registered feedback.
Converting cluster S1 pin feedback to registered feedback.
Converting cluster S0 pin feedback to registered feedback.
The Localized inputs are:
 V4 V3 V2 V1 V0
Universal element Add10 regionalized.
Universal element Sub10 regionalized.
Universal element Q0 regionalized.
Universal element Q2 regionalized.
Universal element Add10 regionalized.
Universal element Sub10 regionalized.
Signal C2 inverted to get better term usage.
==========================================
 The Design does NOT fit.
==========================================
  Overall Summary.
   Type                    Used  Free  Utilization
------------------------------------------------
 Cell Usage
   Macrocells             18.75 53.50 29.4% (3.50 Wasted)
 Pins Usage
   Inputs                  5 3  62.5%
   Outputs                 -- --  N/A
   IO                      15 37 28.8%
   Summary                 20 40 33.3%
==========================================
Chip assignments summary.
Quadrant(1).
    V3 on 1
    V4 on 2
    S1 on 761
    S3 on 762
    S2 on 763
    Clk on 7
    D5 on 8
    D3 on 9
    D2 on 10
    D4 on 11
    D1 on 12
    Q2_UR_4 on 78
    C4 on 79
    Bust on 80
    Hit on 81
    Add10_UR_1 on 173
    C3 on 174
    Sub10_UR_2 on 175
    C2 on 176
    C1 on 177
    Q0_UR_3 on 178
```

Figure 8. Original chip assignments summary of the `JACK5000.FIT` file *(continues)*

```
    Clr on 4
    CardIn on 5
    CardOut on 6
  1 partitioned but unassigned signals.
 Q1
Quadrant(2).
    Sub10 on 27
    Add10 on 28
    Q2 on 29
    Q0 on 30
    Ace on 31
    V2 on 32
    V1 on 34
    is_Ace on 179
Quadrant(3).
    V0 on 36
    D0 on 49
    S0_RU_7 on 107          <RU Converter>
 Converter
    Add10_UR_5 on 185
    Sub10_UR_6 on 186
    S0 on 159
Quadrant(4).
    S4_RU_8 on 120          <RU Converter>
 Converter
  1 partitioned but unassigned signals.
 S4
```

Figure 8. *(Continued)* Original chip assignments summary of the `JACK5000.FIT` file

Fitter Hint 3: Reduce the number of RU converters by promoting registered nodes that are referenced by other pins or nodes placed in other quadrants to pins

Atmel-ViewPLD Users: Add and connect the OUT symbol from the DIO library to the registered nodes.

The ATV5000/ATV5100 automatically generates RU converters so that the regional signals from one quadrant can be routed to other quadrants. In the fitter log files, the RU converters are indicated by the suffix `_RU_n`, where `n` is the total number of occurrences of the RU and UR converters. In Figure 8, the chip assignments summary of the JACK5000 fitter log file (`JACK5000.FIT`) shows that RU converters were generated for the S0 and S4 registered nodes. The RU converters were generated because these regional registered nodes are being ref-

```
D0 = (S0.FB);

D1 = (!S4.FB & !S3.FB & S1.FB
     # !S3.FB & S2.FB & S1.FB
     # S4.FB & S3.FB & !S2.FB & S1.FB
     # !S4.FB & S3.FB & S2.FB & !S1.FB
     # S4.FB & !S3.FB & !S2.FB & !S1.FB);

D2 = (!S4.FB & !S3.FB & S2.FB
     # S4.FB & S3.FB & !S2.FB
     # !S4.FB & S2.FB & S1.FB
     # S4.FB & !S2.FB & !S1.FB);

D3 = (S4.FB & !S3.FB & !S2.FB & S1.FB
     # S4.FB & S3.FB & S2.FB & !S1.FB
     # !S4.FB & S3.FB & !S2.FB & !S1.FB);

D4 = (!S4.FB & S3.FB & S2.FB
     # S4.FB & !S3.FB & !S2.FB
     # !S4.FB & S3.FB & S1.FB
     # S3.FB & S2.FB & S1.FB);

D5 = (S4.FB & S3.FB
     # S4.FB & S2.FB);
```

Figure 9. Optimized equations of JACK5000 design example

erenced by the nodes placed in other quadrants. A look at the optimized equations shown in Figure 9 confirms that the S0 and S4 nodes are inputs to the D0, D1, D2, D3 and D4 output pins.

After promoting the S0 and S4 nodes to pins, the JACK5000 ABEL file was re-compiled. As shown in Figure 10, the updated fitter log file now contains a few more RU converters.

```
 Atmel P5000/P5100 fitter run on  7-Feb-94 10:39 PM.
==============================================
Warnings
==============================================
Fitting Device P5000.
Fitter mode=IGNORE
Converting cluster Ace pin feedback to registered feedback.
Converting cluster S0 pin feedback to registered feedback.
Converting cluster S3 pin feedback to registered feedback.
Converting cluster S2 pin feedback to registered feedback.
Converting cluster S1 pin feedback to registered feedback.
The Localized inputs are:
 V4 V3 V2 V1 V0
Universal element Add10 regionalized.
Universal element Sub10 regionalized.
Universal element Q0 regionalized.
Universal element Q2 regionalized.
Signal C2 inverted to get better term usage.
==============================================
 The Design does NOT fit.
==============================================
  Overall Summary.
    Type                    Used Free  Utilization
 Cell Usage
    Macrocells             17.50 54.2528.4%  (4.00 Wasted)
 Pins Usage
    Inputs                  5 3  62.5%
    Outputs                 -- --  N/A
    IO                       16 36  30.8%
    Summary                  21 39  35.0%
==============================================
 Chip assignments summary.
Quadrant(1).
    V3 on 1
    V4 on 2
    S1 on 761
    S3 on 762
    S2 on 763
    Clk on 7
    D2 on 8
    D1 on 9
    S1_RU_7 on 75
 Converter
    S2_RU_6 on 76
 Converter
    S3_RU_5 on 77
 Converter
    Q2_UR_4 on 78
    C4 on 79
    Bust on 80
    Hit on 81
    Add10_UR_1 on 173
    C3 on 174
    Sub10_UR_2 on 175
    C2 on 176
    C1 on 177
    Q0_UR_3 on 178
```

Figure 10. Chip assignments summary of the `JACK5000.FIT` file after promoting S0 and S4 nodes to pins *(continues)*

```
    Clr on 4
    CardIn on 5
    CardOut on 6
  1 partitioned but unassigned signals.
 Q1
Quadrant(2).
    Sub10 on 27
    Add10 on 28
    Q2 on 29
   Q0 on 30
     Ace on 31
    V2 on 32
    V1 on 34
    is_Ace on 179
Quadrant(3).
    V0 on 36
    D0 on 49
    S0 on 51
  1 partitioned but unassigned signals.
 S4
Quadrant(4).
    D5 on 63
    D3 on 64
    D4 on 65
```

Figure 10. *(Continued)* Chip assignments summary of the `JACK5000.FIT` file after promoting S0 and S4 nodes to pins

```
 Atmel P5000/P5100 fitter run on  7-Feb-94 10:34 PM.
============================================
Warnings
============================================
Fitting Device P5000.
Fitter mode=IGNORE
Converting cluster Ace pin feedback to registered feedback.
Converting cluster S3 pin feedback to registered feedback.
Converting cluster S2 pin feedback to registered feedback.
Converting cluster S1 pin feedback to registered feedback.
Converting cluster S0 pin feedback to registered feedback.
The Localized inputs are:
 V4 V3 V2 V1 V0
Universal element Sub10 regionalized.
Universal element Add10 regionalized.
Universal element S4 regionalized.
Universal element S3 regionalized.
Universal element S3 regionalized.
Universal element S1 regionalized.
Universal element S4 regionalized.
Signal C2 inverted to get better term usage.
============================================
 The Design Fits.
============================================
  Overall Summary.
   Type                    Used  Free Utilization
------------------------------

 Cell Usage
   Macrocells            22.00 51.25  32.6%  (2.75 Wasted)
 Pins Usage
```

Figure 11. Chip assignments summary of the `JACK5000.FIT` file after promoting S0, S1, S2, S3, and S4 nodes to pins *(continues)*

The nodes promotion process is repeated for the S1, S2, and S3 registered nodes.

With the promotion of S0, S1, S2, S3 and S4 registered nodes to pins, the JACK5000 design successfully fit into the ATV5000 device. The chip assignments summary in Figure 11 shows that all the RU converters were successfully eliminated.

Fitter Hint 4: Reduce the number of RU and UR converters by targeting the ATV5100 instead of the ATV5000.

The ATV5100 device has an architecture very similar to the ATV5000. One advantage the ATV5100 has over the ATV5000 is that there are more universal routing resources for logic functions in the ATV5100 (a maximum of 8 universal product terms in the ATV5100 versus 4 in the ATV5000). This device is well suited for applications that have large signal groups (for example, large state machines) which can not be fitted into a single quadrant.

```
    Inputs                    5 3 62.5%
    Outputs                   --  --  N/A
    IO                          21  31  40.4%
    Summary                     26  34  43.3%
 ============================================
  Chip assignments summary.
 Quadrant(1).
     V3 on 1
     V4 on 2
     Clk on 4
     Clr on 5
     CardIn on 6
     CardOut on 7
     S2 on 13
     S3 on 14
     S4 on 15
     S1 on 17
     C4 on 173
     C3 on 174
     C2 on 175
     C1 on 176
     Sub10_UR_1 on 177
     Add10_UR_2 on 178
 Quadrant(2).
     Add10 on 26
     Sub10 on 27
     Q2 on 28
     Ace on 29
     Q0 on 30
     Q1 on 31
     V2 on 32
     V1 on 34
     Hit on 179
     Bust on 180
     is_Ace on 181
     S4_UR_3 on 182
     S3_UR_4 on 183
 Quadrant(3).
     V0 on 36
     D5 on 46
     D3 on 47
     D2 on 48
     D4 on 49
     D1 on 51
     S3_UR_5 on 185
     S1_UR_6 on 186
     S4_UR_7 on 187
 Quadrant(4).
     D0 on 64
     S0 on 65
```

Figure 11. *(Continued)* Chip assignments summary of the `JACK5000.FIT` file after promoting S0, S1, S2, S3, and S4 nodes to pins

Figure 12 shows the ATV5100 chip assignments summary of the original JACK5000 ABEL source file . Comparing the fitter log files in Figures 8 and 12, the design fits more efficiently in the ATV5100 device than the ATV5000 device.

By applying the fitter hint 3, the RU converters can be removed by promoting the S0, S1, S2, S3, and S4 registered nodes to pins. The fitter log file in Figure 13 shows that there are only two UR converters compared to six converters for the ATV5000 device (refer to Figure 11).

```
 Atmel P5000/P5100 fitter run on  8-Feb-94 11:54 AM.
============================================
Warnings
============================================
Fitting Device P5100.
Fitter mode=IGNORE
Converting cluster Ace pin feedback to registered feedback
Converting cluster S3 pin feedback to registered feedback.
Converting cluster S2 pin feedback to registered feedback.
Converting cluster S1 pin feedback to registered feedback.
Converting cluster S0 pin feedback to registered feedback.
The Localized inputs are:
 V4 V3 V2 V1 Clr
Universal element Add10 regionalized.
Universal element Sub10 regionalized.
Universal element V0 regionalized.
Signal C2 inverted to get better term usage.
============================================
 The Design Fits.
============================================
  Overall Summary.
    Type                    Used Free  Utilization
 Cell Usage
    Macrocells             15.75  56.50  25.4%  (3.50 Wasted)
 Pins Usage
    Inputs                  5 3  62.5%
    Outputs                 --  --  N/A
    IO                       16 36  30.8%
    Summary                 21 39  35.0%
============================================
 Chip assignments summary.
Quadrant(1).
    V3 on 1
    V4 on 2
    S1 on 761
    S3 on 762
    S2 on 763
    Clk on 7
    D5 on 8
    D3 on 9
    D2 on 10
    D4 on 11
    D1 on 12
    Q1 on 13
    C4 on 79
    Bust on 80
    Hit on 81
    C2 on 173
    C3 on 174
    C1 on 175
    Add10_UR_1 on 176
    Sub10_UR_2 on 177
    V0 on 4
    CardIn on 5
```

Figure 12. ATV5100 chip assignments summary of the original JACK5000 file *(continues)*

```
    CardOut on 6
Quadrant(2).
    Sub10 on 27
    Add10 on 28
    Q2 on 29
    Q0 on 30
    Ace on 31
    V2 on 32
    V1 on 34
    is_Ace on 179
Quadrant(3).
    Clr on 36
    D0 on 49
    S0_RU_4 on 107
    V0_UR_3 on 185
    S0 on 159
Quadrant(4).
    S4 on 800
    S4_RU_5 on 120
```

Figure 12. *(Continued)* ATV5100 chip assignments summary of the original JACK5000 file

```
 Atmel P5000/P5100 fitter run on  8-Feb-94 01:09 PM.
==============================================
Warnings
==============================================
Fitting Device P5100.
Fitter modeIGNORE
Converting cluster Ace pin feedback to registered feedback.
Converting cluster Add10 pin feedback to registered feedback.
Converting cluster Sub10 pin feedback to registered feedback.
Converting cluster S4 pin feedback to registered feedback.
Converting cluster S3 pin feedback to registered feedback.
Converting cluster S2 pin feedback to registered feedback.
Converting cluster S1 pin feedback to registered feedback.
Converting cluster S0 pin feedback to registered feedback.
The Localized inputs are:
 V4 V3 V2 V1 Clr
Universal element Add10 regionalized.
Universal element Sub10 regionalized.
Signal C2 inverted to get better term usage.
==============================================
 The Design Fits.
==============================================
  Overall Summary.
   Type                    Used  Free  Utilization
-------------------------
 Cell Usage
   Macrocells             16.25  57.00  25.0%  (2.75 Wasted)
 Pins Usage
   Inputs                  5  3  62.5%
   Outputs                 --  --  N/A
   IO                       21  31  40.4%
   Summary                 26  34  43.3%
==============================================
 Chip assignments summary.
Quadrant(1).
    V3 on 1
    V4 on 2
```

Figure 13. ATV5100 chip assignments summary of the `JACK5000.FIT` file after promoting S0, S1, S2, S3, and S4 nodes to pins *(continues)*

```
    Clk on 4
    V0 on 5
    CardIn on 6
    CardOut on 7
    S2 on 13
    S3 on 14
    S4 on 15
    S1 on 17
    C4 on 173
    C3 on 174
    C2 on 175
    C1 on 176
    Add10_UR_1 on 177          <1st UR converter>
    Sub10_UR_2 on 178          <2nd UR converter>
Quadrant(2).
    Add10 on 26
    Sub10 on 27
    Q2 on 28
    Ace on 29
    Q0 on 30
    Q1 on 31
    V2 on 32
    V1 on 34
    Hit on 179
    Bust on 180
    is_Ace on 181
Quadrant(3).
    Clr on 36
    D5 on 46
    D3 on 47
    D2 on 48
    D4 on 49
    D1 on 51
Quadrant(4).
    D0 on 64
    S0 on 65
```

Figure 13. *(Continued)* ATV5100 chip assignments summary of the `JACK5000.FIT` file after promoting S0, S1, S2, S3, and S4 nodes to pins

Fitter Hint 5: Reduce the UR converters by promoting registered nodes with many product terms to pins.

Normally, the ATV5000/ATV5100 fitter will choose the Default or Reverse polarity equations with the fewest number of product terms for the combinatorial nodes and for both the registered and combinatorial output pins (refer to Figure 14). But for the registered nodes, the ATV5000/ATV5100 fitter only implements the Default polarity equations (inverting is not done because of complications arising from T-type flip-flops and reset and preset configurations).

The ABEL Optimizer (PLAOPT) produces two sets of equations, Default and Reverse polarity, for each equation in your design. Both equation sets are functionally equivalent. However, in order to select the Reverse polarity equations, the fitter must invert the polarity of the output signals. This inversion can be achieved simply by setting the polarity of the Atmel PLD outputs to negative or invert (all Atmel PLDs have polarity control on their outputs). For internal combinatorial nodes without polarity control capabilities, the ATV5000/ATV5100 fitter accomplishes the inversions by inverting the references to these nodes in all equations.

Figure 14 shows the FIT50A ABEL example, which illustrates how to ensure that both the Default and Reverse polarity equations are accessible to the fitter.

```
module FIT50A;
title 'A simple design example that the fitter will choose the Default or
       Reverse polarity equations with the fewest number of product terms.';

"Use KEEP fitter option to force to I0..I7 to use the I/O pins as inputs.

CLK pin 1;
RST pin 2;
I0,I1,I2,I3,I4,I5,I6,I7 pin 18,19,21,22,23,24,25,26;

BurCOM node istype 'com'; "COM Node is OK because fitter
                          "automatically choose polarity.  Note that if
                          "the Reverse polarity is chosen, vectors may
                          "failed due to the inversion (if this node is
                          "simulated). In this case, simply add the ! to
                          "the node label in the TEST_VECTORS
                          "section would allow the node to be
                          "simulated.
BurREG node istype 'reg_d'; "Should promote this node to pin because
                          "Default polarity equations are used for
                          "all the registered nodes.

OUTCOM pin istype 'com';    "Fitter will choose polarity equations.

OUTREG pin istype 'reg_d';  "Fitter will choose polarity equations as long
                            "as the .D dot extensions are not used in the
                           "equations. Do not use BUFFER as it will
                            "force fitter to use only the Default polarity.
                            "Default polarity will always be chosen for
                            "REG_T type register.  If the Reverse polarity
                            "is used, the Reset (power-up and
                            "asynchonous) and Preset (asynchonous)
                          "vectors may need to be changed.

"CREATE BUSES
Input = [I7..I0];
EQUATIONS
                            "Default Polarity / Reverse Polarity
BurCOM  = !(Input == 1);    "  8 p-terms      /  1 p-term
OUTCOM  = !((Input == 1) & BurCOM);"  9 p-terms      /  1 p-term

                                  "Default Polarity / Reverse Polarity
BurREG := !(Input == 1);          "  8 p-terms      /  1 p-term
BurREG.c = CLK;                   "If REG_D type flip-flop, use the :=
BurREG.ar = RST;                  "instead of the .D so that the fitter
                                  "or fusemapper will choose Default
                                  "or Reverse polarity equations with
                                  "the fewest product-terms

OUTREG := !((Input == 1) & BurREG); "  9 p-terms      /  1 p-term
OUTREG.c = CLK;
OUTREG.ar = RST;

END;
```

Figure 14. FIT50A ABEL design example to allow fitter to choose Default or Reverse polarity equations

The chip assignments summary in Figure 15 shows that there are four UR converters. A quick look at the FIT50A PLA optimized file (Figure 16) confirms that the Reverse polarity equation of the BurREG node should be used (that is, one product term versus eight product terms in the Default equation). Using fitter hint 5, these UR converters could be eliminated by promoting the BurREG node to pin.

```
 Atmel P5000/P5100 fitter run on  8-Feb-94 03:17 PM.
============================================================
Warnings
============================================================
Fitting Device P5000.
Fitter mode=KEEP
Converting cluster BurREG pin feedback to registered feedback.
Clust BurREG had 8 universals (possible 4) which needed patching.
Universal element I0 was regionalized.
Clust BurREG had 7 universals (possible 4) which needed patching.
Universal element I1 was regionalized.
Clust BurREG had 6 universals (possible 4) which needed patching.
Universal element I2 was regionalized.
Clust BurREG had 5 universals (possible 4) which needed patching.
Universal element I3 was regionalized.
Signal BurCOM inverted to get better term usage.<Reverse polarity equation
used for Burcom>
============================================================
 The Design Fits.
============================================================
  Overall Summary.
   Type                    Used  Free  Utilization
------------------------
 Cell Usage
   Macrocells             6.25  67.75 10.9%  (2.00 Wasted)
 Pins Usage
   Inputs                  2  6  25.0%
   Outputs                 --  --  N/A
   IO                      10  42  19.2%
   Summary                 12  48  20.0%
============================================================
 Chip assignments summary.
Quadrant(1).
    CLK on 1
    RST on 2
    BurREG on 761
    OUTREG on 15
    OUTCOM on 17
    BurCOM on 173
    IO_UR_1 on 174
    I1_UR_2 on 175
    I2_UR_3 on 176
    I3_UR_4 on 177
Quadrant(2).
    I0 on 18
    I1 on 19
    I2 on 21
    I3 on 22
    I4 on 23
    I5 on 24
    I6 on 25
    I7 on 26
Quadrant(3).
Quadrant(4).
```

Figure 15. Original FIT50A fitter log file (no modifications)

```
Product Term Usage:
          Default  Reverse   Signal
          Polarity Polarity  Signal
           ——   ——   ——

              8        1     BurCOM
              9        1     OUTCOM
              8        1     BurREG.REG
              1        1     BurREG.C
              1        1     BurREG.AR
              9        1     OUTREG.REG
              1        1     OUTREG.C
              1        1     OUTREG.AR
```

Figure 16. FIT50A PLA Optimized file

```
 Atmel P5000/P5100 fitter run on  8-Feb-94 04:03 PM.
==========================================================
Warnings
==========================================================
Fitting Device P5000.
Fitter mode=KEEP
Converting cluster BurREG pin feedback to registered feedback.
Signal BurCOM inverted to get better term usage.
==========================================
 The Design Fits.
==========================================
  Overall Summary.
   Type                    Used  Free  Utilization
————————
 Cell Usage
   Macrocells             1.75  72.25 4.9%  (2.00 Wasted)
 Pins Usage
   Inputs                  2  6  25.0%
   Outputs                 --  --  N/A
   IO                       11  41  21.2%
   Summary                  13  47  21.7%
==========================================
 Chip assignments summary.
Quadrant(1).
    CLK on 1
    RST on 2
    OUTREG on 14
    BurREG on 15
    OUTCOM on 17
    BurCOM on 173
Quadrant(2).
    I0 on 18
    I1 on 19
    I2 on 21
    I3 on 22
    I4 on 23
    I5 on 24
    I6 on 25
    I7 on 26
Quadrant(3).
Quadrant(4).
```

Figure 17. Fit50A fitter log file (with promotion of BurREG node to pin)

Fitter Hint 6: Use the fitter option NO_FB_CONVERT to reduce the UR converters.

In the default condition (that is, without the NO_FB_CONVERT option), the ATV5000/ATV5100 fitter will automatically convert references of all registered output-only pins (non-three-statable output pins) so that any equations referencing these signals will utilize their (regional) internal Q1 registered feedbacks (via the ABEL .FB extension) instead of the (universal) pin feedbacks (that is, feedbacks directly from the output pins). Refer to the ATV5000 macrocell configuration in Figure 9 of the ATV5000 data sheet for more information on the feedback types. Which feedbacks you use is important because the internal Q1 registered feedbacks are regional signals, and the pin feedbacks are universal signals. With most designs, utilizing the internal Q1 registered feedbacks will result in the optimal fitting efficiency.

In the fitter log file of the ABEL design example FIT50, the message *"Converting cluster A pin feedback to registered feedback"* means that the internal Q1 registered feedback of the output A will be used for all equations referencing it. The fitter appends the .FB extension to all references of the output A.

```
FIT50 ABEL design example:
Original ABEL equation: B.D = (I & A);
  "A is registered output-only pin
Fitter output equation: B.D = (I & A.FB);
```

With the NO_FB_CONVERT option enabled (specify NO_FB_CONVERT in the Alternate Fitter Strategy box in the Fit Options... command window), the ATV5000/ATV5100 fitter disables the "registered feedback" conversions. This means that the fitter will not mod-

```
module FIT50;
title 'Fitter example showing the use of NO_FB_CONVERT fitter option
       to minimize the Universal-to-Regional (UR) converters for the
       ATV5000 or ATV5100';
"Use fitter option "KEEP" and "NO_FB_CONVERT"

CLK pin;
RST pin;
I pin;

A pin 4 istype 'reg_d,buffer';
B pin 5 istype 'reg_d,buffer';
C pin 6 istype 'reg_d,buffer';

D node 774 istype 'reg_d,buffer';
E pin 19 istype 'reg_d,buffer';

"Input Bus
Regs = [A,B,C,D,E];

EQUATIONS

Regs.c = CLK;
Regs.ar = RST;

A.d = I;                    "Output A forced to Quadrant 1
B.d = I & A.FB;             "Output B forced to Quadrant 1
C.d =  A.FB & B.FB          "Output C forced to Quadrant 1
     # A.FB & C.FB          "Output C requires the .FB feedbacks to be used in
     # B.FB & C.FB          "some product terms because both A and B outputs are
     # B & E                "in the same quadrant as output C. Output E is in
     # C & E;               "quadrant 2 so the last two product terms will be
                            "universal regardless of whether .FB feedbacks are used
                            "for B and C feedbacks.

D.d = A & B                 "Node D forced to Quadrant 2
     # A & C                "Keep feedbacks A, B and C as universal product signals
     # B & C;               "(maximum universal product terms for a registered node
                              "is 4).

E.d =  D;           "Output E forced to Quadrant 2

END;
```

Figure 18. FIT50 ABEL design example for illustrating the NO_FB_CONVERT fitter option

ify the references of the registered output-only pins and will use the .FB, .Q, or .PIN (or no extension) feedback types specified in the original ABEL source file. By specifying the feedback types, you may be able to reduce the number of UR converters in your designs.

Note: The NO_FB_CONVERT fitter option will only be effective when registered nodes in one quadrant reference the registered output-only pins located in other quadrants.

Figure 18 shows the ABEL equations of the FIT50 design example. To illustrate the NO_FB_CONVERT option, the KEEP fitter option was used to force the fitter to place the output pins and nodes in different quadrants (directed by the pin and node pre-assignments).

```
 Chip assignments summary.
Quadrant(1).
    RST on 1
    CLK on 2
    A on 4
    B on 5
    C on 6
Quadrant(2).
    D on 774
    E on 19
    I on 32
    A_UR_1 on 179
    B_UR_2 on 180
    C_UR_3 on 181
Quadrant(3).
Quadrant(4).
```

Figure 19. Chip assignments summary of FIT50 without NO_FB_CONVERT fitter option

```
 Chip assignments summary.
Quadrant(1).
    RST on 1
    CLK on 2
    A on 4
    B on 5
    C on 6
Quadrant(2).
    D on 774
    E on 19
    I on 32
Quadrant(3).
Quadrant(4).
```

Figure 20. Chip assignments summary of FIT50 with NO_FB_CONVERT fitter option

Using the Programmable Polarity Control

The output programmable polarity control in PLDs brings efficiency in logic reduction and control of output polarity to the customers. Unfortunately, it also brings confusion to customers who are not familiar with the software syntax to properly configure the output polarity.

This application note shows the proper usage of the popular ABEL™ and CUPL™ syntax to configure the output polarity of Atmel PLDs.

Configuring Polarity with Atmel-ABEL™ (4.x or higher)

The optimization level best suited for Atmel PLDs is the default option – reduce by pin and auto polarity. This reduction level will take advantage of the polarity control when performing logic optimization one output at a time. This will override the ISTYPE 'NEG' and ISTYPE 'POS' used in ABEL™ 3.x source files (check the user manual on backward compatibility for detail). Therefore, the 'NEG' and 'POS' extensions are not recommended.

The following examples have A, B, and C defined as inputs and OUT or !OUT as the output:

Case 1: (Combinatorial - no ISTYPE definition or ISTYPE 'COM')

```
Declaration
OUT pin 14;
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will consider both Figure 1 (on-set) and Figure 2 (off-set) and automatically select the implementation requiring fewer product terms for the same function. The outcome is represented by Figure 2. Since Figures 1 and 2 are each DeMorgan equivalent of the other, either one is logically correct.

Case 2: (Combinatorial - ISTYPE 'BUFFER')

```
Declaration
OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will only consider the on-set because the ISTYPE 'BUFFER' overrides the automatic selection. The outcome is represented by Figure 1.

Case 3a: (Combinatorial - ISTYPE 'INVERT')

```
Declaration
OUT pin 14 ISTYPE 'invert'; "as-
sume 14 is an I/O pin
equations
OUT = A # B # C;
```

In this case, the compiler will only consider Figure 2 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection. The outcome is represented by Figure 2.

Case 3b: (Combinatorial - no ISTYPE definition)

```
Declaration
!OUT pin 14;
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

The compiler would pick Figure 3 to implement the logic because it takes fewer product terms. In ABEL™ documentation, signals on the right side of the equation do not have "!" as part of their names. ABEL™ preprocessor will remove the "!" from the pin name on the right side of the equation and replace all references on the left side with an additional "!". Logically, this does not change anything. It does, however, tend to create some confusion reading the .DOC files. In the source file, the user should still use whatever pin name is given in the declaration section. All references to the pin or .FB feedbacks will be adjusted by the software to reflect the changes automatically.

Case 3c: (Combinatorial - ISTYPE 'INVERT')

```
Declaration
!OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT = A # B # C;
```

The compiler would pick Figure 4 to implement the logic.

For combinatorial equations, it is best to leave out the ISTYPE statement and let the optimizer choose the best DeMorgan equivalent implementation.

Figure 1.

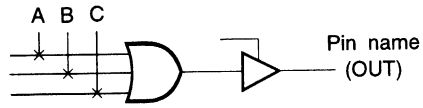


Figure 2.

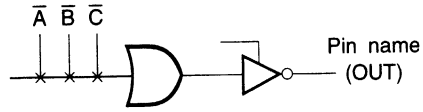


Figure 3.

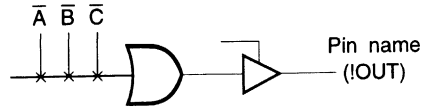
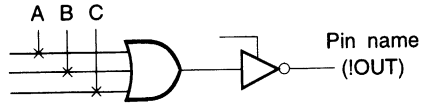


Figure 4.



Note: The "buffer" or "invert" ISTYPE has no effect for combinatorial outputs in Atmel-ABEL 5.x.

Case 4: (Registered - no ISTYPE definition) Beware!

```
Declaration
OUT pin 14;
"assume 14 is an I/O pin
equations
OUT  := A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The pre-processor will warn you for not specifying the ISTYPE of the output. In this case, the compiler will use the fewest product term implementation (Figure 6). This might not be what the user is expecting.(1)

Note:

1. Figure 5 and Figure 6 do not produce identical results. In Figure 5, at power up or after a reset, the output pin appears to be a "0." Unlike Figure 5, Figure 6 powers up and resets to a "1" on the output. Preset and preload behave differently between the two as well. In some applications where power-up state of a register is not important and it never resets or presets, Figures 5 and 6 become identical. Only in this case are they logically equivalent. When using a registered output, always specify the ISTYPE desired.

Case 5: (Registered - ISTYPE 'BUFFER')

```
Declaration
OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT  := A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 5 (on-set) because the ISTYPE 'BUFFER' overrides the automatic selection.

Case 6: (Registered - ISTYPE 'INVERT') Be careful!

```
Declaration
OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT  := A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 6 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection (see Note 1 on Case 4).

Case 7: (Registered - ISTYPE 'BUFFER') Confusing – don't use.

```
Declaration
!OUT pin 14 ISTYPE 'buffer';
"assume 14 is an I/O pin
equations
OUT  := A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 7 (on-set) because the ISTYPE 'BUFFER' overrides the automatic selection.

Case 8: (Registered - ISTYPE 'INVERT')

```
Declaration
!OUT pin 14 ISTYPE 'invert';
"assume 14 is an I/O pin
equations
OUT  := A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The compiler will only consider Figure 8 (off-set) because the ISTYPE 'INVERT' overrides the automatic selection. In ABEL™ documentation, the pin name will be stripped of the "!". It will replace all pin name references with an additional "!" on the right-hand side of the equations.

Figure 5.

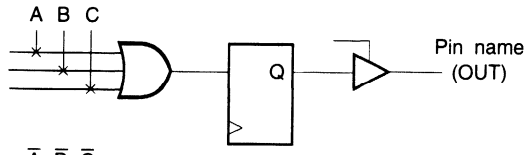


Figure 6.

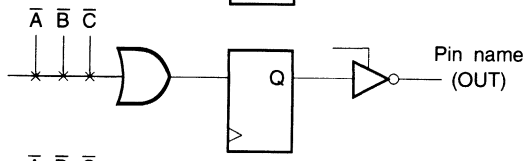


Figure 7.

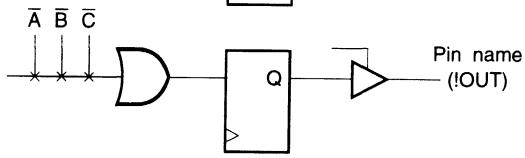
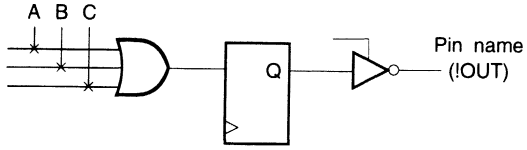


Figure 8.



Note: For cases 4 through 8, if you used the dot extension (.D, .T, etc) in your output equations (like "Out.d = A # B # C;"), then the compiler will only consider the "Buffer" condition (on-set) even when the "invert" ISTYPE is specified for these outputs. The "Buffer" condition is also only considered when you specify REG_T, REG_G, REG_JK or REG_SR in your ISTYPE statement.

Configuring Polarity with Internal Nodes

Internal nodes do not have programmable polarity control. Do not use any ISTYPE extensions. Think of it as "positive logic" only.

Case 1: (Figure 9)

```
Declaration
OUT node 50;
"assume 50 is an internal node
equations
OUT = A # B # C;
```

Case 2: (Figure 10)

```
Declaration
OUT node 50;
"assume 50 is an internal node
equations
OUT.d  = A # B # C;
OUT.c  = CLK;
OUT.ar = AR1;
```

The above example is the only legal method of assigning equations to nodes.

Figure 9.

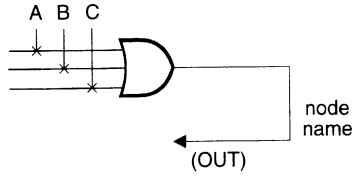
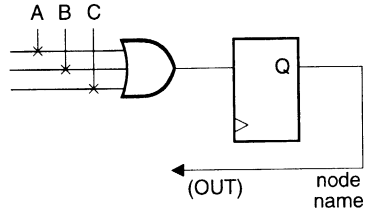


Figure 10.



Configuring Polarity with CUPL™

Note that CUPL™ has no "buffer/invert" ISTYPE statement. Output polarity is controlled by pin declaration versus equation polarity.

Case 1: (Combinatorial)

```
PIN 14 = OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 11. It does not choose the better DeMorgan equivalent automatically. If your equation does not fit, you should check to see if you can rewrite it as:

```
PIN 14 = OUTC;
!OUTC = !A & !B & !C;
```

Case 2: (Combinatorial)

```
PIN 14 = !OUTC; /* assume 14 is an I/O pin */
OUTC = A # B # C;
```

The compiler would choose Figure 12. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation.

Case 3: (Registered)

```
PIN 14 = OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 13. The pin name and the equation name are identical; the compiler does not place an inverter on the output.

Case 4: (Registered)

```
PIN 14 = !OUTC; /* assume 14 is an I/O pin */
OUTC.d = A # B # C;
OUTC.ck = CLK;
```

The compiler would choose Figure 14. The difference between the pin declaration (!OUTC) and the equation name (OUTC) tells the compiler to have an inverter on the output and to implement the equations as specified by the equation. CUPL™ maintains the !OUTC on the pinout diagram documentation and equation name OUTC in the reduced equation portion of the documentation.

Both ABEL™ and CUPL™ conventions for handling signal polarity have drawn praises and criticisms. Help on the software is readily available from Data I/O Corporation (ABEL™), Logical Devices, Incorporated (CUPL™), and Atmel. Don't hesitate to call for help.

6

Figure 11.

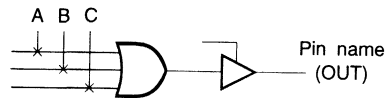


Figure 12.

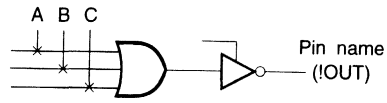


Figure 13.

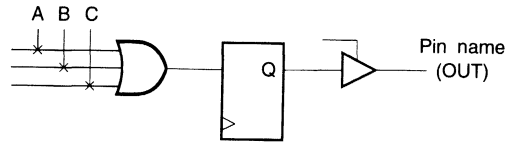
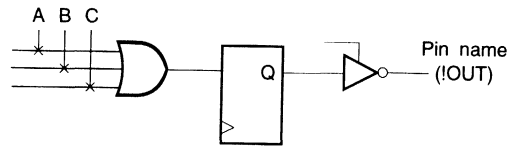


Figure 14.



Polarity Control for Atmel's Flash 16V8 and 20V8 Devices

This section discusses the ABEL™ and CUPL™ syntax for devices with fixed inverting output buffers and output polarity control such as Atmel's Flash 16V8 and 20V8 devices.[1]

Configuring Polarity with ABEL

The following examples have A, B, and C defined as inputs and OUT as the output. Only ISTYPE 'Com' for combinatorial or ISTYPE 'Reg' for registered outputs should be used.[2] This allows ABEL to optimize the logic to generate an implementation with the fewest number of product terms.

Case 1: (Combinatorial - High-True Output)

```
Declaration
OUT pin 14 ISTYPE 'Com';

Equations
OUT = A # B # C;
```

The compiler will pick Figure 15 to implement the logic. To make the output high-true, the compiler will invert the logic twice to obtain correct output polarity.

Case 1a: (Combinatorial - Low-True Output)

```
Declaration
OUT pin 14 ISTYPE 'Com';

Equations
!OUT = A # B # C; "Equivalent to Out = !A & !B & !C
```

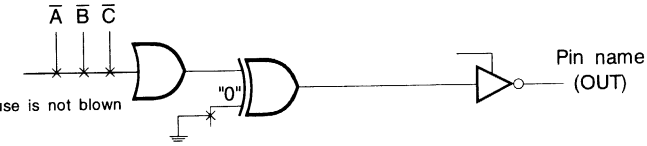
The compiler will pick Figure 16 to implement the logic. To make the output low-true, put a "!" in front of OUT in the logic equations section. The compiler will invert the logic three times to obtain the correct output polarity.

Case 2: (Registered - High-true Output)

```
Declaration
OUT pin 14 ISTYPE 'Reg'; "The 'Reg' ISTYPE should
  be used

Equations
Out := A # B # C ; "':=' is required to specify a
  Registered Output
OUT.clk = clk;
OUT.ar = AR;
```

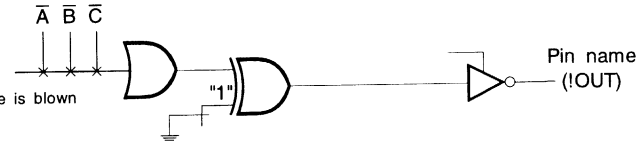
The compiler will choose Figure 17 to implement the logic. To make the output high-true, the compiler will invert the logic twice to obtain the correct output polarity.

Figure 15.



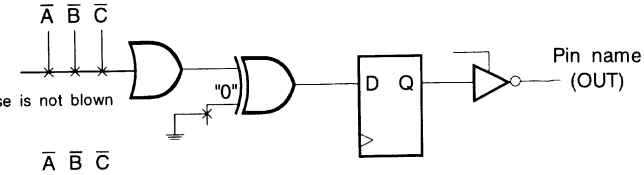
XOR Polarity Fuse is not blown

Figure 16.



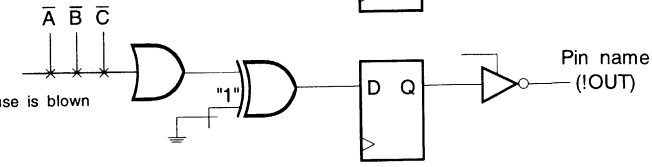
XOR Polarity Fuse is blown

Figure 17.



XOR Polarity Fuse is not blown

Figure 18.



XOR Polarity Fuse is blown

Notes:

1. Because of the fixed inverting outputs, all flip-flops for these devices will reset during power up or through Asynchronous Reset logic to a "High" or "1" state regardless or how the logic is implemented.
2. The compiler will not compile correctly if the ISTYPE such as 'Reg_D', 'Buffer', 'Invert', 'Pos' or 'Neg' are used.

Case 2a: (Registered - Low-True Output)

```
Declaration
OUT pin 14 ISTYPE 'Reg';

Equations
!OUT := A # B # C; "Equivalent to OUT.d = !A & !B &
!C
OUT.clk = clk;
OUT.ar = AR;
```

The compiler will choose Figure 18 to implement the logic. To make the output low-true, put a "!" in front of OUT in the logic equations section. The compiler will invert the logic three times to obtain the correct output polarity.

Configuring Polarity with CUPL

Polarity is controlled in CUPL at the pin declaration, just like other Atmel PLD and CPLD devices. CUPL will optimize the logic equations to match the pin polarity.[1]

Case 1: (Combinatorial - Active High)

```
Pin 14 = OUT
OUT = A # B # C;
```

The compiler will choose Figure 19 to implement the logic. The pin polarity on the pin declaration indicates an active high output, CUPL will invert the logic twice to obtain the correct output polarity.

Case 1a: (Combinatorial - Active Low)

```
pin 14 = OUT
OUT = A # B # C;
```

The compiler will choose figure 20 to implement the logic. The "!" on the OUT pin declaration indicates that an active low output is required. CUPL will invert the logic once to obtain the correct output polarity.

Case 2: (registered - Active High)

```
Pin 14 = Out;
OUT.d = A # B # C;
OUT.ck = clk;
OUT.ar = AR;
```

The compiler will choose Figure 21 to implement the logic. CUPL will invert the logic twice to obtain the correct output polarity.

Case 2a: (Registered - Active Low)

```
Pin 14 = !Out;
OUT.d = A # B # C;
OUT.ck = clk;
OUT.ar = AR;
```

The compiler will choose Figure 22 to implement the logic. The "!" on the OUT pin declaration indicates that an active low output is required. CUPL will invert the logic once to obtain the correct output polarity.

Figure 19.

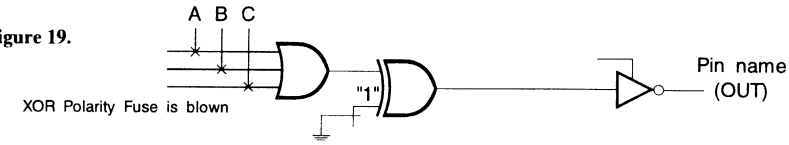


Figure 20.

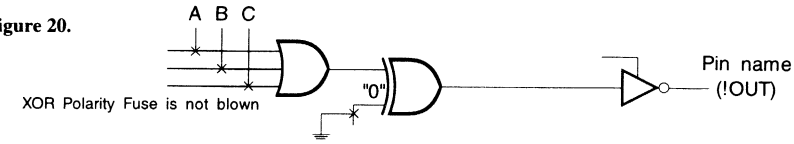


Figure 21.

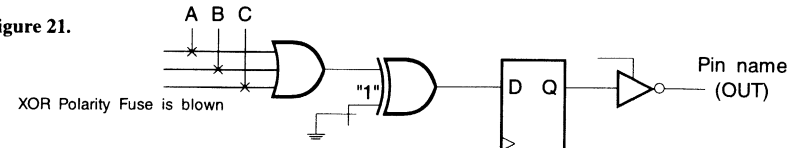
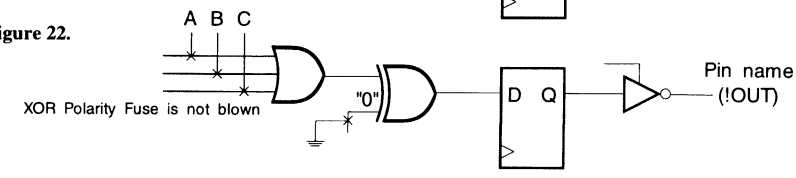


Figure 22.



Note: 1. Because of the fixed inverting outputs, all flip-flops for these devices will reset during power up or through Asynchronous Reset logic to a "High" or "1" state regardless or how the logic is implemented.

Atmel PLDs' Architectures Simplify Timing Calculation

Introduction

This application note shows different graphical timing models that can help the user visualize the A.C. timing of the various Atmel PLD families of devices. Because of their deterministic and path-independent delays, timing calculation becomes straight forward.

Atmel PLDs have regular AND-OR architecture which simplifies timing calculation. All the A.C. timing parameters are clearly stated in the data book. Even for complex designs it only takes a few minutes to calculate the delays by hand.

If the design engineer has access to tools such as the Atmel-ViewPLD, he/she can easily predict the performance of the PLD. PLD software packages with timing simulation capabilities let the design engineer know the performance of the PLD immediately after the design is entered and check the results of the timing simulator and quickly modify the design to meet the system timing requirements. Atmel offers a complete design entry package called Atmel-ViewPLD that has such a timing simulator.

Architectures/Timing Models

The AT22V10 represents the classic PAL™-type architecture with the programmable AND and fixed OR structure. A very small set of A.C. timing parameters can describe all the delays that occur in the implementation of register and combinatorial logic as shown in Figure 1.

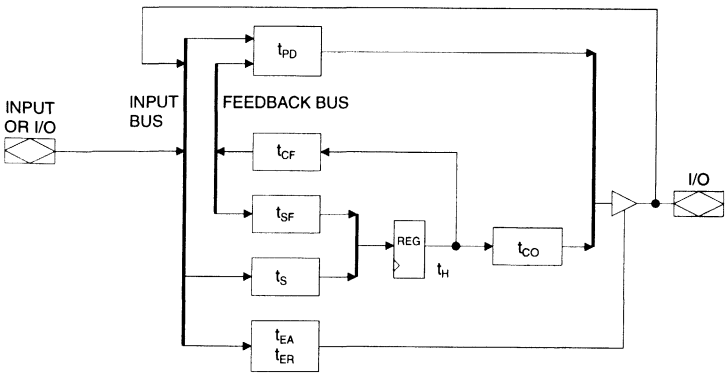
For example, an output is described in the following Boolean equation:

OUTPUT = A0 & !A1 & A2 # SELECT;

A0, A1, A2, and SELECT can be inputs or I/Os and the delay will be simply the time for the signal to propagate from a pin through the AND-OR array, the macrocell, and to the output pin. This is described by the A.C. parameter t_{PD}.

The ATV750/ATV750B and ATV2500/ ATV2500B, with more advanced macrocells, maintain the same AND-OR structure as the AT22V10. Because of this, they can also be described by the same AT22V10 timing model. Even when using the buried registers found in the ATV750/ATV750B and ATV2500/ ATV2500B, the method of calculation for delays stays the same. For ex-

Figure 1. AT22V10, ATV750, ATV750B, ATV2500 and ATV2500B Timing Model



0239B

ample, an ABEL™ description of a binary counter may look like:

COUNT.d = COUNT.fb + 1;

The counter can be implemented using only the internal buried registers of the ATV750, ATV750B, ATV2500 or ATV2500B. In this case the minimum cycle time will be equal to t_{CF} *(clock to feedback)* + t_{SF} *(feedback setup)*. See Figure 2. This is also equal to $1/(F_{MAX}$ *internal)*.

Figure 3 shows the registered data path for a pin-to-pin delay, as might be described by output logic:

REG_A.d = A1 & B1 & !C1;

If A1, B1, and C1 are all signals from either input or I/O pins, then the minimum cycle time will be t_S *(setup time for input or I/O pin)* + t_{CO} *(clock to output)* which is equal to $1/(F_{MAX}$ *external)*.

Figure 4 shows how data propagates for a typical Mealy state-machine, in which the state bits are inputs to combinatorial outputs:

COUNT.d = (COUNT.FB +1);

FULL = (COUNT.FB == ^HFF);

In this case, it will take FULL the delay of t_{CF} + t_{PD} to go from the rising edge of the clock driving the counter to the changing of FULL's output value.

Figure 5 is based upon Figure 1 with the addition of a few A.C. parameters to help describe the new features of the ATV5000 and ATV5100.

These devices have both synchronous and asynchronous modes of operation. With the addition of the synchronous clocking option, the devices perform at a higher clock rate. The A.C. parameters have either the suffix of "S" (synchronous) or "A" (asynchronous) to distinguish the two registered clocking options.

Input latch setup and hold time are additional requirements when the latch is used. If the latch is bypassed, no delay is added.

For these devices, the t_{PD} parameter is broken down further to show different delay paths separately. T_{PD1} and t_{PD2} are similar to the traditional t_{PD} parameter. T_{PD1} is the delay from any pin to any combinatorial output. T_{PD2} is the delay from internal feedback nodes to a combinatorial output pin.

T_{PD3} is the delay from a pin to an internal combinatorial feedback.

Figure 2. *$1/(F_{MAX}$ internal)*

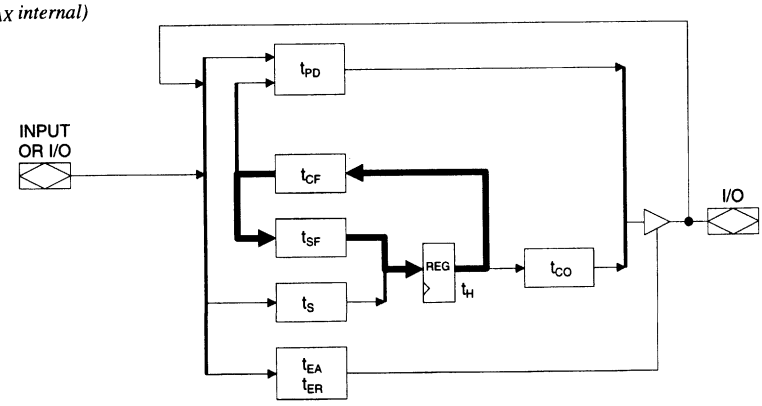
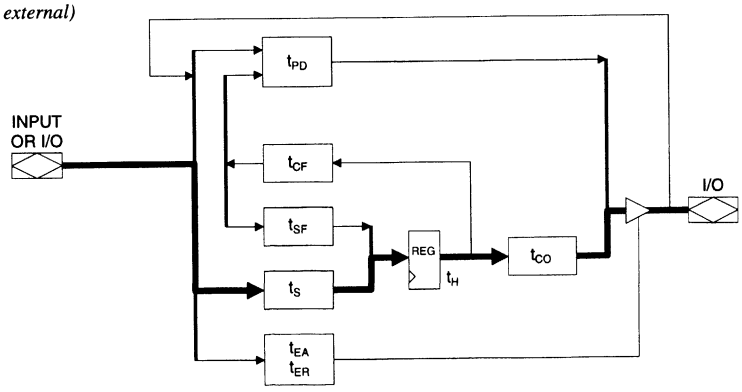


Figure 3. *$1/(F_{MAX}$ external)*



T_{PD4} is the delay from an internal feedback, through the AND/OR array, to an internal combinatorial feedback.

The ATV5000 and ATV5100 Buried Logic Cells let the user configure internal combinatorial or registered feedbacks. Having a combinatorial feedback enables the designer to expand the logic without sacrificing any I/O pins. Also, the B sum term feedbacks in the ATV5000 and ATV5100 can take regional array inputs and make them available to other quadrants.

The most straightforward way to determine the delays is to look at the documentation generated by PLD software after the design has been reduced and fitted. If a reduced equation looks like:

OUTA = WATCHDOG "Product term 1
# A1 & A2 & A3 "Product term 2
# C_OUT;"Product term 3

1. Determine whether the logic is registered or combinatorial.
2. Determine whether OUTA is an internal node or an output pin.

Figure 4. Mealy Machine Delay Path

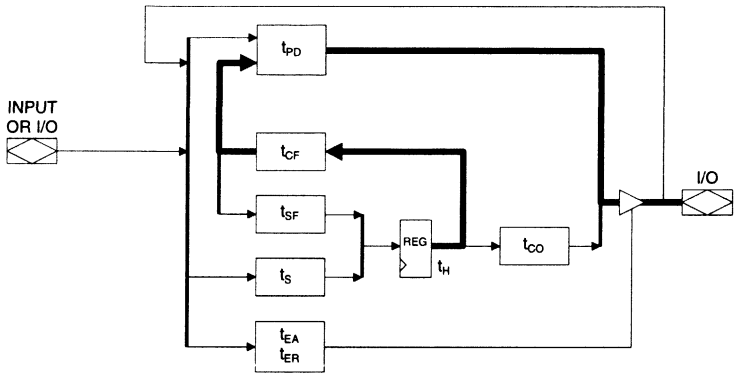
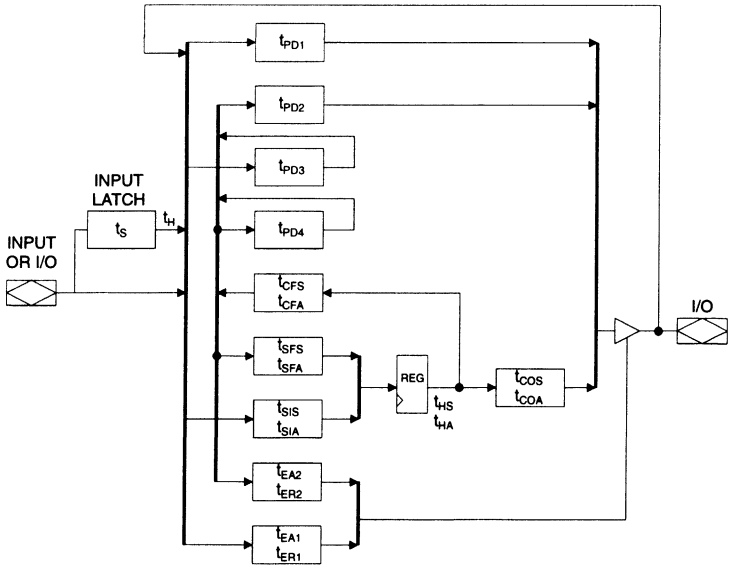


Figure 5. ATV5000 and ATV5100 Timing Model



6

3. Find the source of each of the components that makes up the product terms.

To analyze the various cases, let's assume the following:

1. OUTA is combinatorial. We will look at OUTA implemented on an output pin versus OUTA implemented on a combinatorial node.
2. WATCHDOG is an internal registered node, A1 through A3 are directly from the inputs, and C_OUT is an internal combinatorial node (this covers all signal sources).

Table 1 summarizes the various timing requirements.

Case 1 (Figure 6) is the typical Mealy state machine where the internal state registers are decoded to form a combinatorial output. The total delay from clock to output is $t_{CF} + t_{PD2}$.

Case 2 is the pin-to-pin delay. The A.C. parameter for that is t_{PD1}.

Case 3 is an internal combinatorial feedback's delay from the AND/OR array to the output pin: t_{PD2}.

Case 4 is a "buried Mealy" where the internal state registers are decoded but not placed on an output pin. Instead the result is implemented on an internal combinatorial node where the logic is only useful internal to the design.

Case 5 is the delay from pin to internal combinatorial feedback: t_{PD3}.

Case 6 is the delay from one internal combinatorial node to another internal combinatorial node.

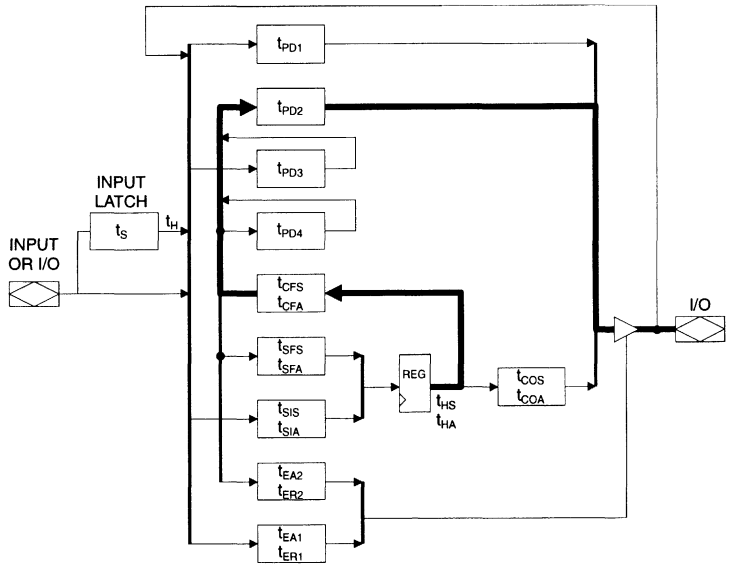
Conclusion

The graphical representation of the A.C. timing models illustrate how simple it is to determine the performance of logic implemented in a Atmel PLD. Atmel complex PLDs, even with their high pin counts and advanced features, have simple timing calculation. They aren't any harder to use than a common AT22V10.

Table 1.

	Registered Feedback P.T. 1	Input from Pins P.T. 2	Internal Combinatorial Node P.T. 3
Combinatorial Output OUTA	Case 1: $t_{CF} + t_{PD2}$	Case 2: t_{PD1}	Case 3: t_{PD2}
Combinatorial Node OUTA	Case 4: $t_{CF} + t_{PD4}$	Case 5: t_{PD3}	Case 6: t_{PD4}

Figure 6. Typical Mealy State Machine



ATV2500 Application Example: Video Frame Grabber

Programmable Logic Device

Application Note

Introduction

This application note shows how the ATV2500 can be used to incorporate multiple control or logic functions into a single programmable logic device. The design example which is used is a simple NTSC video frame grabber. The ATV2500 is used to generate all of the control and addressing for the frame grabber. The application note includes a description of the frame grabber design and implementation using the ATV2500. The ABEL™ source code for the ATV2500 is included for reference and is also available from the PLD applications group on floppy disk.

ATV2500 Description

The ATV2500 is a high density programmable logic device which features 24 I/O pins and 14 input-only pins. Each I/O pin is associated with a logic macrocell (see Figures 1 and 2). The output can be configured as either combinatorial or registered. Each macrocell contains two flip-flops, 12 product terms which can be split into three separate sum terms, and an output enable. Each flip-flop has a clock term and an asynchronous reset term. Groups of four or eight flip-flops each have a common synchronous preset product term.

Each macrocell has a feedback path from the pin and from each register. This makes it possible to bury both registers and use the pin for either a combinatorial output or an input pin. A global bus routes all pins and register feedbacks to every logic cell.

Frame Grabber Design Considerations

The basic idea behind a frame grabber is to sample and store a frame of video data. Once the data is stored, it can be re-displayed, enhanced or saved to a file. In this example, the input video signal is converted with an A/D converter and stored in RAM. To display the

Figure 1. ATV2500 Output Logic, Registered [1]

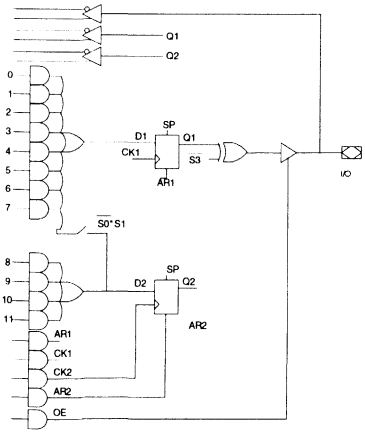
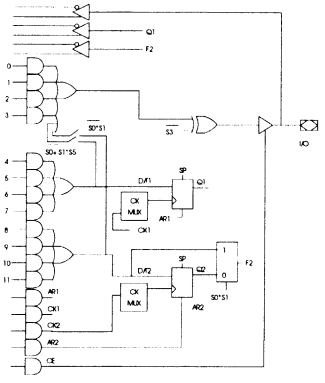


Figure 2. ATV2500 Output Logic, Combinatorial [1]



Note: 1. This diagram shows equivalent logic functions, not necessarily the actual circuit implementation.

0251B

buffered data, the RAM addresses are cycled and the data is converted back to a video signal through a D/A converter.

Video Basics

The NTSC (National Television Standards Committee) composite video signal is the standard used by most television and video systems in North America. The signal is composed of four components: luminance (brightness), chrominance (color), audio and synchronization. An NTSC video image or *frame* is composed of 525 scan lines. Each frame is actually divided into two *fields* of 262.5 scan lines which are interlaced. The fields start with a vertical sync period followed by the scan lines (see Figure 3). Each scan line consists of a horizontal sync period, color burst and video information (see Figure 4).

Timing

The frame grabber samples the entire video frame, including the horizontal and vertical sync periods. Then, in order to generate a video image from the stored data, the data is simply converted back to an analog signal at the same rate it was sampled.

The refresh rate for each field is 59.94 Hz (16.683 ms per field), which means the refresh rate for the whole frame is 29.97 Hz (33.366 ms per frame). The number of bits in each sample and the sampling frequency determine the resolution of the reconstructed video image. An 8-bit sample size was chosen for this example since 8-bit A/D converters are readily available. An 8-bit sample size will allow 256 levels of intensity, which is plenty for the purposes of this design. In order to generate a reasonable image, the sample frequency should be at least twice the NTSC color burst frequency of 3.579545 MHz. A sample frequency of 7.5 MHz was chosen, which is a little more than twice the color burst frequency.

The total number of samples required for each frame will be 253245 (*7.5 MHz x 16.683 ms x 2*).

Interface

The user interface consists of a single button. When the button is depressed, the frame grabber will pass the video signal through to the output. When the button is released, the data is sampled. The converted video signal is monitored to detect a vertical sync. Once the vertical sync is detected, 253245 samples from the video input are stored. Following the sampling, the addresses are continuously cycled creating a frozen image. The captured frame will be displayed until the button is depressed again, causing another frame of data to be sampled and stored.

It is not necessary to start sampling during the vertical sync period since 253245 samples will contain an entire frame. As the addresses are cycled, the vertical sync portion of the video signal will be generated every 16.683 ms. However, if the data were used for any purpose other than just display, it would be more convenient to have the data start at a known point in the video signal.

Frame Grabber Implementation

The schematic for the frame grabber is shown in Figure 5. The three basic functions are: D/A and A/D conversion, control and address generation, and storage for the sampled data.

For the A/D and D/A conversions, the Samsung KSV3100A was selected. It has both an 8-bit A/D converter and 10-bit D/A converter, along with the necessary pre-amplifier and input clamping circuit in a single device. The KSV3100A device is connected as in the recommended operating circuit in the data sheet. The 7.5 MHz system clock is used as the clock for both the A/D and D/A conversions.

The ATV2500 is used to implement all of the control and addresses for the frame grabber. The functions include a vertical sync detector, a control state machine and a RAM address counter. It receives the mode signal from the switch, the 8-bit data bus from the A/D converter and the 7.5 MHz system clock signal. It generates the bus control signals and 18-bit address for the RAM.

A 256K x 8 static RAM module is used for the frame buffer memory. A write enable signal from the controller allows the

Figure 3. Field Timing

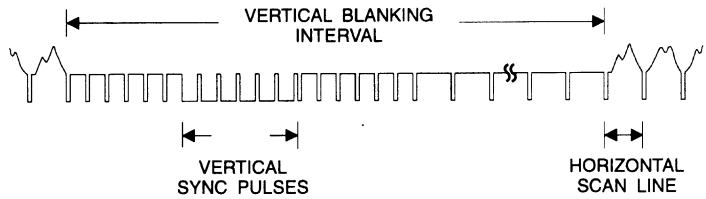
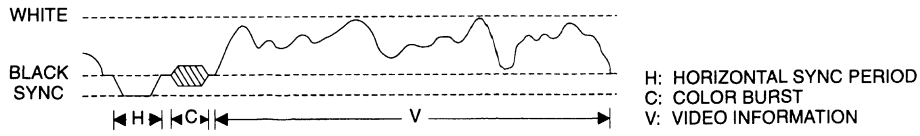


Figure 4. Horizontal Scan Line



converted data to be stored in the RAM during sampling. An output enable signal is used to enable/disable the RAM onto the data bus. External buffers are used to enable the data from the output of the A/D back into the D/A when the video signal is passed through or the data is being sampled.

ATV2500 Control and Address Functions

The ATV2500 is used to implement the control and address functions. These include a vertical sync detector, a control state machine and the RAM address counter. Figure 6 shows a block diagram of the ATV2500 functions.

Vertical Sync Detector

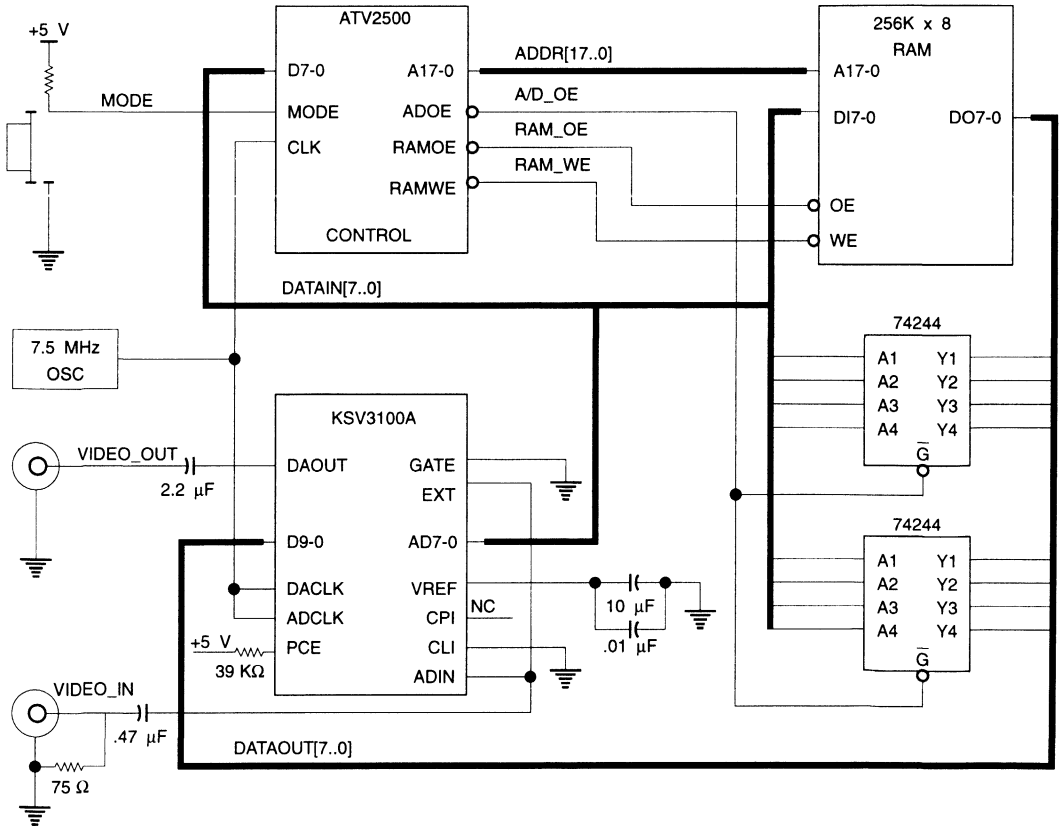
During the horizontal and vertical sync periods, the signal drops to a sync level which is lower than any other portion of the signal. This level will be clamped in the A/D converter and will become the zero value when it is converted. The horizontal sync pulse is about 4.7 µs, which will correspond to about 35 samples. The entire vertical sync period is 20 times the horizontal scan width. Within that period, there are pulses of around 31 ms when the signal is at the sync level. Each of these pulses will correspond to about 238 samples.

The vertical sync detector is a 7-bit counter which will count every sample with a zero value. If it counts 128 such samples, then it has detected one of the pulses in the vertical sync period. The counter is divided into two parts, so that the maximum number of product terms required for any count bit is four. A carry bit from the first stage is used to enable the second stage. The counter will increment whenever the input data is zero. A non-zero value will cause the counter to reset. When the count reaches 127, the VS signal is asserted.

State Machine

A state machine generates internal control for the address generation and external control signals for the RAM. The state dia-

Figure 5. Frame Grabber Schematic



gram is shown in Figure 7. When the MODE input changes, indicating that the frame grabber should sample a new frame, the state machine waits for the VS signal. After the vertical sync is detected, it sets up the control signals to write the sampled data for the entire frame. When the address counter reaches the correct number of samples, the state machine changes the control signals to read the sampled data. The addresses are cycled so that the sampled frame is continuously displayed.

Address Counter

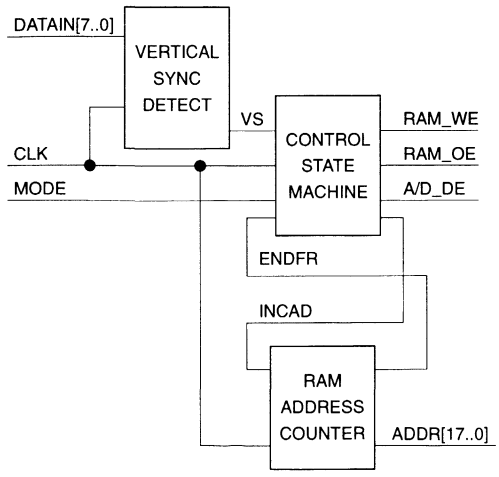
The address counter is controlled by the INCAD control signal from the state machine. If the INCAD signal is asserted, the address will increment until the counter reaches the final address for the correct number of samples. When the INCAD signal is not asserted, or the final address is reached, the counter resets to 0. The 18-bit address counter is broken into two 9-bit stages, so that the maximum number of product terms required for each count bit is less than 12. A carry from the first stage is used to enable to second stage.

Resource Allocation

The address counters use registered I/O pins in the ATV2500. The MSBs of each stage of the counter have more than eight product terms, so they require an entire macrocell. The LSBs of each stage use less than eight product terms, so a buried register is available in each of those macrocells (see Figure 1). The control bits generated by the state machine use combinatorial outputs with less than four product terms, so two buried registers are available in each of those macrocells (see Figure 2). The state bits and vertical sync detect counter bits are assigned to available buried registers.

Assignment of the I/O pins is only dependent on the board layout, since there are no signal routing limitations in the ATV2500. Buried logic can be assigned to any available resources. Table 1 shows a worksheet used to allocate the logic functions in this application to the ATV2500 resources. The shaded boxes indicate resources which are used by another signal generated in the same macrocell. The empty boxes indicate available resources. In this design, four input pins, one I/O pin and associated macrocell plus 13 additional buried registers are available for expansion or design changes.

Figure 6. ATV2500 Function Block Diagram



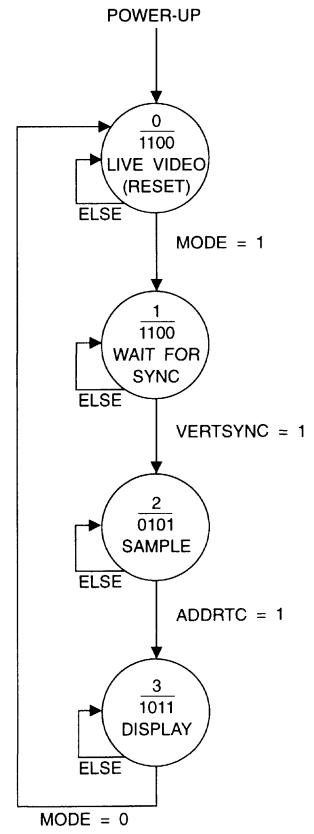
Notes on Test Vectors

In order to test that the address counter rolls over at the correct count, more than 253245 test vectors would be required, which far exceeds the number of vectors allowed in ABEL™. There are a few ways to get around this problem.

The first method is to use the register preload function in PLASIM™. The counter can be preloaded with a count near to the maximum count, and then allowed to roll over. However, since JEDSIM™ does not support the preload function the JEDEC file is not checked.

Another method is to change the terminal count value to a smaller value, so that the counter would reach the terminal

Figure 7. Controller State Diagram



Note: Outputs: RAMWE, RAMOE, ADOE, INCAD

count in fewer vectors. Since the equations are altered, this method could only be used for ABEL™ simulation.

A third method is to use the register synchronous presets to load the counter. This is the method that was used in this design. The registers which use the preset are allocated to the same ATV2500 synchronous preset groups. A spare input pin (PRELD) is used to control the preset in the test vectors. Using this method, the vectors can also be used on the programmer.

Summary

In this example, the address and control functions are greatly simplified by using a single complex programmable logic device. The ATV2500 is ideal for this application since it has enough inputs to accept the control and data signals, and the necessary I/Os to generate the RAM addresses and control. The ability to combine or separate the sum terms in each macrocell allows for maximum usage of the available resources. The functions which require large numbers of product terms do not have to be split into smaller pieces. The functions which require fewer numbers of product terms do not waste an entire macrocell. The leftover buried logic in those macrocells can be used for the control state machine and the vertical sync detector.

Table 1. ATV2500 ABEL Pin/Node Assignment Worksheet Example

Input	Signal	Input	Signal
1	CLK	21	D4
2	MODE	22	D5
3		23	D6
17	DO	37	D7
18	D1	38	
19	D2	39	
20	D3	40	(PRELD)

I/O	Signal	Q2	Signal	Q1	Signal
4	A0	41	SYNC0	217	
5	A1	42	SYNC1	218	
6	A2	43	SYNC2	219	
7	A3	44	SYNC3	220	
8	A4	45	SYNCARRY	221	
9	A5	46	SYNC4	222	
11	A8	47		223	
12	A10	48		224	
13	A6	49	SYNC5	225	
14	A7	50	SYNC6	226	
15	A9	51	ENDFR	227	
16	A13	52	ADCARRY	228	
24	A11	53		229	
25	A12	54		230	
26	A14	55		231	
27	A15	56		232	
28	A16	57		233	
29	A17	58		234	
31	VS	59	ST0	235	
32	RAMWE	60	ST1	236	
33	RAMOE	61		237	
34	ADOE	62		238	
35	INCAD	63		239	
36		64		240	

ABEL™ Source Code

```
module CONTROL ;
title 'Application example for the ATV2500 - Frame Grabber Controller
Atmel Corporation PLD - (408)436-4333 PLD Applications Hotline
Wendey Mueller - January 10, 1992'

CONTROL device 'P2500';

CLK,MODE              pin 1,2; "system clock and mode signal from button
D0,D1,D2,D3           pin 17,18,19,20; "digitized video signal from A/D
D4,D5,D6,D7           pin 21,22,23,37;

A0,A1,A2,A3,A4        pin 4,5,6,7,8 istype 'reg,buffer'; "RAM address outputs
A5,A6,A7,A8,A9        pin 9,13,14,11,15 istype 'reg,buffer';
A10,A11,A12,A13,A14   pin 12,24,25,16,26 istype 'reg,buffer';
A15,A16,A17           pin 27,28,29 istype 'reg,buffer';
RAMWE,RAMOE           pin 32,33 istype 'com,buffer'; "RAM control signals
ADOE,INCAD            pin 34,35 istype 'com,buffer'; "address counter control
VS                    pin 31 istype 'com,buffer';    "vertical sync detected

ADCARRY,SYNCARRY      node 52,45 istype 'reg,buffer'; "counter carry signals
ENDFR                 node 51 istype 'reg,buffer';    "end of frame detected
ST0,ST1               node 59,60 istype 'reg,buffer'; "state bits
SYNC0,SYNC1,SYNC2     node 41,42,43 istype 'reg,buffer';
SYNC3,SYNC4,SYNC5     node 44,46,49 istype 'reg,buffer'; "vertical sync detect
SYNC6                 node 50 istype 'reg,buffer';       "counter

"Use spare input pin as preset signal for testing counter

PRELD                 pin 3;

C,X,Z,H,L,P = .C.,.X.,.Z.,1,0,.P.;

"Create buses

DATA   = [D7..D0];        "data bus
ADDR   = [A17..A0];       "address counter
ADDRA  = [A8..A0];        "address counter LSB
ADDRB  = [A17..A9];       "address counter MSB
SYNC   = [SYNC6..SYNC0];  "vertical sync detect counter
SYNCA  = [SYNC3..SYNC0];  "vertical sync detect counter LSB
SYNCB  = [SYNC6..SYNC4];  "vertical sync detect counter MSB
STMACH = [ST1,ST0];       "state bits

"Define states

S0  = [0,0];
S1  = [0,1];
S2  = [1,0];
S3  = [1,1];

EQUATIONS

"256K address counter - increment when INCAD is true and address
"                       has not reached end of frame, otherwise reset

ADDRA.D = ((ADDRA.FB + 1) & INCAD & !ENDFR); "LSB stage
ADDRA.CK = CLK;

ADCARRY.D = (ADDRA.FB == 510); "synchronous carry bit from 1st stage
ADCARRY.CK = CLK;
```

```
ADDRB.D = ((ADDRB.FB + 1) & INCAD & !ENDFR & ADCARRY) "MSB stage
        # (ADDRB.FB & INCAD & !ENDFR & !ADCARRY);
ADDRB.CK = CLK;

ENDFR.D = (ADDR.FB == 253243); "set ENDFR when address reaches 253243
ENDFR.CK = CLK;

"Use synchronous preset to simplify testing the address counter by
"preloading it with a value close to the last address.

A17.SP = PRELD;
A16.SP = PRELD;
A15.SP = PRELD;
A14.SP = PRELD;
A12.SP = PRELD;
A11.SP = PRELD;
A10.SP = PRELD;
A8.SP  = PRELD;

"Vertical sync detect counter - increment if data is 0, otherwise reset

SYNCA.D = (SYNCA.FB + 1) & (DATA == 0); "LSB stage
SYNCA.CK = CLK;

SYNCARRY.D = (SYNCA.FB == 14); "synchronous carry bit from 1st stage
SYNCARRY.CK = CLK;

SYNCB.D = (SYNCB.FB + 1) & (DATA == 0) & SYNCARRY  "MSB stage
        # SYNCB.FB & (DATA == 0) & !SYNCARRY;
SYNCB.CK = CLK;

VS = (SYNC.FB == 127); "set vertical sync detected bit if count reaches 128

STMACH.CK = CLK;

"State Machine Controller -
"
"Inputs: MODE,VS,ENDFR
"Outputs: RAMWE,RAMOE,ADOE,INCAD

STATE_DIAGRAM STMACH

STATE S0:                       "Reset, live video
   RAMWE = 1;
   RAMOE = 1;
   ADOE = 0;
   INCAD = 0;
   IF (MODE) THEN S1            "If capture mode, go to state 1
   ELSE S0                      "else wait for mode change

STATE S1:                       "Wait for vertical sync signal
   RAMWE = 1;
   RAMOE = 1;
   ADOE = 0;
   INCAD = 0;
   IF (VS) THEN S2              "Vertical sync detected, start sampling data
   ELSE S1                      "else wait for vertical sync

STATE S2:                       "Sample video data
   RAMWE = 0;
   RAMOE = 1;
   ADOE = 0;
```

```
   INCAD = 1;
   IF (ENDFR) THEN S3          "Frame capture complete
   ELSE S2                     "else continue sampling

STATE S3:                      "Display frame data
   RAMWE = 1;
   RAMOE = 0;
   ADOE = 1;
   INCAD = 1;
   IF (!MODE) THEN S0          "Reset, display live video
   ELSE S3                     "else continue to display frame data

@RADIX 16;
@CONST ACNT = 1;
@CONST SCNT = 0;

TEST_VECTORS (
[CLK,MODE,DATA,PRELD] - [SYNC,VS,STMACH,RAMWE,RAMOE,ADOE,INCAD,ADDR, ENDFR])

"check that the vertical sync detector resets if data is not 0 and set mode
"to start sample and display sequence
[ 0,  0,  0,   0    ] - [00,  0, 0,     1,    1,    0,   0,    00000,0    ];
[ C,  0,  0,   0    ] - [01,  0, 0,     1,    1,    0,   0,    00000,0    ];
[ C,  0,  1,   0    ] - [00,  0, 0,     1,    1,    0,   0,    00000,0    ];
[ C,  1,  1,   0    ] - [00,  0, 1,     1,    1,    0,   0,    00000,0    ];

"simulate vertical sync
@REPEAT 7E {
@CONST SCNT = SCNT + 1;
[ C,  1,  0,   0    ] - [SCNT,0, 1,     1,    1,    0,   0,    00000,0    ]; }
[ C,  1,  0,   0    ] - [7F,  1, 1,     1,    1,    0,   0,    00000,0    ];
[ C,  1,  0,   0    ] - [00,  0, 2,     0,    1,    0,   1,    00000,0    ];
[ C,  1,  0,   0    ] - [01,  0, 2,     0,    1,    0,   1,    00001,0    ];

"state machine has detected vertical sync and started sampling.
@REPEAT 0FE {
@CONST ACNT = ACNT + 1;
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    ACNT, 0    ];}
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    00100,0    ];
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    00101,0    ];

"Use preset to preload a count value near the largest address value.
[ C,  1,  1,   1    ] - [00,  0, 2,     0,    1,    0,   1,    3DD02,0    ];
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    3DD03,0    ];

"Allow counter to reach the largest address and roll over. State machine
"then changes controls to display sampled data.
@CONST ACNT = 3DD03;
@REPEAT 037 {
@CONST ACNT = ACNT + 1;
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    ACNT, 0    ];}
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    3DD3B,0    ];
[ C,  1,  1,   0    ] - [00,  0, 2,     0,    1,    0,   1,    3DD3C,1    ];
[ C,  1,  1,   0    ] - [00,  0, 3,     1,    0,    1,   1,    00000,0    ];
[ C,  1,  1,   0    ] - [00,  0, 3,     1,    0,    1,   1,    00001,0    ];
[ C,  1,  1,   0    ] - [00,  0, 3,     1,    0,    1,   1,    00002,0    ];

END ;
```

ATV5000 Application Example: DMA Controller

Programmable Logic Device

Application Note

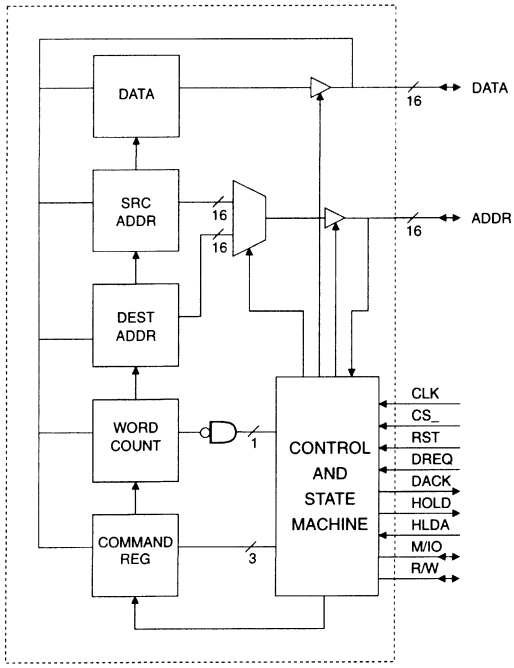
Introduction

This application note shows how the ATV5000 complex programmable logic device can be used to implement a simple DMA Controller. It includes a description of the DMA controller function and the implementation using an ATV5000. The ABEL™ source code is included for reference, and is also available from the factory on floppy disk.

A Direct Memory Access (DMA) controller is a peripheral device used in a CPU system to perform block data transfers between memories and I/O devices. It generates the addresses and control necessary to perform the transfer. The DMA controller improves system performance by transferring data directly between devices instead of using the CPU.

The ATV5000 is a high-density programmable logic device, featuring 52 I/O logic cells and 128 flip-flops. This application takes advantage of the buried registers to store and increment or decrement the addresses and word count. The counters are easily implemented with minimal logic by using T-type registers. The high I/O count can easily accommodate the 16-bit bi-directional data and address buses.

Figure 1. Internal Block Diagram



0482A

6

DMA Controller Description

The DMA controller is used to transfer blocks of data between system memory and other memory or I/O devices. Figure 1 shows the basic block diagram for the DMA controller. The interface to the CPU consists of an address bus, a data bus, and some control signals. These signals are used by the CPU to load initialization data into the DMA controller registers. When the DMA controller is granted control of the buses, the same signals are used to transfer the data. This example uses i386™ type bus control signals. Figure 2 shows how this DMA controller would be used in a CPU system.

The transfer is initiated when the CPU loads the starting source and destination addresses, word count, and control word into the DMA controller registers. The external device asserts the DMA request signal to request a DMA. The DMA controller then requests control of the system buses and control signals. When the CPU grants the bus request, the DMA controller acknowledges the DMA request and starts the DMA.

The data is read in on the data bus and then latched and written back out. The source address or destination address is multiplexed onto the address bus during the read cycle or write cycle. The system bus control signals are used by the DMA controller as control signals for the memory or I/O device. The DMA controller transfers the requested number of words and then relinquishes bus control. The DMA cycle timing is shown in Figure 3.

Figure 2. System Block Diagram

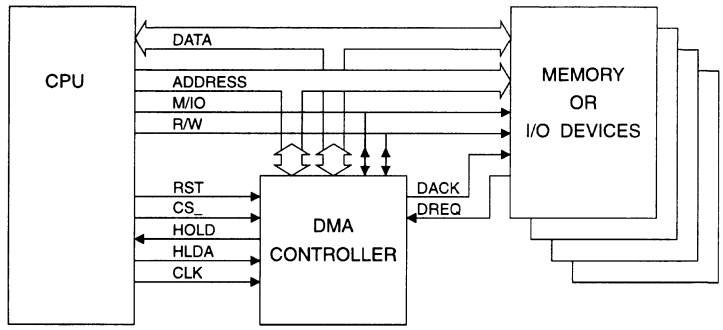
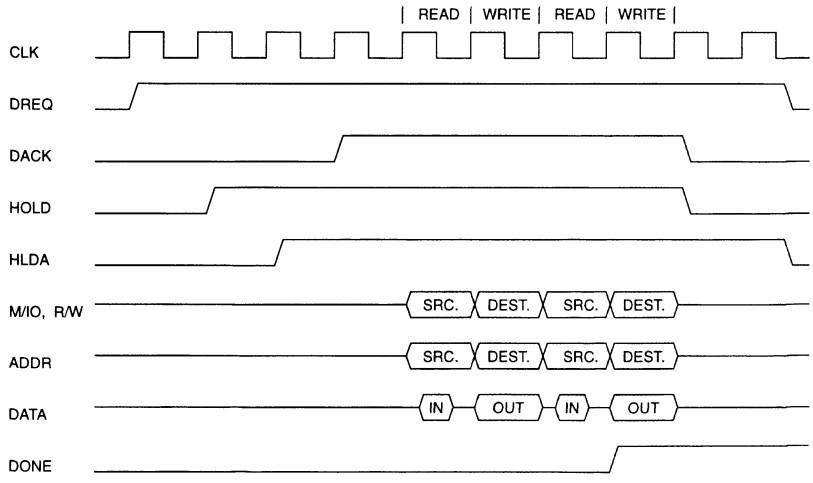


Figure 3. DMA Timing



ATV5000 Description

The ATV5000 is 68-pin high-density programmable logic device, which features 52 I/O pins and eight input-only pins. Each I/O pin is associated with a logic macrocell (see Figures 4, 5, and 6). Each macrocell has an input latch, two flip-flops, 13 product terms which can be split into three separate sum terms, and an output enable term. The I/O pin can be driven with either a combinatorial or registered output. Each flip-flop has a clock term, asynchronous reset term, and asynchronous preset term, and can be configured as either a D-type or T-type flip-flop.

In addition, there are 24 buried logic cells (see Figure 7). Each buried logic cell can be configured as registered or combinatorial. If registered, each flip-flop has a clock term, asynchronous reset term, and synchronous preset term, and can be configured as a D-type or T-type flip-flop.

The ATV5000 is divided into four quadrants with 13 I/O macrocells and six buried logic cells each (see Figure 8). A universal bus routes signals to all four quadrants, and a regional bus routes signals within each quadrant. The regional buses contain the true and false feedback signals from each register, from the buried logic cells, and from the eight input-only pins. The universal bus contains the regional bus inputs plus the true and false signals from each I/O pin.

Figure 4. Logic Cell, Two Buried Registers, Combinatorial to I/O Cell

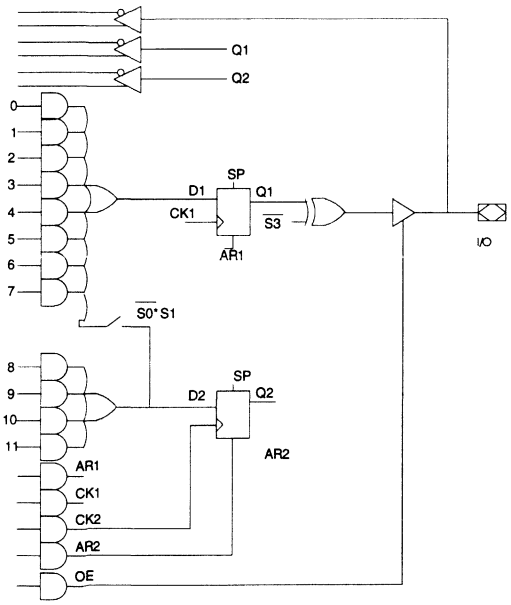


Figure 5. Logic Cell with Combinatorial Sum Terms, Register to I/O Cell

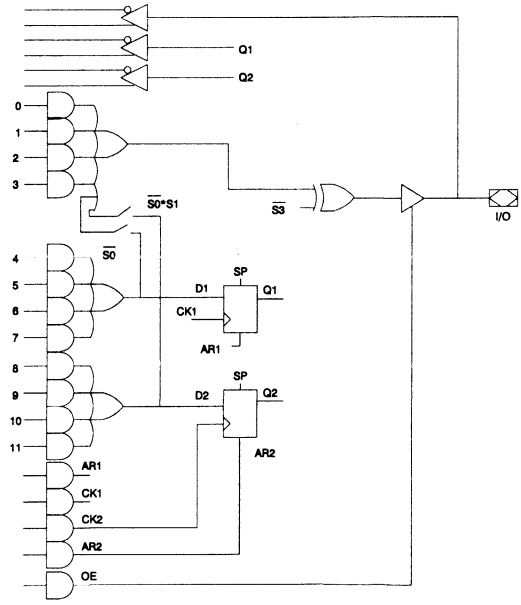


Figure 6. I/O Pin Logic

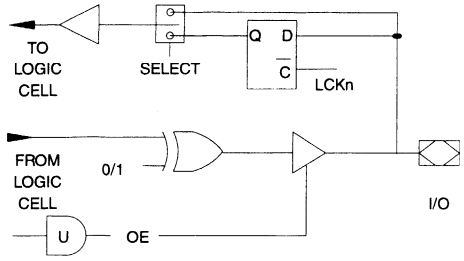


Figure 7. Buried Logic Cells

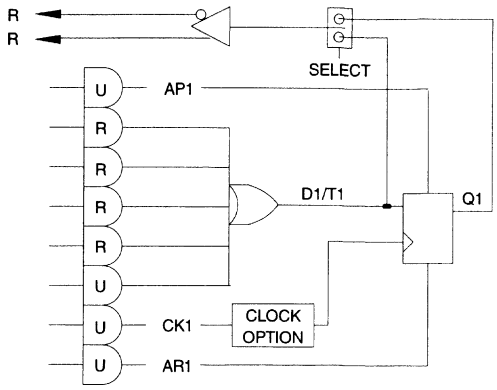
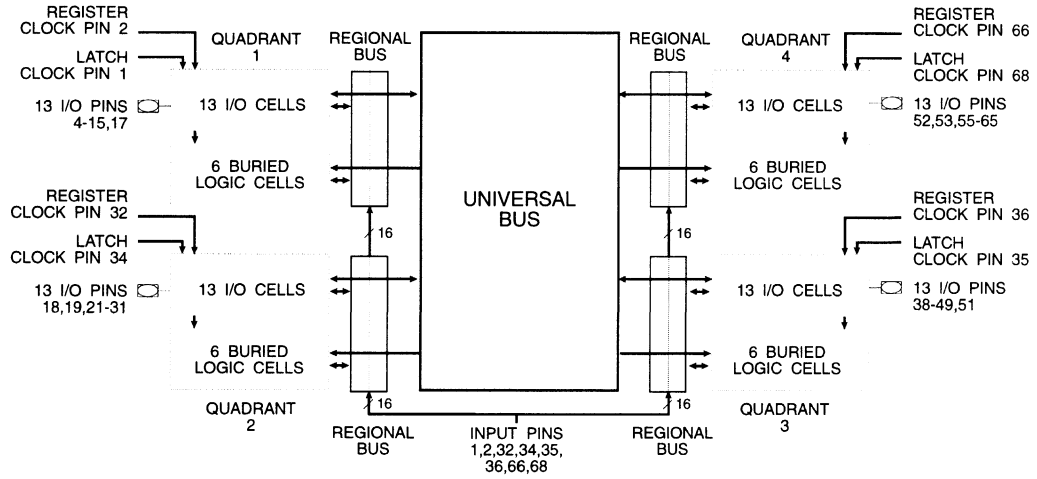


Figure 8. ATV5000 Block Diagram



DMA Controller Implementation

The DMA controller consists of three basic functions: system interface, internal address and word counters, and a state machine controller.

System Interface

The system interface consists of a 16-bit bi-directional data bus, a 16-bit bi-directional address bus, bi-directional bus control signals, and handshaking signals to request bus control.

The data and address buses are assigned to I/O pins in the ATV5000. When the CPU controls the system buses, the buses are used as inputs to receive initialization data. When the DMA controller controls the system buses, the buses are bi-directional. The data bus is tri-stated while the source data is read and registered, and then enabled to write the data to the destination. The address bus outputs are enabled and multiplex the source or destination address onto the bus.

The CLK and RST signals are the CPU system clock and reset signals. The CLK signal is used as the clock for all registers, so that all data transfers are synchronized to the system clock. The CS_ selects whether the DMA controller is being addressed for initialization. Both signals are assigned to input pins in the ATV5000, so that the signals are available on the regional buses in all quadrants.

The M/IO and R/W signals are used to control the bus activity. For initialization, the R/W signal enables a write and the LSB bits of the address bus are decoded to select which register is to be accessed. During a DMA transfer, the M/IO selects the source or destination as an I/O device or a memory and the R/W signal selects either a read or write operation. Both signals are assigned to I/O pins in the ATV5000, since they are used as inputs during initialization and outputs during a DMA cycle.

There are two sets of handshaking signals: the DMA request and acknowledge (DREQ and DACK), and the bus request and acknowledge (HOLD and HLDA). The DREQ and HLDA are assigned to input pins in the ATV5000. The HOLD and DACK signals are assigned to I/O pins in the ATV5000, since they are signals output by the controller.

Address and Word Counters

The address and word counters store the starting addresses, transfer word count, and command word. All use buried registers in the ATV5000, since the data does not need to be directly output. The registers are used as counters which load and then increment or decrement. The load and count functions are controlled by the bus control signals and the state machine.

The registers are configured as T-type flip-flops, so that a minimum number of product terms are required to implement the counter functions. Loading is accomplished by XORing the output of the register with the load data, causing the T flip-flop to toggle if the data does not match.

The outputs of the address registers are multiplexed onto the address bus to provide source and destination addresses for the DMA transfer. After each transfer, the addresses are incremented and the word count is decremented. When the word count reaches zero, the DONE signal is sent to the state machine, indicating that the transfer is complete.

The command word is decoded and used by the state machine to determine what type of DMA will be performed. The data is only used by the state machine, so it can be stored in buried registers in the ATV5000. The word consists of three bits: two bits which indicate whether the source and destination are memory or I/O devices, and a third bit which enables the DMA to start. After the DMA is complete, the enable bit is reset.

State Machine

A state machine provides all of the internal and external control signals for the DMA transfers. It also performs the handshaking for bus access and DMA requests. Figure 9 shows the state diagram for this machine.

The state machine starts in a reset state where it waits for the CPU to initialize a DMA. The next three states perform the handshaking to request bus control and start the DMA. A two-state loop is used to transfer each word. The first state reads the source data and the second state writes the destination data. When the DONE bit indicates that the DMA is complete, the state machine branches back to the reset state to wait for another DMA request.

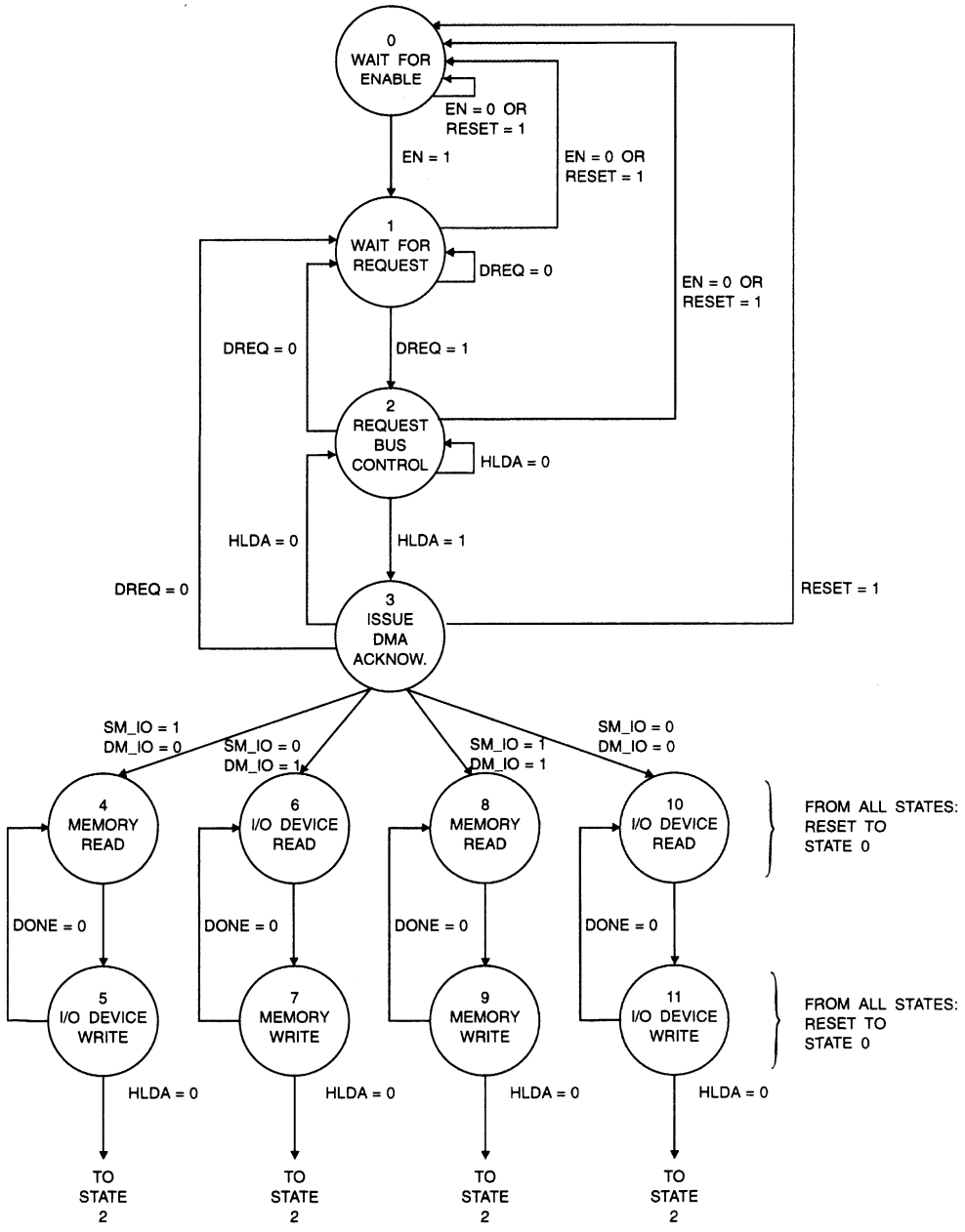
The RST signal will reset the state machine and abort the DMA. If bus control is revoked (HLDA is de-asserted) during a DMA, the state machine relinquishes bus control, suspends the transfers, and then completes the DMA when bus control is granted again. If the DMA request is removed (DREQ is de-asserted) during a DMA, the DMA controller will terminate the DMA and wait for another request.

The state bits can be assigned to buried registers in the ATV5000, since they are only used internally. The external control signals are assigned to registered I/O pins in the ATV5000. The internal control signals are also assigned to registered I/O pins so that they can be fed back universally in the ATV5000.

ATV5000 Resource Allocation

The goal in allocating functions to the available resources in the ATV5000 is to group functions which interface each other into the same quadrant. This will minimize the number of signals

Figure 9. State Diagram



which must be routed on the universal bus and minimize the number of universal product terms required for each logic function. Within a quadrant, the I/O pins and associated logic are assigned first, and then any remaining buried resources can be assigned.

In this application, the address and data bus interfaces and the address and word counters would ideally be located in the same quadrant. This would minimize the universal bus routing and allow the counters to use buried registers. Since there are not enough resources in each quadrant to fit that much logic, the functions must be divided into smaller pieces. Figure 10 shows how the logic for this application is divided and allocated into quadrants.

The buses and counters are "bit-sliced" to create logic blocks which fit into each quadrant. The counters are divided by creating stages with a look-ahead carry in between. The first quadrant contains five bits of the data and address buses, five bits of each of the counters, and a carry bit from each counter. The second quadrant contains the next five-bit section and the third quadrant contains the last six-bit section. The carry bits are routed on the universal bus to the next quadrant. The state machine and command register are allocated to the fourth quadrant. The internal control signals generated by the state machine are routed on the universal bus to all quadrants.

Each of the counters would normally require three universal product terms for the load and count functions, since the control signals are universal. This would mean that each of the counters needs two sum terms in each logic cell. To avoid this, a regional load control signal was created in each quadrant for each of the counters, using the buried logic cells. Two of the counters universal product terms then become regional product terms, and the counters only require one sum term.

Each bit of the address bus is assigned to a combinatorial I/O pin. Each of those logic cells has two buried registers available, which are used for the address counters. The logic cell configuration is shown in Figure 4. Each bit of the data bus is assigned to a registered I/O pin. Each of those logic cells has an additional buried register available, which is used for the word counter. The carry bits for the counters are assigned to registered I/O pins so they can be routed universally.

The four state bits required seven, ten, four, and four product terms. In order to provide seven product terms, the first state bit was assigned to a registered I/O pin and allocated two sum terms. The other available register in that logic cell was assigned to one of the state bits which only required four product terms. The logic cell configuration is shown in Figure 5. The state bit which required ten product terms was assigned to a registered I/O pin and allocated all three sum terms. The control signals from the state machine (both internal and external) were assigned to registered I/O cells. The other available buried registers in those logic cells were assigned to the remaining state bit and the command register bits.

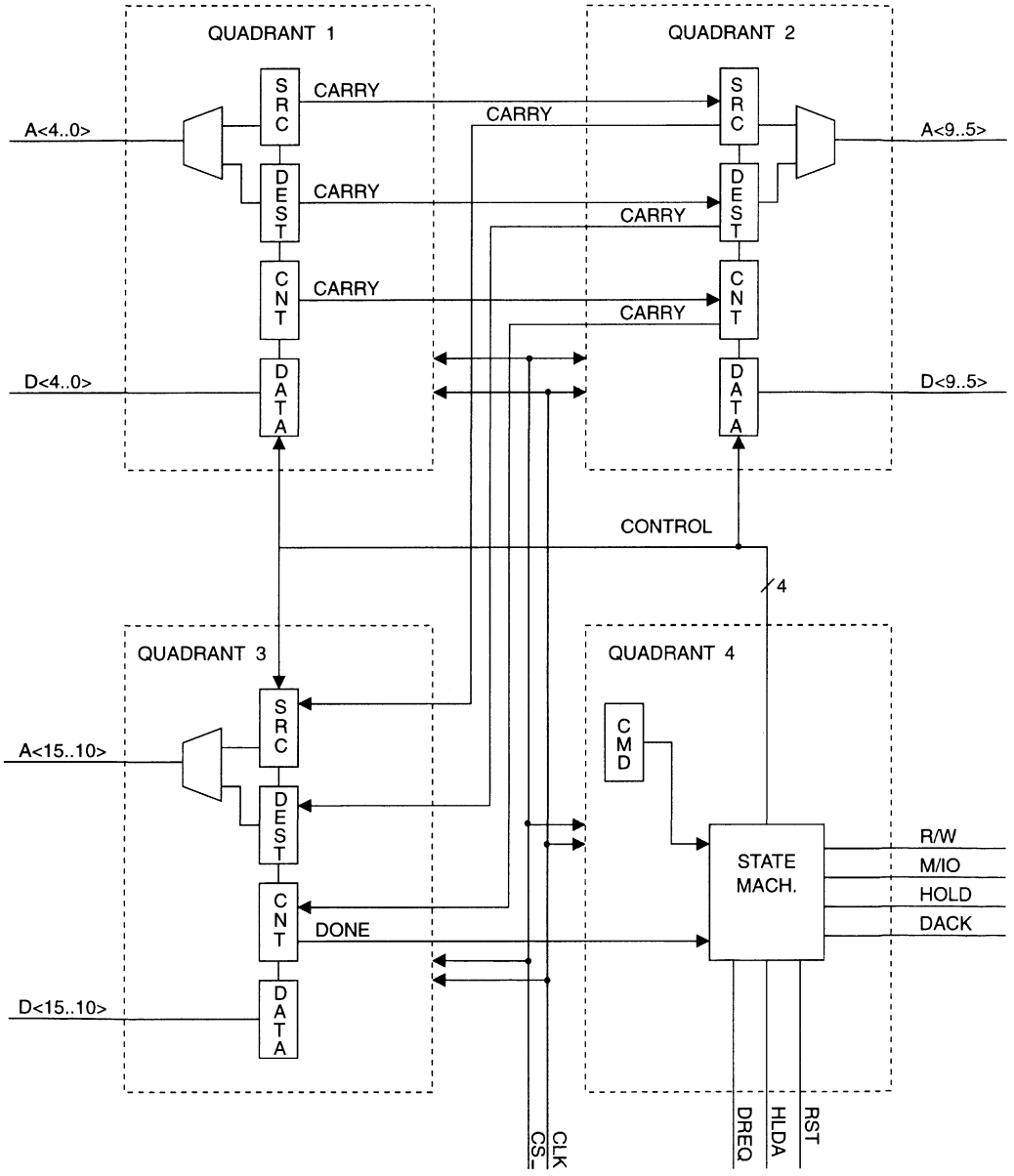
This application uses five input pins, 49 I/O pins and 86 flip-flops. There are three input pins left unassigned. Quadrants 1 and 2 each have three buried registers and three buried logic cells left unassigned. Quadrant 3 has one buried register and three buried logic cells left unassigned. Quadrant 4 has three I/O logic cells, four buried registers, and six buried logic cells left unassigned.

The equations and pin and node assignments used to implement the design are given in the ABEL™ source file at the end of this application note.

Summary

This example shows how the ATV5000 can be used to implement a complex function. The DMA controller design uses many of the features of the ATV5000. It requires a few dedicated input pins and a large number of I/O pins. The internal counters and control can use the buried logic without sacrificing I/O pins. The design which is presented is a simplified DMA controller, and is meant to show the basic functions. The interface and timing can be tailored to a particular CPU system. The design also provides an example of how to describe the device features using the ABEL™ high level descriptive language.

Figure 10. Resource Allocation



ABEL™ Source Code

```
module DMAC ;
title 'DMA Controller - Example for the ATV5000
Atmel Corporation PLD - (408)436-4333 PLD Applications Hotline
Wendey Mueller - Sept. 15, 1992'

DMAC device 'P5000';

CLK,CS_,RST              pin 1,2,32;
HLDA,DREQ                pin 34,35;
D0,D1,D2,D3              pin 4,5,6,7 istype 'reg_d,buffer';
D4,D5,D6,D7              pin 8,18,19,21 istype 'reg_d,buffer';
D8,D9,D10,D11            pin 22,23,38,39 istype 'reg_d,buffer';
D12,D13,D14,D15          pin 40,41,42,43 istype 'reg_d,buffer';
A0,A1,A2,A3              pin 9,10,11,12 istype 'com,buffer';
A4,A5,A6,A7              pin 13,24,25,26 istype 'com,buffer';
A8,A9,A10,A11            pin 27,28,44,45 istype 'com,buffer';
A12,A13,A14,A15          pin 46,47,48,49 istype 'com,buffer';
R_W,M_IO                 pin 55,56 istype 'reg_d,buffer';
HOLD,DACK                pin 57,58 istype 'reg_d,buffer';

ST0,ST1                  pin 52,53 istype 'reg_d,buffer';
ST2,ST3                  node 160,162 istype 'reg_d,buffer';
EN,SM_IO,DM_IO           node 163,164,165 istype 'reg_d,buffer';
DMA_EN,BUS_OE            pin 59,60 istype 'reg_d,buffer';
CNTEN,LATEN              pin 61,62 istype 'reg_d,buffer';
CNT0,CNT1,CNT2,CNT3      node 121,122,123,124 istype 'reg_t,buffer';
CNT4,CNT5,CNT6,CNT7      node 125,134,135,136 istype 'reg_t,buffer';
CNT8,CNT9,CNT10,CNT11    node 137,138,147,148 istype 'reg_t,buffer';
CNT12,CNT13,CNT14,CNT15  node 149,150,151,152 istype 'reg_t,buffer';
SA0,SA1,SA2,SA3          node 766,767,768,769 istype 'reg_t,buffer';
SA4,SA5,SA6,SA7          node 770,779,780,781 istype 'reg_t,buffer';
SA8,SA9,SA10,SA11        node 782,783,793,794 istype 'reg_t,buffer';
SA12,SA13,SA14,SA15      node 795,796,797,798 istype 'reg_t,buffer';
DA0,DA1,DA2,DA3          node 126,127,128,129 istype 'reg_t,buffer';
DA4,DA5,DA6,DA7          node 130,139,140,141 istype 'reg_t,buffer';
DA8,DA9,DA10,DA11        node 142,143,153,154 istype 'reg_t,buffer';
DA12,DA13,DA14,DA15      node 155,156,157,158 istype 'reg_t,buffer';
SCARRY1,SCARRY2          pin 14,29 istype 'reg_d,buffer';
DCARRY1,DCARRY2          pin 15,30 istype 'reg_d,buffer';
CCARRY1,CCARRY2          pin 17,31 istype 'reg_d,buffer';
DONE                     pin 51 istype 'com,buffer';
LDSRC1,LDSRC2,LDSRC3     node 173,179,185 istype 'com,buffer';
LDDST1,LDDST2,LDDST3     node 174,180,186 istype 'com,buffer';
LDCNT1,LDCNT2,LDCNT3     node 175,181,187 istype 'com,buffer';

C,K,X,Z,U,D,H,L = .C.,.K.,.X.,.Z.,.U.,.D.,1,0;

"CREATE BUSES

DATABUS = [D15..D0];     "data bus
DATA = [D4..D0];  DATB = [D9..D5];  DATC = [D15..D10];
DLSB = [D7..D0];

ADDR = [A15..A0];        "address bus
ALSB = [A7..A0];

WRDCNT = [CNT15..CNT0]; "word count
CNTLSB = [CNT7..CNT0];
CNTA = [CNT4..CNT0];  CNTB = [CNT9..CNT5];  CNTC = [CNT15..CNT10];

SRCADR = [SA15..SA0];    "source address
```

```
SRCA = [SA4..SA0];  SRCB = [SA9..SA5];  SRCC = [SA15..SA10];
SRCLSB = [SA7..SA0];

DSTADR = [DA15..DA0];   "destination address
DSTA = [DA4..DA0];  DSTB = [DA9..DA5];  DSTC = [DA15..DA10];
DSTLSB = [DA7..DA0];

COMMAND = [EN,DM_IO,SM_IO]; "command register

STMACH = [ST3,ST2,ST1,ST0]; "state bits
STDATA = [CNTEN,LATEN,DMA_EN,BUS_OE,M_IO,R_W,DACK,HOLD]; "state machine outputs

"DEFINE STATES

S0  = [0,0,0,0];
S1  = [0,0,0,1];
S2  = [0,0,1,0];
S3  = [0,0,1,1];
S4  = [0,1,0,0];
S5  = [0,1,0,1];
S6  = [0,1,1,0];
S7  = [0,1,1,1];
S8  = [1,0,0,0];
S9  = [1,0,0,1];
S10 = [1,0,1,0];
S11 = [1,0,1,1];

"Register select for initialization
"
" A1  A0  register selected
"--------------------------
" 0   0   Command register
" 0   1   Source address register
" 1   0   Destination address register
" 1   1   Word count register
"

EQUATIONS

M_IO.OE = DMA_EN;  "M_IO and R_W are control outputs during DMA
R_W.OE = DMA_EN;

ADDR = (!BUS_OE & SRCADR.FB)     "Select source or destination address
     # (BUS_OE & DSTADR.FB);
ADDR.OE = DMA_EN;                "Address output during DMA

DATABUS.D = (DATABUS & LATEN)       "Clock in data on input bus if
          # (DATABUS.FB & !LATEN); "LATEN is true
DATABUS.CK = !CLK;
DATABUS.OE = BUS_OE;             "Data output to destination during DMA

COMMAND.D = [D2,D1,D0];          "load command register
COMMAND.CK = CLK & !CS_ & R_W & !A1 & !A0;
COMMAND.AR = DONE;

LDSRC1 = !CS_ & R_W & !A1 & A0; "create regional controls for
LDSRC2 = !CS_ & R_W & !A1 & A0; "source address counter
LDSRC3 = !CS_ & R_W & !A1 & A0;

LDDST1 = !CS_ & R_W & A1 & !A0; "create regional controls for
LDDST2 = !CS_ & R_W & A1 & !A0; "destination address counter
LDDST3 = !CS_ & R_W & A1 & !A0;
```

```
LDCNT1 = !CS_ & R_W & A1 & A0;  "create regional load controls for
LDCNT2 = !CS_ & R_W & A1 & A0;  "word counter
LDCNT3 = !CS_ & R_W & A1 & A0;

"Source address counter - 16-bit up-counter w/ parallel load
"                         3 stages with look-ahead carry in between

SRCC.T = ((SRCC.FB + 1) $ SRCC.FB) & CNTEN & SCARRY2 & SCARRY1  "count
       # (DATC.FB $ SRCC.FB) & LDSRC3;                          "load
SRCB.T = ((SRCB.FB + 1) $ SRCB.FB) & CNTEN & SCARRY1            "count
       # (DATB.FB $ SRCB.FB) & LDSRC2;                          "load
SRCA.T = ((SRCA.FB + 1) $ SRCA.FB) & CNTEN                      "count
       # (DATA.FB $ SRCA.FB) & LDSRC1;                          "load
SRCADR.CK = CLK;

SCARRY1.D = (SRCA.FB == ^h1E) & CNTEN  "source address 1st stage carry
          # SCARRY1.FB & !CNTEN;
SCARRY1.CK = CLK;
SCARRY2.D = (SRCB.FB == ^h1F) & CNTEN  "source address 2nd stage carry
          # SCARRY2.FB & !CNTEN;
SCARRY2.CK = CLK;

"Destination address counter - 16-bit up-counter w/ parallel load
"                              3 stages with look-ahead carry in between

DSTC.T = ((DSTC.FB + 1) $ DSTC.FB) & CNTEN & DCARRY2 & DCARRY1  "count
       # (DATC.FB $ DSTC.FB) & LDDST3;                          "load
DSTB.T = ((DSTB.FB + 1) $ DSTB.FB) & CNTEN & DCARRY1            "count
       # (DATB.FB $ DSTB.FB) & LDDST2;                          "load
DSTA.T = ((DSTA.FB + 1) $ DSTA.FB) & CNTEN                      "count
       # (DATA.FB $ DSTA.FB) & LDDST1;                          "load
DSTADR.CK = CLK;

DCARRY1.D = (DSTA.FB == ^h1E) & CNTEN  "destination address 1st stage carry
          # DCARRY1.FB & !CNTEN;
DCARRY1.CK = CLK;
DCARRY2.D = (DSTB.FB == ^h1F) & CNTEN  "destination address 2nd stage carry
          # DCARRY2.FB & !CNTEN;
DCARRY2.CK = CLK;

"Word counter - 16-bit down-counter w/ parallel load
"               3-stages with look-ahead carry in between

CNTC.T = ((CNTC.FB - 1) $ CNTC.FB) & CNTEN & CCARRY2 & CCARRY1  "count
       # (DATC.FB $ CNTC.FB) & LDCNT3;                          "load
CNTB.T = ((CNTB.FB - 1) $ CNTB.FB) & CNTEN & CCARRY1            "count
       # (DATB.FB $ CNTB.FB) & LDCNT2;                          "load
CNTA.T = ((CNTA.FB - 1) $ CNTA.FB) & CNTEN                      "count
       # (DATA.FB $ CNTA.FB) & LDCNT1;                          "load
WRDCNT.CK = CLK;

CCARRY1.D = (CNTA.FB == ^h01) & CNTEN  "word count 1st stage carry
          # CCARRY1.FB & !CNTEN;
CCARRY1.CK = CLK;
CCARRY2.D = (CNTB.FB == ^h00) & CNTEN  "word count 2nd stage carry
          # CCARRY2.FB & !CNTEN;
CCARRY2.CK = CLK;

DONE = (CNTC.FB == 0) & CCARRY1 & CCARRY2; "Detects when DMA is complete

STMACH.CK = CLK;
STDATA.CK = CLK;
```

```
"State Machine Controller -
"
"Inputs: RST,EN,SM_IO,DM_IO,DREQ,HLDA,DONE
"Outputs: CNTEN,LATEN,DMA_EN,BUS_OE,M_IO,R_W,DACK,HOLD

STATE_DIAGRAM STMACH

STATE S0:                          "Reset, idle state
   IF (EN & !RST) THEN             "If DMA is enabled, go to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                            "else, wait for enable
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;

STATE S1:                          "DMA enabled, wait for DMA request
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (DREQ) THEN             "If DMA requested, go to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                            "else, wait for DMA request
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;

STATE S2:                          "DMA requested, issue bus request
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!DREQ) THEN            "If DMA request was removed, return to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (HLDA) THEN             "If bus control granted, go to state 3
      S3 WITH STDATA.D = [0,1,0,0,0,0,1,1]; ENDWITH;
   ELSE                            "else, wait for bus control
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;

STATE S3:                          "Bus granted, issue DMA acknowledge
   IF (!EN # RST) THEN             "If disabled or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!DREQ) THEN            "If DMA request was removed, return to state 1
      S1 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN            "If bus control was revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE IF (SM_IO & !DM_IO) THEN   "Start DMA: Memory - I/O Device
      S4 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;
   ELSE IF (!SM_IO & DM_IO) THEN   "Start DMA: I/O Device - Memory
      S6 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;
   ELSE IF (SM_IO & DM_IO) THEN    "Start DMA: Memory - Memory
      S8 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;
   ELSE IF (!SM_IO & !DM_IO) THEN "Start DMA: I/O Device - I/O Device
      S10 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

STATE S4:                          "DMA cycle, memory read
   IF (!DREQ # RST) THEN           "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                            "else, continue DMA transfer
      S5 WITH STDATA.D = [1,0,1,1,0,1,1,1]; ENDWITH;

STATE S5:                          "DMA cycle, I/O device write
   IF (!DREQ # RST # DONE) THEN    "If DMA request removed, reset or done,
                                    "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN             "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                             "else, continue DMA transfer
      S4 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;

STATE S6:                          "DMA cycle, I/O device read
```

```
   IF (!DREQ # RST) THEN          "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S7 WITH STDATA.D = [1,0,1,1,1,1,1,1]; ENDWITH;

STATE S7:                         "DMA cycle, memory write
   IF (!DREQ # RST # DONE) THEN   "If DMA request removed, reset or done,
                                  "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN           "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S6 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

STATE S8:                         "DMA cycle, memory read
   IF (!DREQ # RST) THEN          "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S9 WITH STDATA.D = [1,0,1,1,1,1,1,1]; ENDWITH;

STATE S9:                         "DMA cycle, memory write
   IF (!DREQ # RST # DONE) THEN   "If DMA request removed, reset or done,
                                  "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN           "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S8 WITH STDATA.D = [0,1,1,0,1,0,1,1]; ENDWITH;

STATE S10:                        "DMA cycle, I/O device read
   IF (!DREQ # RST) THEN          "If DMA request removed or reset, return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S11 WITH STDATA.D = [1,0,1,1,0,1,1,1]; ENDWITH;

STATE S11:                        "DMA cycle, I/O device write
   IF (!DREQ # RST # DONE) THEN   "If DMA request removed, reset or done,
                                  "return to state 0
      S0 WITH STDATA.D = [0,1,0,0,0,0,0,0]; ENDWITH;
   ELSE IF (!HLDA) THEN           "If bus control revoked, return to state 2
      S2 WITH STDATA.D = [0,1,0,0,0,0,0,1]; ENDWITH;
   ELSE                           "else, continue DMA transfer
      S10 WITH STDATA.D = [0,1,1,0,0,0,1,1]; ENDWITH;

"This set of test vectors initializes the source address, destination address,
"word count and command data.

TEST_VECTORS (
[CLK,RST,CS_,M_IO,R_W,ALSB,DLSB] - [SRCLSB,DSTLSB,CNTLSB,COMMAND])
[ 1,  0, 1,  0,   1,  0,   0   ] - [  0,     0,     0,    0      ];
[ 1,  1, 1,  0,   1,  0,   0   ] - [  0,     0,     0,    0      ];
[ K,  0, 0,  0,   1,  1,  00A  ] - [00A,     0,     0,    0      ];
[ K,  0, 0,  0,   1,  2,  0B0  ] - [00A,   0B0,     0,    0      ];
[ K,  0, 0,  0,   1,  3,  003  ] - [00A,   0B0,   003,    0      ];
[ K,  0, 0,  0,   1,  0,  007  ] - [00A,   0B0,   003,    7      ];

"This set of test vectors performs a DMA transfer using the addresses and word
"count which was loaded.

TEST_VECTORS (
[CLK,RST,CS_,ALSB,DLSB,DREQ,HLDA] - [STMACH,STDATA,SRCLSB,DSTLSB,CNTLSB,DONE])
[ 1, 0,  1,  0,   0,   0,   0   ] - [1,      X,     0A,     0B0,    03,     0   ];
[ C, 0,  1,  0,   0,   0,   0   ] - [1,      X,     0A,     0B0,    03,     0   ];
```

```
[ C, 0,  1,  0,   0,   1,   0   ] - [2,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [3,     X,     0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,  55,   1,   1   ] - [8,     06B,   0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0A,    0B0,   03,    0   ];
[ C, 0,  1,  0,  66,   1,   1   ] - [8,     06B,   0B,    0B1,   02,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0B,    0B1,   02,    0   ];
[ C, 0,  1,  0,  77,   1,   1   ] - [8,     06B,   0C,    0B2,   01,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0C,    0B2,   01,    0   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [8,     06B,   0D,    0B3,   00,    1   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [9,     0BF,   0D,    0B3,   00,    1   ];
[ C, 0,  1,  0,   0,   1,   1   ] - [0,     X,     0E,    0B4,   0FF,   0   ];

END ;
```

Tips on Using Test Vectors for Atmel PLDs

Test vectors are a useful method for verifying designs implemented in Programmable Logic Devices (PLDs). Test vectors allow the designer to verify, test and debug a PLD design for proper functionality before it is used in the system. Most PLD development software tools and programmers offer test vector capabilities so that PLDs can be functionally simulated via software and tested during the programming process.

This application note describes the use of test vectors in the ABEL and CUPL HDLs (Hardware Description Languages)[1]. In addition, some pitfalls and precautions on the usage of test vectors will be discussed. When simulating your design using test-vectors in the Atmel-ABEL or Atmel-CUPL development tool, it is important to note that the test vectors may not simulate the actual timing requirements of your design. The ABEL or CUPL test vectors are only used to simulate and test the logic of your PLD design.

To illustrate the usage of the test vectors in ABEL and CUPL HDLs, the following examples are included in this application note.

Example #1 Example using the "D", "U", "C" and "K" vector values
Example #2 Testing Combinatorial Functions
Example #3 Testing Registered Functions
Example #4 Using Sets for a group of signals in Test-Vectors
Example #5 Repeating Vectors with the ABEL @REPEAT or CUPL $REPEAT syntax
Example #6 Simulating Buried Nodes
Example #7 Testing Bi-Directional I/O pins

In this application note, please pay special attention to the key notes that are indicated by the ☞ symbol.

Simulating in ABEL

ABEL allows the designer to enter test vectors within the ABEL source file by using the TEST_VECTORS statement. ABEL provides two functional simulators, PLASIM (PLASIM.EXE) and JEDSIM (JEDSIM.EXE) to simulate a PLD design. The PLASIM simulator, which simulates the ABEL logic equations, is executed from the "Simulate Equations", "Simulate Optimized" or "Simulate Fitted Design" command in the ABEL design environment. The first two commands simulate the pre-fitted (device independent) equations. If you have the Atmel PLD fitters, you can simulate fitted equations with the "Simulate Fitted Design" command. The second simulator available in the ABEL development tool is the JEDSIM. This simulator, which is executed via the "Simulate JEDEC" command in the ABEL design environment, verifies your test vectors with the logic data extracted from the device JEDEC file.

Simulation Trace Options

With the ABEL functional simulators (PLASIM and JEDSIM), you can select the following trace options for producing simulation outputs:

Trace Formats

The simulation output formats available in ABEL include the Pins, Waveform, Table and Macrocell formats. Note that this display option is detailed, and should be used in conjunction with the "Signal" option to reduce the size of the output report. The default option is Table format.

(continued)

Note: 1. Atmel-ABEL or Data I/O ABEL™ Version 4.x or above, and Atmel-CUPL or Logical Devices' CUPL™ Version 4.4c or above.

Simulation Trace Options (Continued)

Trace Outputs

This option selects the simulation trace level desired, such as Brief, Detailed or Clock option. The default is the Brief option. The Detailed and Clock options are useful for debugging complex logic circuits. For instance, the Clock option generates a simulation report that shows register values when the clock is 0, 1, and 0 again for each vector. This option is useful with the Macrocell trace format for debugging asynchronous circuits.

Other trace options available in ABEL include Trace Signal, Trace Last Vector, Trace First Vector, Trace Powerup, Trace X Value, Trace Z Value and Trace .tmv options. For more information on the ABEL simulators and the trace options, please refer to your ABEL User manual.

Simulating In CUPL

With CUPL, a PLD design is simulated via the CSIM (CSIM.EXE) functional simulator. This simulator simulates the logic equations of your design before the logic is mapped into your selected target PLD. Unlike ABEL, the test vectors for the CUPL are not specified within the source file. All CUPL test vectors must be specified in a test specification source file with file extension ".SI". For instance, if you have a CUPL source file called GATES.PLD, then your test-vector specification file will be called GATES.SI.

Simulation Trace Options

Like the ABEL simulators, the CUPL simulator CSIM has several simulation trace options that you can select to control the simulation outputs. The CSIM trace options is set by the $TRACE directive in the ".SI" file, and it ranges from Trace Levels 0 to 4. The default option is Level 0 that prints only the resulting simulation results. The Trace Levels 1 through 4 turns on the intermediate simulation results for each vector. These levels are specifically used for debugging your design. For example, Trace Level 1 prints the intermediate results for any vector that requires more than one evaluation pass to become stable, and Level 2 shows register values when the clock is 0, 1, and 0 again for each vector.

Please refer to your CUPL manual for more detailed information on the CUPL CSIM simulator and its trace options.

Types of Test Vector Signals

In accordance with the standards defined by the "JEDEC STANDARD No. 3-C", Table 1 shows some of the most commonly used JEDEC test vector values when testing a PLD device. The table also shows the ABEL and CUPL test vector values that correspond to each JEDEC vector.

Table 1. ABEL and CUPL Test Vector Values

Vector In JEDEC File	Description	ABEL[1] Test Vector Value	CUPL Test Vector Value
0	Drive Pin Low	0	0
1	Drive Pin Low	1	1
C	Drive Pin Low- High-Low	.C.	C
K	Drive Pin High-Low-High, Fast Transition	.K.	K
U	Drive Pin High, Fast Transition	.U.	Not Used
D	Drive Pin Low, Fast Transition	.D.	Not Used
X	Output Not Tested, Input Defined Default Level	.X.	X
F	Float Input or Output	.F.	Not Used
L	Test Output Low	0	L
H	Test Output High	1	H
Z	Test Input or Output for High Impedance	.Z.	Z

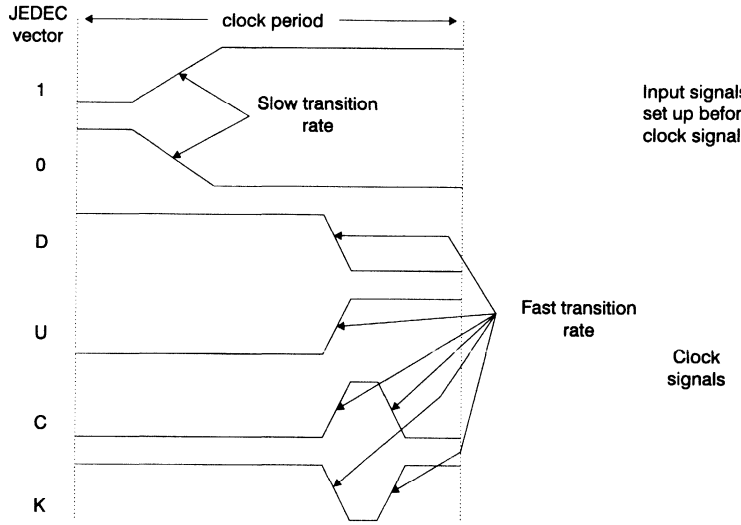
Note: 1. In ABEL, you can assign the test vector values to identifiers (in the ABEL DECLARATIONS section), and then use these identifiers in the TEST_VECTORS section. The following is an example of the ABEL test vector value assignments:
H, L, X, Z, D, U, C, K, F = 1, 0, .X., .Z., .D., .U., .C., .K., .F.;

Test Vector Issues on the Programming Hardware

When entering test vectors in your design, it is very important to use the proper vector values. If incorrect vector values are used, the vectors may fail on the PLD programmer even though they passed the ABEL or CUPL functional simulation. For instance, if you use "0" and "1" vector values to drive the clock pin of your design, the vectors will probably fail on the programmer even though they passed the ABEL or CUPL simulation (see Recommendation #1).

In addition to improper test vector usage, test vector failures on PLD programmers may also be a result of the programmer's hardware characteristics. The programming hardware dictates the sequence in which inputs in a given vector are applied to the device. For example, the programmer may assert "0" and "1" input vectors in a sequential manner from the first pin to the last pin, or asserts the input vectors almost simultaneously. In addition, the programmer also sets the "transition" or "edge" rate of the input signals. Most of today's PLD programmers can drive both slow and fast edge signals because they contain both normal and high-speed (or "clock") input drivers. Figure 1 shows the typical waveforms of the input signals applied by a programmer.

Figure 1. Typical Waveforms of input vectors applied by a PLD programmer



Recommended Vector Usage

The following recommendations will ensure:

1. That your test vectors simulations results from ABEL or CUPL are consistent with the verification or testing results by the programming hardware;
2. That the test-vectors applied by the programmer are not hardware dependent.

☞Recommendation #1:

Always use the "D", "U", "C" or "K" vector value for clock pins or clock product terms. Do not use "0" and "1" values to clock registers. See Example #1 in the Appendix Section.

For registered functions, it is very important to always use the value "D", "U", "C", or "K" to clock registers. If you use "0" and "1" input vectors to drive the clock pin of your design, the vectors may pass the ABEL or CUPL functional simulation but these same vectors may fail when they are applied on the programmer.

The two problems associated with using "0" and "1" input values for clocking the registers are:

1. The input data to the register may not set-up prior to the clock signal. With all PLD programmers, the "0" and "1" input values are applied to the device's pin before the "D", "U", "C" or "K" input. This implementation ensures that the input data to the registers are set-up prior to the registers receiving the clock signal. If "0" and "1" input values are used for clocking, then the registers could get the clock signal before the input data is set-up. This would cause incorrect input signals to be set-up and clocked into the register, resulting in a test vector failure on the programmer.

Recommended Vector Usage (Continued)

Note that you can eliminate the input data set-up problem by adding a wait-state vector prior to each "0" and "1" edge transition. However, using "0" and "1" input vectors to drive the clock for the registers is still not recommended due the possibility of the slow edge rate input drivers being used by the programmer.

2. The slow transitions of the clock signals that may cause the input data to the register to be "double clocked".

   In most PLD programmers, there are clock or high speed drivers that can drive input signals with fast edge rate. These drivers are usually dedicated for driving pins with the "D", "U", "C", or "K" clock values. For the "0" and "1" values, normal input drivers with slow edge rate are used (see Figure 1)[(1)].

   Note that there are some PLD programmers that have clock or high speed drivers which are hard-wired to some dedicated pins only (usually pin 1 of each package type). So, even when the clock values such as "D", "U", "C" and "K" are used, test vectors may still fail because slow drivers are used. This is especially important for the Atmel V-Series CPLDs because the architectures allow any input or I/O pin, or an AND function to be configured as clock for the registers. Many of today's PLD programmers either have a clock or high-speed driver dedicated to each pin, or allow limited number of high speed drivers to be routed to any pin.

For driving clocks that are gated in a clock product term, the "C" or "K" value can still be used as long as the clock pin is not used in other combinatorial functions (see Recommendation #3).

☞Recommendation #2:

Use the "D" or "U" value if your design uses the rising and falling edges of the same clock pin. See Example #1 in the Appendix Section.

In some designs, you may be required to use the rising and falling clock edges to completely test the logic. With these designs, use the "D" or "U" values on the clock pins whenever possible.

☞Recommendation #3:

Use the "D" or "U" value for generated clocks that are implemented in product term clock functions and are used in separate combinatorial functions. See Example #1 in the Appendix Section.

If a clock pin is used to drive both a product term clock function and a separate combinatorial function, then it is recommended to use "D" or "U" value on the clock pin. As mentioned in Recommendation #1, the PLD programmer applies the "D" and "U" values after all the "0" and "1" values are implemented. If the clock pin is used in a separate combinatorial function, the logic values 0 and 1 are also asserted by the "D" and "U" values respectively. Even though these logic values are applied a little later than the signals implemented via the "0" and "1" values, there is still sufficient time (typically in ms for most programmers) for the combinatorial logic to settle out before the programmer senses the output signal. For this type of design, the "C" or "K" clock vector is not suitable because the clock pulse may return to the inactive level (LOW or HIGH) before the programmer senses the output.

☞Recommendation #4:

Do not use the "F" vector on unused inputs and I/Os

To reduce noise being injected into the device, do not use the "F" value because some programmers may actually "float" the pins. We recommend that all unused device's inputs and I/Os to be terminated.

☞Recommendation #5:

Use 2 to 3 vector cycles for testing bi-directional I/Os

(See example 7 in appendix)

When testing bi-directional I/O pins, it is important to specify the vectors in a proper manner. For instance, if you are testing an I/O pin as an input, in which the I/O pin was originally configured as an output, always ensure that the I/O pins are in high impedance state before driving them as inputs.

When testing the I/O pin as an input (from an output mode):

1. First, set the I/O pin to high impedance by disabling the output enable. Use the "Z" value for the I/O pin.
2. Then, drive the I/O pin as an input.

If a single vector is used to disable and drive the I/O pins at the same time, these I/O pins may experience signal or bus contention conditions (i.e. the programmer is driving signals into the device's pins, and at the same time the device's output pins are driving) when the vector is being exercised on the programmer. This signal contention condition can sometimes cause your vectors to fail on the programmer, and may possibly cause damage to the I/O pins.

When testing the I/O pin as an output (from an input mode):

1. Set the I/O pin to the "X" (don't care) value.
2. Enable the output enable so that the I/O pin is driving.
3. Set the I/O pins with values "L" and "H" ("0" and "1" for ABEL) to verify the output signals.

Note: 1. The JEDEC standard specifies that the "0" and "1" vectors must use a fine current drive since the programmer must allow the applied input conditions to be overridden by bidirectional I/O pins.

Appendix Section - Examples on using Test-Vectors in Atmel PLDs

The following examples discuss the use of test-vectors in several different logic functions. If applicable, the test-vector examples for each logic function are illustrated in both ABEL and CUPL HDL formats.

Example #1 - Example using the "D", "U", "C" and "K" vector values

The following ABEL example illustrates the usage of the "D", "U", "C", and "K" clock values. Note that since the "D" and "U" values are not supported by CUPL, the corresponding CUPL example is not shown. For illustration on the "C" and "K" clock vectors usage in CUPL, please refer to Example #3.

DUCK.ABL

```
module duck
title ' When to use .D., .U., .C., and .K. ATMEL Corporation ';

        DUCK device 'P750';

I1,I2,I3,I4,I5            pin  1,2,3,4,5;
I6,I7,I8,I9,I10,I11,I13   pin  6,7,8,9,10,11,13;

O19,O20,O21,O22,O23       pin  19,20,21,22,23;
O14,O15,O16,O17,O18       pin  14,15,16,17,18;

B14,B15,B16,B17,B18     node 26,27,28,29,30;
B19,B20,B21,B22,B23     node 31,32,33,34,35;
O23                     IsType  'BUFFER,REG';
O22                     IsType  'BUFFER,REG';

X,Z,D,U,C,K   =.X.,.Z.,.D.,.U.,.C.,.K.;
" Writing Test Vectors for a Asynchronous Device "
" If you want a complete clock cycle, use C and K on your
" clock pins whenever possible.
" If you want to see what happens after one clock edge, use U
" and D on the clock pins whenever possible.
" If you use a 1 then a 0 or a 0 then a 1 to clock your,
" registers, then expect --- trouble.
" Different programmers treat test vectors differently.  Some go
" from pin to pin and assert 0's and 1's in a sequential manner
" then look for C's, K's, U's, and D's and assert them from pin
" to pin.  If 0's and 1's are used, your registers can be clocked
" before the inputs to the registers even have a chance to change
" and therefore the programmers report a failure to pass vector
" message.
" Other programmers assert  0's and 1's almost simultaneously and
" then go through the test vector and look for C's, K's, U's, and
" D's and then assert them almost simultaneously.  This could also
" give you a failure if you use 0's and 1's to clock.  Since your
" clock and data will be asserted almost simultaneously (still no
" guarantee which will come first ), the set-up time is not
" satisfied thus the programmers report a test vector failure.
" Keep in mind that the programmers do functional tests, not timing
" tests.  It won't catch your timing errors in your design for you.
" The test vectors simply verify your design's functionality but
" that alone should reduce the time spent on the test bench.
```

```
Equations
O23.ck =  I3;   O23.re =  I6;   O23.oe =  1;
B23.ck = !I3;   B23.re =  I6;

O23.D =   I1 # I2;
B23.D =   I4 &  O23.Q
        # I5 & !O23.Q;

O22.D = I7;
O22.ck = I8 & I9; "I9 is clock pin used in product term and
             "in O21 combinatorial function.

 O21 = I9 & I10;

test_vectors (
[I1,I2,I3,I4,I5,I6] - [O23,B23])
[ 0, 0, 0, 0, 0, 1] - [ 0 , 0 ];"reset
[ 1, 0, C, 1, 0, 0] - [ 1 , 1 ];"clock O23 first then B23 - "Recommendation #1
[ 0, 0, U, 0, 0, 0] - [ 0 , 1 ];"clock O23 - Recommendation #2
[ 0, 0, K, 1, 0, 0] - [ 0 , 0 ];"clock B23 first then O23 - "Recommendation #1
[ 0, 1, D, 0, 1, 0] - [ 0 , 1 ];"clock B23 - Recommendation #2
[ 0, 1, U, 0, 1, 0] - [ 1 , 1 ];"clock O23 - Recommendation #2

test_vectors (
[I7,I8,I9,I10] - [O22,O21])
[ 1, 0, U, 0 ] - [ 0 , 0 ]; "U and D send logic 1 and 0 "respectively
[ 1, 0, D, 0 ] - [ 0 , 0 ]; "to O21 combinatorial function.
[ 1, 1, U, 1 ] - [ 1 , 1 ]; "O21 passed - Recommendation #3
[ 0, 1, D, 1 ] - [ 1 , 0 ];
[ 0, 1, U, 1 ] - [ 0 , 1 ];
end
```

Example #2 - Testing Combinatorial Functions

The following GATES example shows how the test vectors are implemented for simple combinatorial functions such as OR, AND, XOR and INVERT logic gates.

ABEL File

GATES.ABL

```
module GATES
title 'Simple examples showing how test vectors are used for combinatorial outputs';

"Inputs d0, d1      pin 1,2;
"Outputs
Out1    pin 14 ISTYPE 'COM';
Out2    pin 15 ISTYPE 'COM';
Out3    pin 16 ISTYPE 'COM';
Out4    pin 17 ISTYPE 'COM';

"Constant Declarations to be used in the TEST_VECTORS section X,H,L =  .X.,1,0;
".X. = 'Don't Care' state that can be used for inputs or outputs.
" 1 = Logic High
" 0 = Logic Low.
```

```
EQUATIONS
Out1  = d0 # d1;     "OR function
Out2  = d0 & d1;     "AND function
Out3  = d0 $ d1;     "XOR function
Out4  = !d0;         "INVERT function

TEST_VECTORS 'Test AND/OR Functions'
([ d0, d1 ] - [ Out1 , Out2] )
[  0 ,  0 ] - [    L    ,   L  ];   "0 is substituted for L
[  1 ,  0 ] - [    H    ,   L  ];   "1 is substituted for H
[  0 ,  1 ] - [    H    ,   L  ];
[  1 ,  1 ] - [    H    ,   H  ];

TEST_VECTORS 'Test XOR/INVERT Functions'
([ d0, d1   ] - [ Out3,  Out4 ] )
[  0 ,  0   ] - [   L    ,    H  ];
[  1 ,  0   ] - [   H    ,    X  ];
[  0 ,  1   ] - [   H    ,    X  ];
[  1 ,  1   ] - [   L    ,    L  ];

"ABEL allows several test_vector statements to be used in a module.
"Each test vector group is compiled individually. The compiler will
"combine vectors from all groups to create a composite test vector set
"when it creates the JEDEC file.
end
```

CUPL Files

GATES.PLD

```
Name            GATES;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;

/* Inputs */
Pin 1 = d0;
Pin 2 = d1;

/* Outputs */
Pin [14..17] = [out1..4];

/* Logic Equations */

out1 = d0 # d1;  /* OR Function */
out2 = d0 & d1;  /* AND Function */
out3 = d0 $ d1;  /* XOR Function */
out4 = !d0;      /* INVERT Function */
```

GATES.SI

```
Name            GATES;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;
/*****************************************************************/
/*   Simulation Input File for Gates Example                     */
/*****************************************************************/
ORDER: d0,%1,d1,%1,            /* Inputs */
        out1,out2,%1,out3,out4;    /* Outputs */
VECTORS:
0 1 HL HH    /* 0,1 = Input values */
1 0 HL HL    /* L,H = Output values */
0 1 HL HH
1 1 HH LL
0 0 LL LH
1 0 HL HL
0 1 HL HH
1 1 HH LL
```

Example #3 - Testing Registered Functions

A simple 4-bit Binary Counter with reset function is used to illustrate the test vector implementation for a registered function.

ABEL File

COUNT4.ABL

```
module COUNT4

"inputs
clk    pin 1;
reset pin 2;

"outputs
q0,q1,q2,q3 pin 14,15,16,17 ISTYPE 'REG';

"Constant Declarations to be used in the TEST_VECTORS section
C,H,L = .C.,1,0;
".C. = Low-High-Low Clock pulse

Equations

"4-Bit Binary Counter equations using D-type registers
q0.d =  !q0;
q1.d =  !q1 &  q0 #
        q1 & !q0;
q2.d =  !q2 &  q1 &  q0 #
        q2 & !q1    #
        q2 &        !q0;
q3.d =  !q3 &  q2 &  q1 &  q0 #
        q3 & !q2          #
        q3 &        !q1   #
        q3 &        !q0;
```

```
[q3,q2,q1,q0].ar = reset;   "resets the counter
[q3,q2,q1,q0].clk = clk;    "clocks the counter

Test_vectors '4-Bit Counter'
([clk, reset] - [q3,q2,q1,q0])
[ C ,    1  ] - [ L , L , L , L ];  "resets the counter
[ C ,    0  ] - [ L , L , L , H ];  "1
[ C ,    0  ] - [ L , L , H , L ];  "2
[ C ,    0  ] - [ L , L , H , H ];  "3
[ C ,    0  ] - [ L , H , L , L ];  "4
[ C ,    0  ] - [ L , H , L , H ];  "5
[ C ,    0  ] - [ L , H , H , L ];  "6
[ C ,    0  ] - [ L , H , H , H ];  "7
[ C ,    0  ] - [ H , L , L , L ];  "8
end
```

CUPL Files

COUNT4.PLD

```
Name            COUNT4;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;

/* Inputs */
Pin 1 = clk;
Pin 2 = reset;

/* Outputs */
Pin [14..17] = [q0..3];

/* Logic Equations */

/* 4-Bit Binary Counter equations using D-type registers */
q0.d =  !q0;
q1.d =  !q1 &  q0 #
        q1 & !q0;
q2.d =  !q2 &  q1 &  q0 #
        q2 & !q1    #
        q2 &           !q0;
q3.d =  !q3 &  q2 &  q1 &  q0 #
        q3 & !q2    #
        q3 &        !q1    #
        q3 &        !q0;

[q3..0].ar = reset;    /* resets the counter */
[q3..0].ck = clk;      /* clocks the counter */
```

COUNT4.SI

```
Name            COUNT4;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;

/*****************************************************************/ /*
Simulation Input File for Register Example                       */
/*****************************************************************/

ORDER: clk,%1,reset,%1,             /* Inputs */
        q3, q2, q1, q0;             /* Outputs */

VECTORS:
C 1 LLLL   /* resets the counter */
C 0 LLLH
C 0 LLHL
C 0 LLHH
C 0 LHLL
C 0 LHLH
C 0 LHHL
C 0 LHHH
C 0 HLLL
```

Example #4 - Using Sets for a group of signals in Test-Vectors

When using the ABEL or CUPL design language, you can simplify the logic description for groups of signals such as Address and Data Lines, by grouping the signals in a set. This grouping of signals in sets also simplifies your test vectors and hence makes them easier to understand.

The 4-bit Binary Counter design from Example #3 was modified to show that the test vector implementation was simplified by grouping the counter outputs q3, q2, q1 and q0 in a set called count. The bold words indicate either additions or changes to the original counter design.

ABEL File

COUNT4A.ABL

```
module COUNT4A

"Pin declarations same as COUNT4.ABL

count = [q3,q2,q1,q0];  "Used in the TEST_VECTORS section

Equations
"Design equations same as COUNT4.ABL.
"               .
"              .
"@RADIX n   where n is 2 (binary), 8 (octal), 10 (decimal - default) or 16 (hexadecimal)
"The @RADIX compiler directive allows the base numbering system to be changed.
"The default numbering system is 10.

Test_vectors '4-Bit Counter'
([clk, reset] - count)
[ C ,    1  ] -    0  ;  "reset the counter
[ C ,    0  ] -    1  ;
[ C ,    0  ] -    2  ;
```

```
[ C ,    0  ] -    3  ;
[ C ,    0  ] -    4  ;
[ C ,    0  ] -    5  ;
[ C ,    0  ] -    6  ;
[ C ,    0  ] -    7  ;
[ C ,    0  ] -    8  ;
end
```

CUPL Files

COUNT4A.PLD

```
Name            COUNT4A;
/*
                    .
                    .
Design desciptions and equations same as COUNT4.PLD.

*/

field count = [q3..0];
```

COUNT4A.SI

```
Name            COUNT4A;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;

/*****************************************************************/
/*   Simulation Input File for Register Example                  */
/*****************************************************************/

Base: decimal;  /* Selection: octal, decimal and hexadecimal.
             This syntax sets the base numbering system.
             Use single quotes for inputs, and double
             quotes for outputs.
                    Eg. Inputs: '9'
                                Outputs: "9"
             If the quotes (single or double) are not used,
             the default numbering system is binary, i.e. 0 or 1.
             */
ORDER: clk,%1,reset,%1,          /* Inputs */
   count;                        /* Outputs */
VECTORS:
C 1 "0"
C 0 "1"
C 0 "2"
C 0 "3"
C 0 "4"
C 0 "5"
C 0 "6"
C 0 "7"
```

```
C 0 "8"
```

Example #5 - Repeating Vectors with the ABEL @REPEAT or CUPL $REPEAT syntax

Both the ABEL and CUPL HDLs have a compiler directive that causes a vector to be repeated a specified number of times. This REPEAT directive is particularly useful for generating sets of test vectors, especially vectors for testing counters. For more detailed information on the syntax of the REPEAT compiler directive, please refer to your ABEL or CUPL manual.

The 4-bit Binary Counter design from Example #4 was modified further to use the REPEAT syntax. The REPEAT syntax reduces the effort of generating the vectors for the counter design. Note that the modifications to Example #4 are indicated by the bold words.

ABEL File

COUNT4B.ABL

```
module COUNT4B

"Design descriptions and equations same as COUNT4A.ABL.
"             .
"             .
@CONST CNT = 1;   "Initialize the Constant CNT
Test_vectors '4-Bit Counter'
([clk, reset] - count)
[ C ,    1  ] -    0  ;  "reset the counter
[ C ,    0  ] -    1  ;

@REAPEAT 13 {  "Repeat vector for 13 times
@CONST CNT = CNT + 1; "Increment CNT
[ C ,    0  ] -  CNT;              "The compiler automatically inserts the CNT value
                                   "into the vector.
}

 [ C ,    0  ] -   15 ;  "Last count
[ C ,    0  ] -    0  ;  "Count roll back to zero

end
```

CUPL Files

COUNT4B.PLD

```
Name            COUNT4B;
/*
                    .
                    .
Design desciptions and equations same as COUNT4A.PLD.
                    .
*/
```

COUNT4B.SI

```
Name            COUNT4B;
Partno          XXXXX;
Date            3/27/95;
Designer        Atmel;
Device          V750;
/*****************************************************************/
/*   Simulation Input File for Register Example                  */
/*****************************************************************/
Base: decimal;      /* Selection: octal, decimal and hexadecimal.
                    This syntax sets the base numbering system.
                    Use single quotes for inputs, and double
```

```
                    quotes for outputs.  Eg. Inputs: '9'
                    Outputs: "9"   '
                    If the quotes (single or double) are not used,
                    the default numbering system is binary, i.e. 0 or 1.
*/

ORDER: clk,%1,reset,%1,          /* Inputs */
        count;                                /* Outputs */

VECTORS:
C 1 "0"
C 0 "1"
$REPEAT 13;  /* Repeat 13 times */
C 0 "*"
C 0 "15"  /* Last count */
C 0 "0"    /* Count roll back to zero */
```

Example #6 - Simulating Buried Nodes

In addition to output pins, ABEL and CUPL allow buried nodes (combinatorial or registered) to be simulated. Simulating the buried logic allows the designers to debug the complex logic and state machines in their PLD designs. There are no special requirements for simulating the buried nodes, except that it is important to note that the buried node vectors cannot be functionally verified on a programmer. This means that the expected output for the buried nodes will not appear on the JEDEC file. If verifying the functionality of the buried nodes on the programmer is important, then these nodes can be buffered to the unused I/O pins of the device.

☞ If a fitter is used for the Atmel-ABEL or Data I/O's ABEL tool, the fitter will optimize the design by choosing the reversed polarity of the combinatorial nodes (indicated by the "Polarity is INVERT" message in the fitter output file ".FIT"). To compensate for the reversed polarity, the fitter inverts all the references to the combinatorial nodes. Hence, the resulting logic at the output pins is equivalent to the original equations. If these buried combinatorial nodes are simulated (via the "Simulate Fitted Design" or "Simulate JEDEC" command only), the vectors for these nodes will need to be inverted to reflect the change in polarity of the the buried nodes. A 4-Bit Loadable Shift Register design is used to illustrate the buried node simulation.

6

ABEL File

SHIFT4.ABL

```
MODULE shift4
TITLE '4-Bit Loadable Shift Register';

"Block Diagram "
"                               ..........................
"                               :                        :
"              Load ..........> :                        : ..........> Ser_out
"                               :                        :
"                               :                        :
"                               :                        :
"           D0..D3 ..........>  :                        :
"                               :                        :
"                               :                        :
"                               :                        :
"              CLK ..........> :>                        :
"                               :                        :
"                               :........................:

"When Load is TRUE, D0..D3 data is loaded into the shift register.
"Once Load is FALSE, the data is shifted to the right (D3 - D0).
"A '0' is loaded into the D3 during the shifting process.  The
"last bit of the shift register, Ser_out shifts the data out.
```

```
shift4 device 'p750';

"Inputs
CLK pin 1;
Load pin 2;
RES pin 3;

D0,D1,D2,D3 pin 4,5,6,7;

"Outputs
Ser_out pin 23 istype 'buffer,reg_d';  "This output is the Q0 bit.

"Q Nodes (used the ATV750 buried nodes)
Q0 = Ser_out;
Q1,Q2,Q3 node 26,27,28 istype 'buffer,reg_d';

Qnodes = [Q3,Q2,Q1,Q0];  "Q nodes
Qshift = [0 ,Q3,Q2,Q1];      "Shifting input, always shift 0 into Q3.
Din    = [D3,D2,D1,D0];      "Data input

EQUATIONS
Qnodes.clk = CLK;  "Clock for the Shift Register
Qnodes.ar = RES;   "Reset for the Shift Register

Qnodes.d =   Load & Din       "Load in the data
               # !Load & Qshift;  "Shifts the data

DECLARATIONS
C,X = .C.,.X.;

@radix 2; "set to Binary numbering system

TEST_VECTORS
([CLK, RES, Load, Din] - [Qnodes,Ser_out]); "Ser_out=Q0
[  0  ,   0   ,   0   ,  X   ] -  [ 0000 ,  0    ];
[  C  ,   0   ,   1  ,1110]    -  [ 1110 ,  0    ];  "Loads Data Din
[  C  ,   0   ,   0  ,  X   ]  -  [ 0111 ,  1    ];
[  C  ,   0   ,   0  ,  X   ]  -  [ 0011 ,  1    ];
[  C  ,   0   ,   0  ,  X   ]  -  [ 0001 ,  1    ];
[  C  ,   0   ,   0  ,  X   ]  -  [ 0000 ,  0    ];
[  C  ,   0   ,   1  ,0101]    -  [ 0101 ,  1    ];  "Loads Data Din
[  0  ,   1   ,   0  ,  X   ]  -  [ 0000 ,  0    ];  "Resets Registers
end
```

CUPL Files

SHIFT4.PLD

```
Name            SHIFT4;
Partno          XXXXX;
Date            3/27/95;
Designer        PLD Expert;
Company         Atmel;
```

```
Assembly      None;
Location      None;
Device        V750;

/*
Block Diagram
"
"
"                                  Load ·····>                              > Ser_out
"
"
"
"                                  D0..D3 ····>
"
"
"
"                                  CLK ·····>  >
"
"
"
When Load is TRUE, D0..D3 data is loaded into the shift register.
Once Load is FALSE, the data is shifted to the right (D3 - D0).
A '0' is loaded into the D3 during the shifting process.  The
last bit of the shift register, Ser_out shifts the data out.
*/
Pin 1 = CLK;
Pin 2 = Load;
Pin 3 = RES;

Pin [4..7] = [D0..3];

/* Outputs */
Pin 23 = Ser_out; /* This output is the Q0 bit. */

/* Q Nodes (used the ATV750 buried nodes) */
Q0 = Ser_out;
Pinnode [26..28] = [Q1..3];

field Qnodes = [Q3..0];       /* Q nodes */
field Qshift = ['b'0,Q3..1];    /* Shifting input, always shift 0
                                   into Q3. */
field Din    = [D3..0];          /* Data input */

Qnodes.ck = CLK;  /* Clock for the Shift Register */
Qnodes.ar = RES;  /* Reset for the Shift Register */

Qnodes.d =   Load & Din      /* Load in the data */
          # !Load & Qshift;  /* Shifts the data */
```

SHIFT4.SI

```
Name          SHIFT4;
Partno        XXXXX;
Date          3/27/95;
```

```
Designer      PLD Expert;
Company       Atmel;
Assembly      None;
Location      None;
Device        V750;

/*****************************************************************/
 /*   Simulation Input File for Buried Node Example               */
/*****************************************************************/

ORDER:
CLK,%1,RES,%1,Load,%1,Din,%2,  /* Inputs */
Qnodes,%2,                     /* Buried Nodes,
Ser_out=Q0 */     Ser_out;     /* Output */

VECTORS:
0 0 0  XXXX  LLLL  L
C 0 1  1110  HHHL  L  /* Loads Data Din */
C 0 0  XXXX  LHHH  H
C 0 0  XXXX  LLHH  H
C 0 0  XXXX  LLLH  H
C 0 0  XXXX  LLLL  L
C 0 1  0101  LHLH  H  /* Loads Data Din */
0 1 0  XXXX  LLLL  L  /* Resets Registers */
```

Example #7 - Testing Bi-Directional I/O pins

The following example illustrates the use of test vectors to verify bi-directional I/O pins. It is important to specify your bi-directional I/O vectors in the following manner:

When testing the I/O pin as an input (from an output mode):

1. First, set the I/O pin to high impedance by disabling the output enable. Use the "Z" value for the I/O pin.
2. Then, drive the I/O pin as an input.

When testing the I/O pin as an output (from an input mode):

1. Set the I/O pin to the "X" (don't care) value.
2. Enable the output enable so that the I/O pin is driving.
3. Set the I/O pins with values "L" and "H" ("0" and "1" for ABEL) to verify the output signals.

ABEL File

BIDIR.ABL

```
module BIDIR
Title 'This example shows how to test a bi-directional I/O pin in ABEL '

"Inputs

ENA  pin 2;   "Output enable
D1  pin 3;

"Outputs

IO1  pin 22 istype 'com'; "This pin is being used bi-directionally
IO2  pin 21 istype 'com'; "This pin is defined as an output
```

```
"IO1 and IO2 pins could also be defined as registered outputs

Declarations

X,Z,H,L = .X.,.Z.,1,0;  ".Z. = High Impedance or Tri-state

Equations

IO1 = D1;            "I/O pin IO1 as an output
IO1.oe = ENA;        "When ENA=1, output IO1 is enabled,
                     "When ENA=0, output IO1 is tristated and can be used as input

IO2 = IO1;           "IO1 is used as an input for this output

test_vectors 'Bi-directional I/O test'
([ENA, D1, IO1] - [IO1,IO2]); "IO1 must be specified on both the input and output sides.
[  1   ,   0,   X  ] - [  0 ,  0 ];"IO1 output is enabled, it is important to use X (don't care)
                                   "for IO1 on the input side when IO1 output is enabled.  Almost
                                   "all programmers do not drive the pins with vector X.
                                   "Even if ENA=0 (IO1 output disabled), it is recommended to
                                   "always use vector X on the input side of all bi-directional I/O
                                   "for the first vector (because the programmer may enable the
                                   "output while setting up for the vector testing).
[  1   ,   1,   X  ] - [  1 ,  1 ];"IO2 output follows the IO1 because of the combinatorial
                                   "feedback.
[  0   ,   0,   X  ] - [  Z ,  1 ];"Disable the IO1 output, but keep the vector X on input IO1
                                   "to ensure that it is not driven as input.
[  0   ,   0,   1  ] - [  Z ,  1 ];"It is safe to drive IO1 as an input now.
[  0   ,   0,   0  ] - [  Z ,  0 ];

end
```

CUPL Files

BIDIR.PLD

```
Name            BIDIR;
Partno          xxxxx;
Date            3/7/95;
Designer        Atmel;
Device          V750;

/*****************************************************************/
/* This example shows how to define and use a     */
/* a bi-directional I/O pin in CUPL.                          */
/*****************************************************************/

/* Inputs */
Pin 2 = ENA;
Pin 3 = D1;

/* Outputs */
Pin 22 = IO1;
Pin 21 = IO2;
```

```
/* Logic Equations */
IO1 = D1;
IO1.oe = ENA;        /* IO1 output is enabled when ENA = 1 */

IO2 = IO1.IO;         /* IO1 is used as in input here */
```

BIDIR.SI

```
Name            BIDIR;
Partno          xxxxx;
Date            3/7/95;
Designer        Atmel;
Device          V750;

/*******************************************************/
/*  Simulation Input file for Bi-directional I/O  */
/*                    Example                          */
/*******************************************************/

ORDER: ENA,%1,D1,%2,    /* Inputs */
                    IO1,%1,IO2;  /* Outputs */

VECTORS:
0 0  Z X    /* Disable the I/O output pin on the first vector to ensure
            no signal contentions on the programmer during
            test-vector setup */
1 0  L L    /* IO1 output is enabled and can be tested now */
1 1  H H    /* IO2 follows the IO1 because of combinatorial feedback */
0 0  Z X    /* IO1 output is disabled. Always use a separate vector to disable the I/O
            pin first */
0 0  1 H    /* IO1 is now used as an input. */
0 0  0 L    /* IO1 is now used as an input. */
```

Summary

The ABEL and CUPL test vectors are useful for checking the logic of your complex PLD designs through software simulation. To further verify your designs, the test vectors can be used on the PLD programming hardware to test the actual device operation. To achieve consistent results between the software simulations and vector testing implemented on the programmers, it is recommended that you use appropriate input and output vector values. Remember that both software simulation and programmer vector testing provide only functional testing of your design. They are not intended to verify timing requirements of your designs.

Contents

Recommended Design Methods

Introduction

Described here are a series of guidelines for designing with AT6000 Series field programmable gate arrays (FPGAs). Among the topics covered are basic cell functionality, building simple functions, general manual placement-and-routing rules, and schematic-entry tips that can make time spent in the Interactive Editor more productive. Keeping these guidelines in mind can reduce design time and produce more efficient circuits.

The Basics

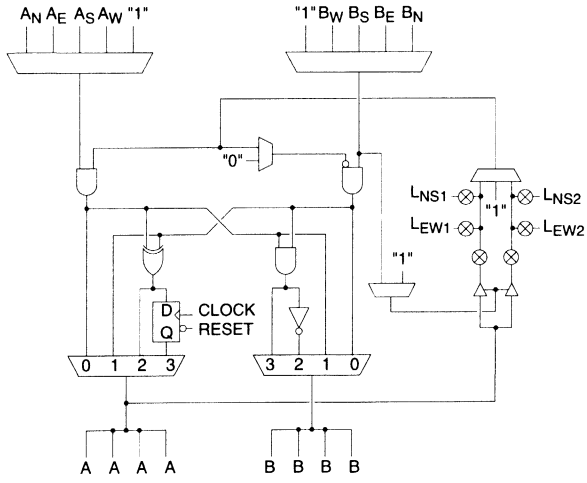
Before beginning a design, it is important to understand the building blocks of the Atmel architecture. AT6000 Series devices consist of a symmetrical array of cells that perform logic functions and are connected to a comprehensive busing structure. Symmetrical interconnects on the four sides of each cell provide cell-to-cell and cell-to-bus connections. Figure 1 shows the logic contained in each cell. A more detailed explanation of cell functionality can be found in the AT6000 Series data sheet.

Logical Functions and Cell Configurations

The logical function is the function a cell is performing; the cell configuration is how the cell is configured to perform that function. Cells can perform 44 logical functions, each corresponding to at least one cell configuration.

For example, a cell can be configured six different ways to perform the same inverter function. Figures 2a and 2b show two of these configurations. The inverter in 2a goes from a local bus input (L) to a B output. The inverter in 2b takes an A input signal, inverts it, and drives it to the A, B, and L outputs. Depending on routing conditions and the use of neighboring cells, one configuration may be more appropriate than another.

Figure 1. Cell Structure



0460A

The following table shows the number of cell configurations associated with each logical function:

Logical Function	Cell Configurations	
Combinatorial (1 output)		
INV	Inverter	6
AN2	2-input AND	4
ND2	2-input NAND	4
XO2	2-input XOR	2
ORT	2-input OR	1
MUX	A = (A•L) XOR (B•L')	1
AN2L	(B•L') 2-input AND with 1 Inverted Input	1
ORL	(A+L') 2-input OR with 1 Inverted Input	1
AN3	3-input AND	1
ND3	3-input NAND	1
ANXO	2-input AND Feeding an XOR	1
BUF	Buffer	1
Combinatorial (2 outputs)		
INVW	Local Bus Input Inverter with Thru Wire	2
INVINV	Two Inverters	3
AN2S	2-input AND and B Wire	1
AN2X	2-input AND and B Cross Wire	1
AN2INV	(A•L,L') 2-input AND and Inverter	1
INVAN2	(L',A•L) Inverter and 2-input AND	1
NDND	Two 2-input NANDS	1
XOND	2-input XOR & NAND	2
SELBUFS	A = (A•L);B = (B•L')	1
SELBUFX	A = (B•L');B = (A•L)	2
XOND3	A = (A•L) XOR B;B = (A•L) NAND B	1
WAN2L	Wire & (B•L')	1
AN2LW	(B•L') & Wire	1
Flip-Flop		
FD	D Flip-Flop Q Out	1
FDN	D Flip-Flop QN Out	3
FDHA	D Flip-Flop = Half-Adder Sum	2
FDMUX	D Flip-Flop = (A•L) XOR (B•L')	1
FDND	D Flip-Flop = 2-input NAND	1
FDOR	D Flip-Flop = 2-input OR	1
FDORL	D Flip-Flop = 2-input OR with 1 Inverted Input	1
FDXOAN3	D Flip-Flop = (A•L) XOR B; B = (A•L) AND B	1
CLKEDGE	Clock Edge Detect	1
Tri-state		
BUFZ	Tri-state Buffer	1
FDZ	Tri-state D Flip-Flop	1
LZ	"0" or "Z" (high impedance)	1
HZ	"1" or "Z" (high impedance)	1
CLKEDGEZ	Clock Edge Detect or "Z"	1
Constant		
ONE	Logic One	2
ZERO	Logic Zero	2
ONEONE	Two Logic Ones	1
ZEROZERO	Two Logic Zeros	1
ZEROONE	Logic One and Logic Zero	2

Figure 2a. First Inverter Configuration

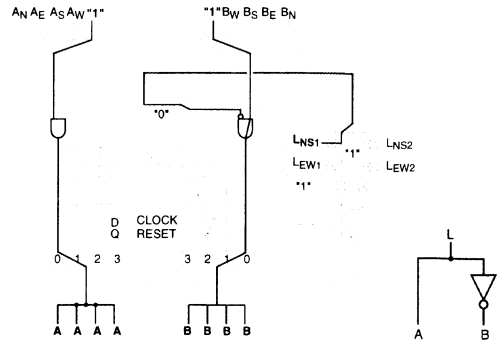
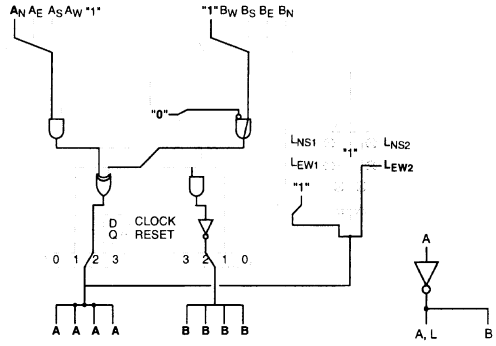


Figure 2b. Second Inverter Configuration



Comining Cell Functions

When cells are used in combination, more functions are available. The combination of two cells, for example, can produce a four-input AND gate as shown in Figure 3. Other two-cell functions include a three-input XOR and a set/reset NAND latch.

The combination of three cells can produce more complex operations such as the two-input AND/OR function shown in Figure 4.

The three cells in combination produce a specific output, but the outputs of each cell can be used as part of another function. The following table lists the intermediate outputs available from this function:

Inputs		Outputs					
A	B	NAND	XOR	XNOR	NOR	OR	AND
0	0	1	0	1	1	0	0
0	1	1	1	0	0	1	0
1	0	1	1	0	0	1	0
1	1	0	0	1	0	1	1

This same two-input AND/OR function could be implemented using a single cell, but that would preclude use of the intermediate outputs.

Macros

When cells are grouped together to perform a specific logical function, they form a macro. A single-macro function, like a single logical function, can be configured in more than one way. Each of these physical variations is called a shape. Shapes vary in their use of routing resources, the relative placement of logic cells, and the number and type of physical primitives used. Routing varies from shape to shape, making some shapes faster than others. Designs can therefore be tuned for speed or size.

Macros are either hard or soft. Hard macros maintain the relative placement of each logic cell. The timing of a hard macro can be fully characterized and remains constant regardless of the macro's orientation in the layout because the relative placement of its components remains unchanged. Because the AT6000 Series architecture is symmetrical, hard macros can be flipped or rotated without affecting internal macro timing.

Soft macros are made by dismantling, or softening, a hard macro, or by creating a schematic symbol that represents a series of hard macros. (In essence, every unplaced design is really a large, soft macro.) Each cell in a soft macro can be placed individually, so the timing of a soft macro depends on cell placement and interconnect.

A list of the more than 200 macros included in the Atmel Macro Library appears in the Integrated Development System data sheet. Most macros have more than one shape, yielding a total of over 350 configurations.

Macros can be combined to make more complex functions. For example, six half-adders (HA1, shown in Figure 5a) can combine to create the 4-bit Summer shown in Figure 5b. The Summer uses four binary inputs and defines its outputs as follows:

If 0 bits = 1, then output = 0 (Binary 000)
If 1 bit = 1, then output = 1 (Binary 001)
If 2 bits = 1, then output = 2 (Binary 010)
If 3 bits = 1, then output = 3 (Binary 011)
If 4 bits = 1, then output = 4 (Binary 100)

The Summer counts how many of the four-input bits are true and outputs the sum. Figure 5c shows the layout of the Summer in the Atmel architecture.

Placement and Routing

Once the macros to be used in a design have been selected and the schematic is complete, the design *is* ready to be placed and routed. Placement and routing are interdependent because cells can be used for both logic and routing. The relationship between

7

Figure 3. Two Cells Combine to Make a Four-Input AND

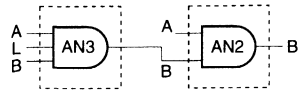


Figure 4. A Two-Input AND/OR Functions Uses Three Cells

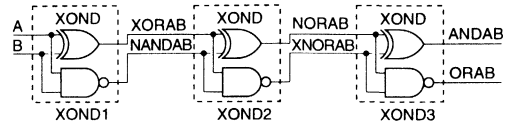


Figure 5a. Schematic of HA1

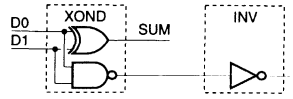


Figure 5b. Six HA1 Macros Used to Build a 4-Bit Summer Function

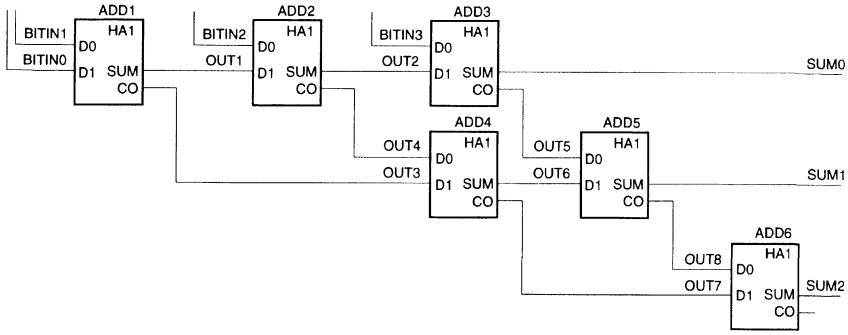
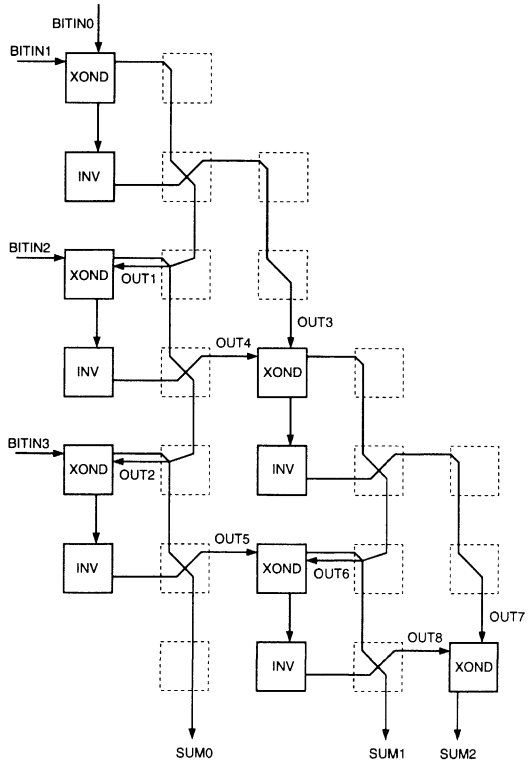


Figure 5c. Layout of the 4-Bit Summer



placement and routing creates a number of trade-offs involving circuit speed, cell utilization and location of routed nets. For example, cell placement can interfere with routing by blocking a cell and making the net unroutable. Understanding these trade-offs makes place and route easier and more efficient.

Routing Rule 1: Conserve busing resources.

In general, because cells are more plentiful than buses, cells should be used in place of buses for routing signals over short distances. Placing interconnected cells in adjacent locations in the array, or abutting them, avoids routing delays and makes it easy to route the signals together.

To conserve buses, it is sometimes better to use more than the minimum number of cells to implement a function. For example, a two-input OR gate can be performed in one cell, but requires the use of a local bus, as shown in Figure 6a. If the local bus is already in use, then it is better to implement the function using three cells and no local bus, as in Figure 6b. Using a bus-free macro implementation makes layout more flexible because the macro can be placed and routed with less restriction.

Busing resources are best saved for routing signals across longer distances (more than five cells) in the array, for tri-state capabilities, for signals with high fanout, and for hard-to-route nets.

Routing Rule 2: Align common signals used as inputs.

When a number of signals provide the inputs for many functions, group the signals together and route them in parallel.

Consider implementing the decoder function shown in Figure 7a. The decoder implements full or partial product terms:

Q1 = S3' & S2 & S1 & S0'
Q2 = S3 & S2' & S1' & S0'
Q3 = S3 & S0'

The layout of the decoder is shown in Figure 7b. Each cell receives the same input via a local bus, and directs the input to an inverter (INV), a two-input AND gate (AN2), or a two-input gate with one inverted input (AN2L). Because Q1, Q2, and Q3 go through the same number of cells, timing for each signal is regular.

Consider also the two-to-four decoder shown in Figure 8a. The logic schematic and physical layout (Figure 8b) show this function implemented using four cells and two local buses. As in the product term example above, the two inputs S1 and S0 enter the cells from the local bus, but signals could enter from adjacent cells if the local bus was already being used to route another signal. The outputs exit from the A and B cell outputs.

Figure 6a. Two-Input OR Using One Cell and a Local Bus

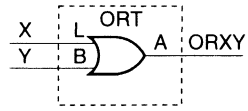


Figure 6b. Two-Input OR Using Three Cells and No Bus

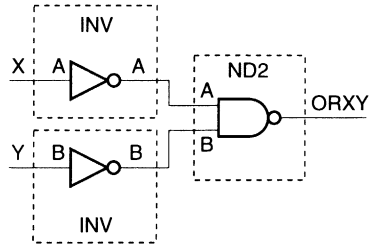


Figure 7a. Schematic of Decoder Function

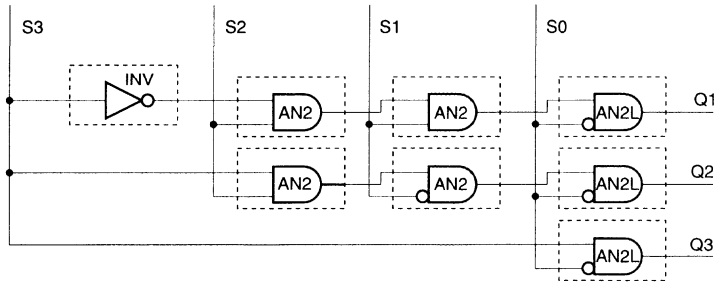


Figure 7b. Layout of the Decoder

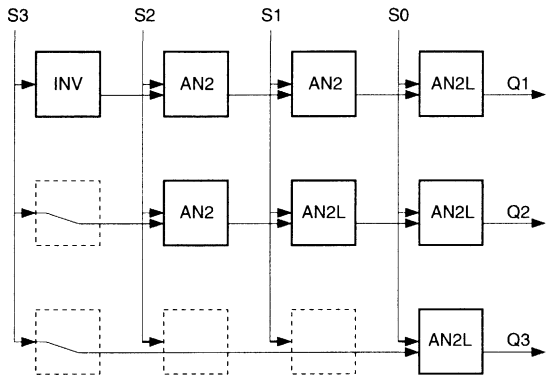


Figure 8a. Schematic of Two-to-Four Decoder Function

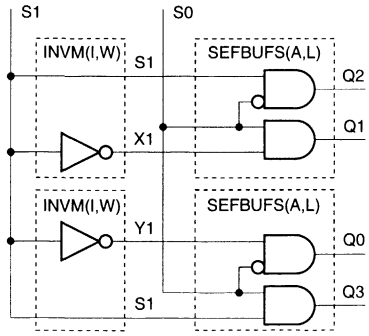
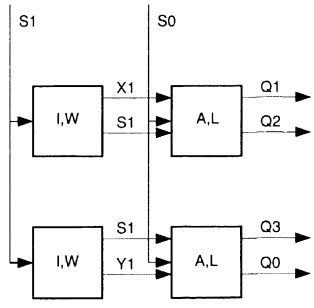


Figure 8b. Layout of Two-to-Four Decoder Function



Routing Rule 3: Use express buses whenever possible.

Because they are not connected directly to cells and thus have lower capacitive loads, express buses are faster than local buses and should be used whenever possible to increase design performance. Also, using an express bus in place of a local bus frees up the local bus for other routing purposes. In some cases, however, substituting an express for a local bus will not be possible:

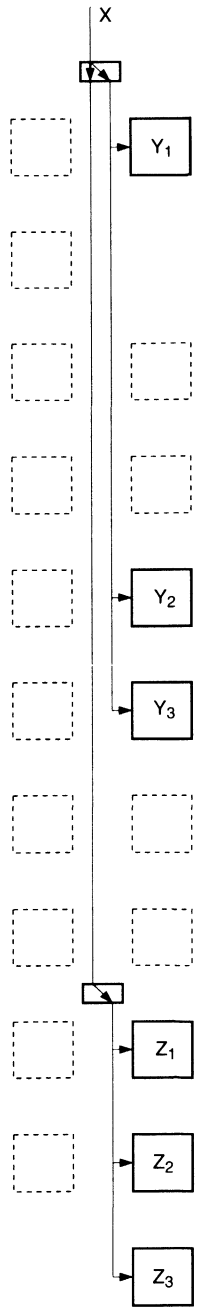
- when connecting directly to a cell
- when using a bi-directional signal
- when making 90° turns

For increased performance it is best to limit the number of local bus segments carrying a signal and to cross repeater boundaries only if necessary.

Branching the express bus signal to the local bus at each repeater can be beneficial when the fanout of a signal is greater than eight or the signal goes through more than one repeater. This helps balance the load of each local bus segment, making timing consistent across the length of the array.

Figure 9 illustrates an example of branching. Signal X is routed through the express bus and branches at the repeaters to the local bus segments driving the Y and Z cells. If signal X had been routed via the local bus to cells Y_1, Y_2, and Y_3, and through a repeater (local bus to local bus) to cells Z_1, Z_2, and Z_3, the load of the Y cells would impact the speed of the signal reaching the Z cells.

Figure 9. Branching Signals Increases Performance



Routing Rule 4: Forced redundancy can save routing resources and minimize skew.

If the same function is being used at different locations in the array, two methods can be used to distribute the functions. Figure 10a illustrates the first method. The function can be performed at a single location and the output routed to other locations in the array. With the second method, shown in Figure 10b, the inputs of the function can be routed to each location of the array and the function performed at each location. Unless the signals are already accessible throughout the array, this option can require extra routing resources. If routing resources are available, however, the second method may be preferable because it lets you align signal paths in parallel and makes timing more consistent.

Routing Rule 5: Organize registers in columns.

Clocks are distributed along the top edge of the Atmel array and allow each column of logic cells to be clocked individually (see the AT6000 Series data sheet for a detailed description). Grouping cells that use the same clock in a limited number of columns frees up the clocks in the remaining columns. Similarly, registered I/Os should be placed at the sides of the array rather than the top or bottom so the corresponding entrance and exit cells can be controlled by the same column clock.

Although independent clocking increases the flexibility of the AT6000 Series architecture, synchronous designs based on a single global clock yield better results. Asynchronously clocked registers can restrict placement and routing because they make grouping cells together more difficult and, depending on the number of different clocks in a design, can use up limited clock resources too quickly. The global clock is the most efficient clock because it is available to all cells and has low skew.

Use of the asynchronous reset logic along the bottom of the array is similar to that of the column clocks. Place logic requiring the same reset in the same column, and limit the variety of resets in a design.

Schematic Entry Tips

Although it is possible to implement designs directly in the layout using the Interactive Editor, many engineers describe their designs in a schematic and use the resulting netlist for placement and routing. The tips included here describe how to label macros and nets in Viewdraw for use with the Interactive Editor in netlist-driven mode.

Labels applied in the schematic carry over to the "to-be-placed" list of macros in the Interactive Editor. The label from each hierarchical level is included in the list, beginning with the top-level symbol and continuing down the hierarchy to the macro label. For easy viewing in the placement menu, use a short label to identify each instance of a component on the schematic.

Component labels are used in the Interactive Editor for placement. Labels can be entered at the keyboard or selected from a placement menu. The placement menu lists labels in alphabetical order, with the first item preselected. Careful use of labels can organize macros such that functions appear together, making placement go more quickly.

Nets that connect components can also be labeled for easy identification, making it simple to correlate placement and routing with the design schematic. Workview automatically assigns names to unlabeled nets (see Workview manuals for details), so it is best to create meaningful labels as you create the schematic.

Making your own components

Viewlogic lets you create components by defining symbols to represent underlying schematics. The elements of the Viewlogic component appear in the Interactive Editor's placement list under a common root name. The underlying elements can be selected from the list and placed like any other Atmel macro.

The Design Manager automatically creates a symbol for the Atmel FPGA using the 132-pin PQFP package by default. This symbol can be modified to specify I/O connections, or replaced with any of the other package symbols.

Figure 10a. Function Outputs are Routed to Other Locations in the Array

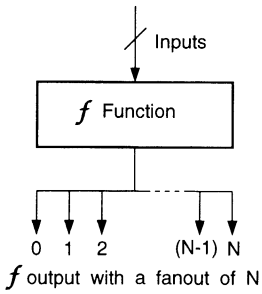
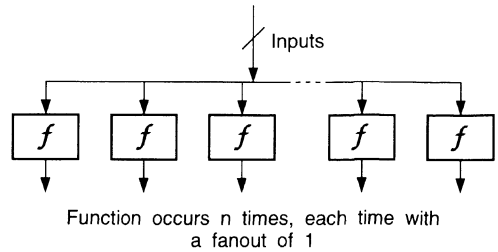


Figure 10b. The Function is Performed at Different Locations in the Array



Implementing Cache Logic™ with FPGAs

by Joel Rosenberg

The Cache Logic Concept

Atmel Corporation has developed an enabling technology to make adaptive hardware possible for electronics systems. This capability, trademarked as *Cache Logic*, was developed and patented by Concurrent Logic (recently acquired by Atmel Corporation, Inc.).[1]

Cache logic is a cost-saving way of implementing logic more efficiently. The active functions of an application are performed by a field programmable gate array (FPGA) that can be reconfigured as it operates, while inactive functions are stored in an inexpensive configuration memory—an EPROM, for example. As new functions are required, they are written over old ones.

A single application is made up of many smaller macro-level operations, like counters, multipliers, shift registers, and multiplexers. When an application is broken down into its sub-operations, two things become apparent. First, functionality overlaps. A single function may be used a number of different times. Second, there is a high degree of functional latency. At any given moment, only a small portion of an application's operations are active; only a few functions are used at the same time.

By consolidating functionality, eliminating redundancy, and tracking the occurrence of each sub-operation, functions can be organized such that a relatively small, inexpensive logic device is reconfigured as it operates to perform a complex function. In a 10,000-gate application, for example, only 2,000 gates might be active at once. By caching the extra 8,000 gates for later use, a 2,000-gate device replaces a more expensive 10,000-gate device.

Cache Logic Implementation

Cache logic implementation is conceptually similar to cache memory. In cache memory, the highest speed memory (usually SRAM) is used to store active data, while the bulk of data resides in lower-cost storage, such as DRAM, or EPROM, disk, etc. Cache logic works in a similar fashion. Only a small fraction of the circuitry —those functions which are loaded into the logic cache—is active in a system at any given time, while unused functions or variations reside in lower-cost system memory. It is even possible to compile variations of a design in real time. As logic functions are required, they can be loaded into cache logic, replacing or complementing the logic already present.

Figure 1 shows the block diagram for the Atmel AT6000 FPGA, which is an ideal medium for cache logic. The ability to implement cache logic requires FPGAs that are capable of being dynamically reconfigured in system, either completely or partially, without disrupting the operation of the balance of logic in the device. Another requirement is architecture symmetry. This is necessary to make possible the arbitrary placement of generic blocks in a location that is available at the time required. It is also necessary to allow for easy modeling of device characteristics for the artificial intelligence required in the partitioning of a design. The symmetry also simplifies the creation of arrays of devices to create a larger digital medium for the implementation of cache logic.

Note: (1) The method for exploiting Cache Logic was pioneered by the University of Strathclyde in Scotland and is described in Lysaght, P. and Dunlop, J., "Dynamic Reconfiguration of Field Programmable Gate Arrays", in *More FPGAs*, W. Moore and W. Luk, Eds., Abingdon EE&CS Books, England 1994.

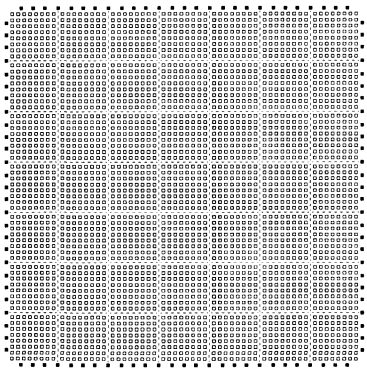
Predetermined and Dynamic Cache Logic

There are two types of cache logic which have been defined: *predetermined* cache logic and *dynamic* cache logic. *Predetermined* cache logic involves the use of predefined functions and macros that are stored in external, nonvolatile memory (EPROM, EEPROM, disk, CD ROM, or even memory remote from the system loaded over a communications link). These functions have already been placed and routed and have bit streams which have been previously generated (Figure 2). The implementation of these functions is controlled by a resident manager in the logic cache, or in an external control such as a microcontroller/processor routine. New functions may be downloaded to the logic cache in the background without disrupting the operation of the cache (logic, I/O, and register data), as shown in Figure 3. In fact, data in the registers is not lost even in the area being overwritten.

The second type of cache logic, *dynamic*, is the basis for building adaptive hardware. Dynamic caching involves the determination of logic, placement and routing of the logic, bit stream generation, and programming the logic cache in real time. The major issues to be addressed in the development of this capability include (but are not limited to) the scheduling and allocation of functions, random-logic collection, and collision handling and avoidance within the cache. Dynamic cache logic exists as a concept today; the physical implementation issues described above have not yet been fully addressed.

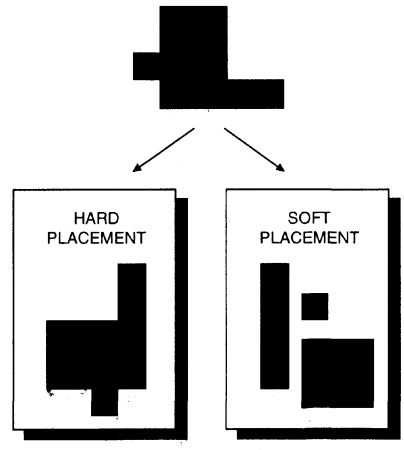
Cache logic may be applied in many applications. The concept of *virtual products* will be introduced, which utilizes the flexibility of programmable logic. Virtual products do not require cache logic programmability but, as we see, the use of cache logic greatly reduces the amount of programmable digital media needed to implement a virtual product.

Figure 1. AT6000 Array



- Symmetrical Array
- Identical Cells
- 8-by-8 Cell Sectors
- Programmable Interconnects
- Surrounded by I/O
- No Dedicated Functions
- Reconfigurable On-the-Fly
- Full
- Partial
- Without Data Loss

Figure 2. Macro Library



- Over 200 Hard Macros
- Fast
- Fully Specified
- Fixed Routing
- All Can be Softened
- Flexible Placement
- User-Defined Macros
- Create Own Library
- Use on Future Designs
- Test Macros
- For Debug/System Test
- Super Macros
- Major Predefined Functions
- Specialized for Markets

Virtual Products

A *virtual product* is a combination of a "tangible asset," such as a data acquisition board, and a service, such as product customization. The first thing to understand about virtual products is what the end customer wants, and how system developers can match their core competencies with these needs.

There are two issues raised in the manufacture of virtual products:

1. How to balance economy of scale achieved in volume manufacturing with special features that customers are willing to pay for; and
2. How to create diversity while maintaining a level of quality associated with standard high-volume production.

Cache Logic and FPGAs help the manufacturers achieve these two requirements of virtual products. A virtual product line is one with characteristics which meet the needs of a class of customers. An example would be a PC-based data-acquisition product. Such a product has certain physical requirements consistent with a PC-bus card standard. The board would also have a series of standard data gathering features such as multiple-channel A-to-D converters, digital I/O ports, D-to-A converters, and high-speed clock counters. These features are typically accomplished by highly integrated well-designed ICs readily available to all manufactures. The complexity of such products is in the data path and protocol which connects the PC to the standard IC products. The structure of this data path is prejudiced by optimum system performance, cost, and customer preference, the key item being customer preference for a successful virtual product, or for that matter any successful product.

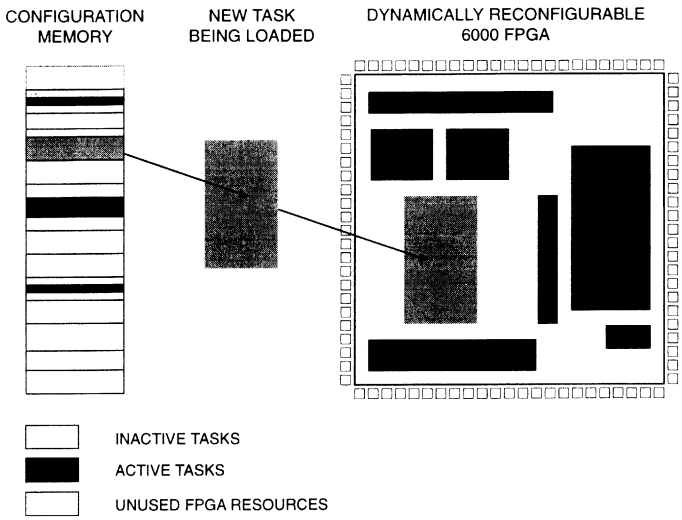
The traditional approach to creating a data-acquisition product, like most products, is to create a board with a standard bus footprint, use industry standard A-to-D and D-to-A circuits, and then create a custom data path. The manufacturer then has to trust marketing studies and instinct to determine the best data path approach. It is possible to hedge the bet by adding redundancy. This redundancy has two detrimental effects: added cost, and added complexity for the end user. The selection of wrong data path protocol or excessive complexity caused by redundancy results in dissatisfied or nonexistent customers.

A virtual product does not mean that a manufacturer would be able to offer one product which was all things to all people. The use of programmable logic would allow a manufacturer to create an extensive catalog of products, but only have a small number of tangible assemblies to tool for manufacturing. The manufacturer would use FPGAs and cache logic FPGAs to create diversity in its product line. The cost of diversity to the manufacturer is the cost of service, or "personalization engineering," required to create a niche design on a standard assembly. The advantage for the customer is a mass-produced product which meets their specific needs.

The virtual product approach allows a manufacturer to perfect a single assembly. The FPGA's ability to be configured for self-test could even enhance the quality of the assembly. Atmel has developed the IEEE1148 boundary-scan supermacro. Utilizing the reconfigurable logic capability of the AT6000 family, the boundary-scan function may be loaded into the device and diagnostics performed, then the device can be reconfigured for other logic functions. A single Atmel device may be used for testing and logic, with no overhead or speed penalty, as is the case for all other FPGAs and other ASIC devices.

The result would be an inventory of nearly identical raw-product assemblies, which through virtual design becomes a catalog

Figure 3. Cache Logic Concept



full of products when shipped to the customer. With a solid design, most customer problems can be traced to the virtual-design personalization process, and be repaired in the field with FPGA configuration updates. It is also possible to introduce new features into virtual products as soon as they are invented and proven, rather than wait until a new hardware product is designed, tooled, and manufactured.

Cache Logic Benefits

There are several benefits derived from cache logic design:

- New functionality may be added to existing hardware, without having to make modifications to the board.
- The hardware may be tailored to the application, resulting in higher system performance across a broad range of applications.
- The FPGA density limitations are eliminated.
- Overall system reliability is improved by reducing the number of physical products manufactured and utilizing boundary scan macros for manufacturing and system testing.

Overall product life cycle costs are significantly reduced by using reusable software and hardware:

- lower development costs
- lower inventory costs
- quicker time to market
- fewer parts on the board
- lower power consumption
- lower total system cost
- reusable designs

Summary

To many people, the ideal of adaptive hardware or virtual products is a futuristic concept. The AT6000 family is capable of implementing cache logic and virtual products today. The Atmel FPGA and its abilities to implement cache logic make it a foundation for adaptive hardware and virtual products. Successful design with this new technology has been commercially demonstrated. Today's design methodology, that requires a new product for each new function, will be replaced by adaptive hardware products that meet the needs of both customers and suppliers with customized products and improved quality, while reducing product development time and overall life cycle costs.

Table 1. Examples of Cache Logic™ Applications

Power and Space-Sensitive Applications	Compute Intensive Applications
Portable Computers	Computer Graphics
Battery-Operated Instrumentation	Image Processing
Portable Communications	Data Compression
Portable Medical Equipment	Speech Recognition
	Pattern Recognition
Reprogrammable Hardware	**Application Acceleration**
Test Equipment	CAD
Industrial Control	Database
Instrumentation	Spreadsheet
Special-Purpose Computers	Multimedia
Connectors	

Cache Logic™ is a trademark of Atmel Corporation.

Data Acquisition Systems Using Cache Logic™ FPGAs

by Rafe Camerota, Design Manager
and Joel Rosenberg, Marketing Manager

Atmel has developed an enabling technology to make adaptive hardware possible for Data Acquisition, Logic Analyzer, and other instrumentation products. This capability, trademarked as *Cache Logic*, was developed and patented by Atmel.

Cache logic is conceptually similar to cache memory. In cache memory, the highest speed memory (usually SRAM) is used to store active data, while the bulk of data resides in lower cost storage, such as DRAM, EPROM, disk, etc. Cache logic works in a similar fashion. Only a small fraction of the circuitry is active in a system at any given time. Only active functions are loaded into the logic cache, while unused functions, or variations, reside in lower cost system memory. It is even possible to compile variations of a design in real time. Logic functions are loaded into the logic cache as required, replacing, or complementing the logic already present.

The ability to implement cache logic requires FPGAs that are capable of being dynamically reconfigured in system, either completely or partially, without disrupting the operation of the balance of logic in the device. Another requirement is architecture symmetry. This is necessary to enable the arbitrary placement of generic blocks in a location that is available as required. It is also necessary to allow for easy modeling of device characteristics for the artificial intelligence required in the partitioning of a design. The symmetry also simplifies the creation of arrays of devices to create a larger digital medium for the implementation of cache logic. Cache logic can be used in many applications. The example used in this description of cache logic will be a series of data acquisition products. The example will also discuss the concept of virtual products, which utilize the flexibility of programmable logic. Virtual products do not require cache logic programmability, but as we see the use of cache logic greatly reduces the amount of programmable digital media needed to implement a virtual product.

The Virtual Product

A *virtual product* is a combination of a "tangible asset," such as a data acquisition board and a service, such as product customization. The first thing to understand about virtual products is what the end customer wants, and how manufacturers can match theirs core competencies with these needs.

There are two issues raised in the manufacture of virtual products:

1. How to balance economy of scale achieved in volume manufacturing with special features that customers are willing to pay for; and

2. How to create diversity while maintaining a level of quality associated with standard high-volume production.

Cache Logic and FPGAs help the manufacturers achieve these two requirements of virtual products. A virtual product line is one that has characteristics that meet the needs of a class of customers. An example would be a PC based data acquisition product. Such a product has certain physical requirements consistent with a PC bus card standard. The board would also have a series of standard data gathering features, such as multiple channel A-to-D converters, digital I/O ports, D-to-A converters, and high speed clock counters. These features are implemented in standard, high integration ICs. The most complex portions of these products are the data path and protocol sections that connect the PC to the standard ICS products. The structure of this data path is a function of optimizing system performance, cost, and customer preference.

The traditional approach to creating data-acquisition products is to create a board with a standard bus footprint, use industry standard

Field Programmable Gate Array

Application Note

7

0462A

A-to-D and D-to-A circuits, and then create a custom data path. The manufacturer then has to trust marketing studies and instinct to determine the best data path approach. It is possible to hedge the bet by adding redundancy. This redundancy has two detrimental effects: added cost, and added complexity for the end user. The selection of wrong data path protocol or excessive complexity caused by redundancy results in dissatisfied or nonexistent customers.

A virtual product does not mean that a manufacturer would be able to offer one product that was all things to all people. The use of programmable logic would allow a manufacturer create an extensive catalog of products, but only have a small number of tangible assemblies to tool for manufacturing. The manufacturer would use FPGAs and cache logic FPGAs to create diversity in their product line. The cost of diversity to the manufacturer is the cost of service, or "personalization engineering," required to create a niche design on a standard assembly. The advantage for the customer is a mass produced product that meets thier specific needs.

Quality

Quality is a very important advantage of the virtual product approach to design. Quality is usually the ultimate factor in device selection. Quality customer service can be defined as a high level of product diversity, and is measured by the degree that the specific customer requirements are met.

The foundation of product quality is in the manufacturing process. Unlike service quality, product diversity (quality customer service) is detrimental to the goal of 100% quality. Total product quality is attained by tooling for a long term process of implementation, evaluation, and feedback. Multiple custom products produced on the same assembly line conflict with the ability to attain the highest product quality and best economies of scale. Quality enhancing techniques, including just-in-time delivery, multi-discipline staffing, and integrated engineering, do not work well with multiple short run products.

The virtual product approach allows a manufacturer to perfect a single assembly. The FPGA's ability to be configured for self-test could even enhance quality of the assembly. Atmel has developed the IEEE1148 boundary scan supermacro. Utilizing the reconfigurable logic capability of the AT6000 family, the boundary scan function may be loaded into the device, diagnostics performed, and then the device can be reconfigured for other logic functions. A single Atmel device may be used for testing and logic, with no overhead or speed penalty, as is the case for all other FPGAs and other ASIC devices.

The result would be an inventory of nearly identical raw product assemblies, which through virtual design becomes a catalog full of products when shipped to the customer. Most customer problems can be traced back to the virtual design personalization process, and be repaired in the field with FPGA configuration updates. It is also possible to introduce new features into virtual products as soon as they are conceived, rather than wait until a new hardware product is designed.

A New Paradigm in Customer and Supplier Relations

New ways of doing business will develop between suppliers and their customers in a "virtual product world." The customer must realize that the cost of product development is amortized in the customized virtual product. The cost of a new personalization may be nearly the same as a complete product.

A virtual product is obsolete when the need for a personalization ceases to exist, as opposed to when the product assembly wears out.

Data Acquisition Example

The Data Acquisition system shown in the accompanying figure is one where a family of products is desired but only one assembly will be manufactured. The intent is to offer a Multiple Channel Analog-to-Digital conversion and 16 digital I/O channels, and multiple digital timers for setting sample periods. The product will be a PC-AT bus card that supports various combinations of data transfer protocols. It is conceivable that different classes of customer will want use a specific setup exclusive of all others, and not understand why anyone would want to work any other way. Putting the features into a matrix shows how many potential products are possible from this set of components (see Table 1).

The result is over 16 products that are different in their data path and protocol approach. It is possible that all of these protocols and data path structures can be implemented in a single 2,000- to 5,000-gate FPGA. Cache logic makes the fitting of the protocol in 2,000 to 5,000 gates possible. This is because each data

Table 1. ADC or Digital I/O Sample Mode

Bus Interface	External	Timer	Demand	State	Continuous
I/O Mapped	X		X		X
I/O with Internal	X	X		X	X
DMA Byte Transition	X	X	X	X	X
DMA Array Transition		X	X	X	X

path protocol combination still needs to be programmable. Items such as timer periods, I/O direction and grouping, the use of each interrupt and timer output, and DMA address counters can be implemented using cache logic, saving circuit redundancy and complexity.

Timer Periods

The timers can be compiled in a structured format. The user defines the number and period of timers required. Each timer contains an N-bit counter, and an M-value decoder, where M is the count equal to the desired period. The Atmel symmetric architecture makes the creation of macros from a high level description straight forward. An area for timers is included in the FPGA. The configuration data for that area is compiled according to customer description. The customer would receive a compiler program, and not a set of pre-defined configuration.

I/O Direction

The FPGA has flexible, individually programmable I/O. There is no reason that a description of the I/O direction and byte grouping could not result in the appropriate configuration of that area of the FPGA. The grouping of the I/Os into bytes is made by a cross-point switch. The cross-point switch is implemented using FPGA programmability. The only requirement in the development of the product is the allocation of sufficient resources in the FPGA for the cross-point area. A byte grouping description by the user would then result in configuration information for enabling the proper pass gate connections in that section of the FPGA.

Timer and Interrupt Usage

In a data acquisition circuit interrupts and timer outputs are used by many parts of the circuit. Time is required to set the period of a digital or analog sample. As the digital I/O control function, the interrupt and timer outputs can be routed to various combinations of control inputs, PC bus or internal logic of the data acquisition chips. This flexibility, although like a cross-point switch, would be more of a channel routing function. A set of routing resources is used for the connection of various programmable inputs and outputs with access to the reserved channel area.

DMA Address Generation

In designs using DMA, the DMA address is stored in a register or counter, depending on the mode. This counter is compiled based on software requirements.

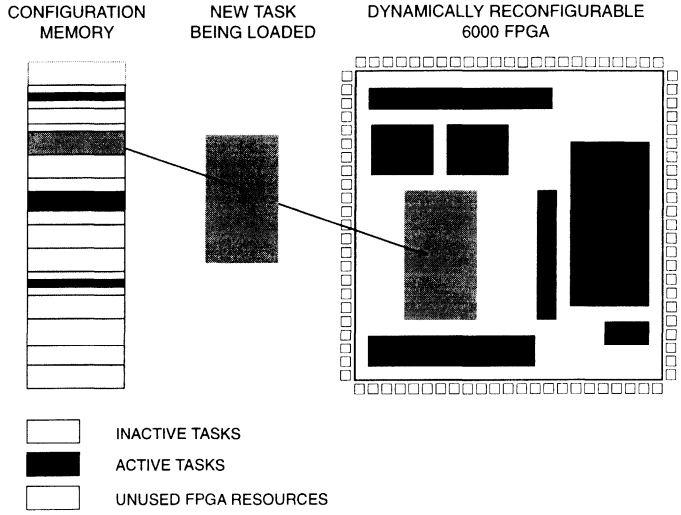
FPGA Configuration

Figure 1 shows the configuration of the FPGA SRAM: controlling its functionality and hookup are a patchwork of configuration information from various sources. Some are a base configuration file used by all products, others from look-up tables or macro compilers. The Atmel FPGA would allow items such as timer periods, or DMA address values to be updated continuously, without effecting the operation of unrelated logic. The advantage of cache logic is the elimination of redundancy. Cache logic allows the creation of any structure from the digital medium. In traditional designs a circuit would have redundancy for each anticipated eventually, and the control to enable and disable it as well. Even if an application used all possible features, some circuits would be idle, since some combinations would never occur concurrently.

The creation of FPGA configuration files from a high-level description is not an easy task. The manufacturer of a virtual product will need to make the description of the final configuration as intuitive as possible for the end customer. Given equal raw product assemblies the virtual product, like the fixed product that is easiest to use, will be the most successful. The FPGA manufacturer's responsibility is to the manufacturer. The FPGA

7

Figure 1. Cache Logic Concept



configuration and architecture must be easy to grasp, and the configuration process must be readily available. A set of compilation development tools and example like this data acquisition product will help to make the manufacturer more comfortable with the implementation of cache logic designs.

Benefits

There are several benefits of this approach to data-acquisition and other instrumentation suppliers:

1. New functionality may be added to existing hardware, without having to make modifications to the board.

2. The hardware may be tailored to the application, resulting in higher system performance across a broad range of applications.

3. Overall system reliability is improved by reducing the number of physical products and utilizing boundary scan macros for manufacturing and system testing.

4. Overall product life cycle costs are significantly reduced by using reusable software and hardware:

lower development costs

lower inventory costs

quicker time to market

fewer parts on the board

lower power consumption

lower total system cost

Summary

To many people the ideal of a virtual product is a futuristic concept. The FPGA of today is a virtual product. It is available and dependable. The Atmel FPGA and its abilities to implement cache logic make it a foundation for other virtual products. Design with this new technology has been commercially demonstrated. Today's design methodology, that requires a new product for each new function, will be replaced by the virtual product. The needs of both customers and suppliers, with customized products and improved quality; while reducing product development time and cost and attaining economies of scale by high volume production.

High-Speed, Loadable 16-Bit Binary Counter

By Frederick Furtek

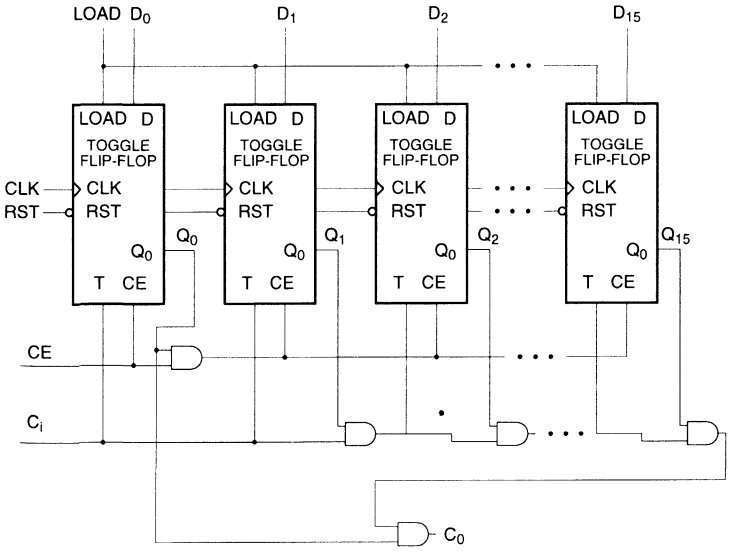
Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a fast synchronous, loadable 16-bit binary counter that operates at 70 MHz on and off chip under the worst commercial operating conditions. The use of prescaled logic to generate the carry-enable signals for each count bit allows faster operation than traditional carry-enable generation methods. The 16-bit counter is very compact, yet the inputs and outputs are readily accessible.

Description

Figure 1 shows a block diagram representation of the counter architecture and I/O. CLK is the clock signal, RST is the reset signal, and LOAD is the load data signal. CE is the count enable signal. CLK is a positive, edge-triggered synchronous signal, RST is an active low, asynchronous signal, and LOAD is an active low, synchronous signal. Pins D_0 through D_{15} are the load data inputs, pins Q_0 through Q_{15} are the count bits. Pin C_i is the carry in, C_o is the carry out. Toggle flip-flops are used as the register elements for each bit of the

Figure 1. Architecture and I/O of 16-Bit Counter



Field Programmable Gate Array

Application Note

7

0463A

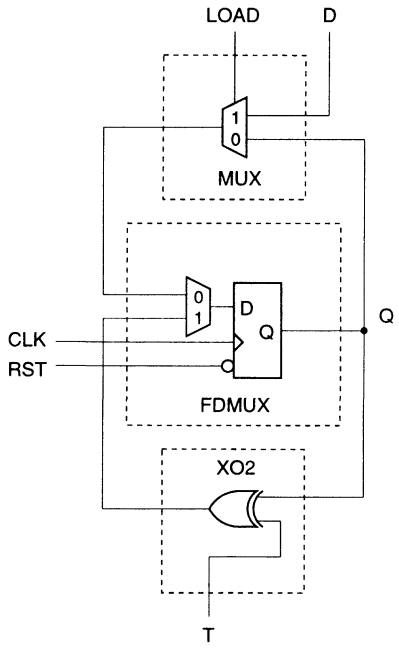
counter. They toggle on the rising edge of CLK when their RST, CE, and T inputs pins are high and the LOAD pin is low.

Initial power-up of the AT6000 device resets all the registers so the counter begins counting on the first rising edge of CLK if C_i, RST, and CE are set high and LOAD is set low. The circuit counts by allowing each register element to toggle in succession on the rising edge of CLK if the Q outputs of all prior elements are asserted.

Asserting RST at any time inhibits counting, but also resets the registers to low values.

Figure 2 shows the implementation of a register element in the 16-bit counter logic architecture. The Q output of this circuit will toggle if T and CE are high and LOAD is low on the rising edge of CLK. If CE and LOAD are low, then Q will not change, regardless of T. If CE is high and LOAD is low, then Q will remain the same if T is low upon the rising edge of CLK.

Figure 2. Schematic of 16-Bit Counter Register Element



To load a value into the counter, LOAD is set high and CE is set low before the rising edge of CLK. The value is latched into the register elements on the rising edge of CLK.

CE should then be held low until after the next rising edge of CLK to allow the carry-enable logic time to recalculate the T inputs for each register element. The carry-enable logic is the chain of two-input AND gates that generates the T signal inputs.

If LOAD is asserted for one clock cycle and CE is low for two clock cycles, the data at $D_{0\text{-}15}$ is loaded into the registers on the first clock cycle, and the counting continues from the newly loaded value on the second cycle (Figure 3).

During the LOAD cycle, when the data at $D_{0\text{-}15}$ is clocked into the counter, the carry-enable logic must have time to generate and propagate the results to every bit. Since an arbitrary number at $D_{0\text{-}15}$ can cause a carry-enable signal to propagate along the entire length of the carry-enable chain, the critical path during a LOAD operation has the potential to pass through 14 AND gate (AN2) stages before entering the last register element. By holding the CE signal low an extra clock cycle to inhibit the counting operation (as shown in Figure 3), the carry-enable logic has additional time to propagate the correct values to each bit.

During normal operation Q_0, the least-significant bit of the counter, is also a fast carry-enable signal. As shown in Figure 4, the CE inputs of each register element ahead of the first bit are tied to the Q_0. All bits greater than Q_0 must wait for Q_0 to switch from low to high before they can change on the rising edge of CLK. As the more significant bits change, their values trickle forward through the two-input AND gates that form the carry-enable logic to the T inputs of succeeding register elements. Distributing Q_0 in this manner allows an extra clock cycle for the chain of two-input AND gates to calculate the carry-enable signal for the T input of each register element.

The exact layout of the fast carry-enable logic for the first several bits of the 16-bit counter is shown in Figure 5. By replicating and concatenating the circuitry surrounded by the dotted box, the entire counter function is realized. The AN2 gates feed two-input XOR gates, (XO2). The FDMUX macro provides a two-to-one multiplexer feeding the input of a D-type flip-flop in a single cell. The MUX macro is a one-cell two-to-one multiplexer.

The performance and utilization statistics are given in Table 1. Both implementations are available in schematic and layout form.

Figure 3. Timing Diagram of Counter Load Cycle

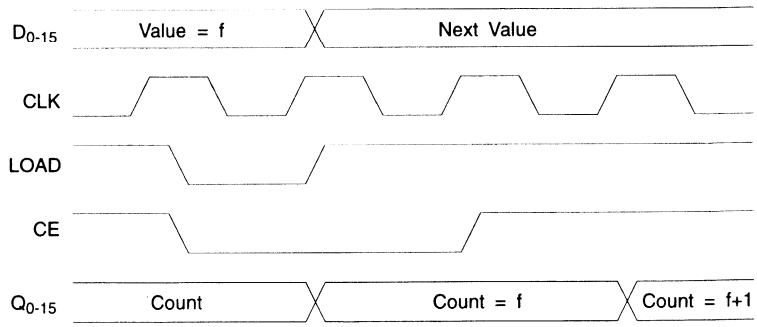


Figure 4. Schematic of Counter Architecture

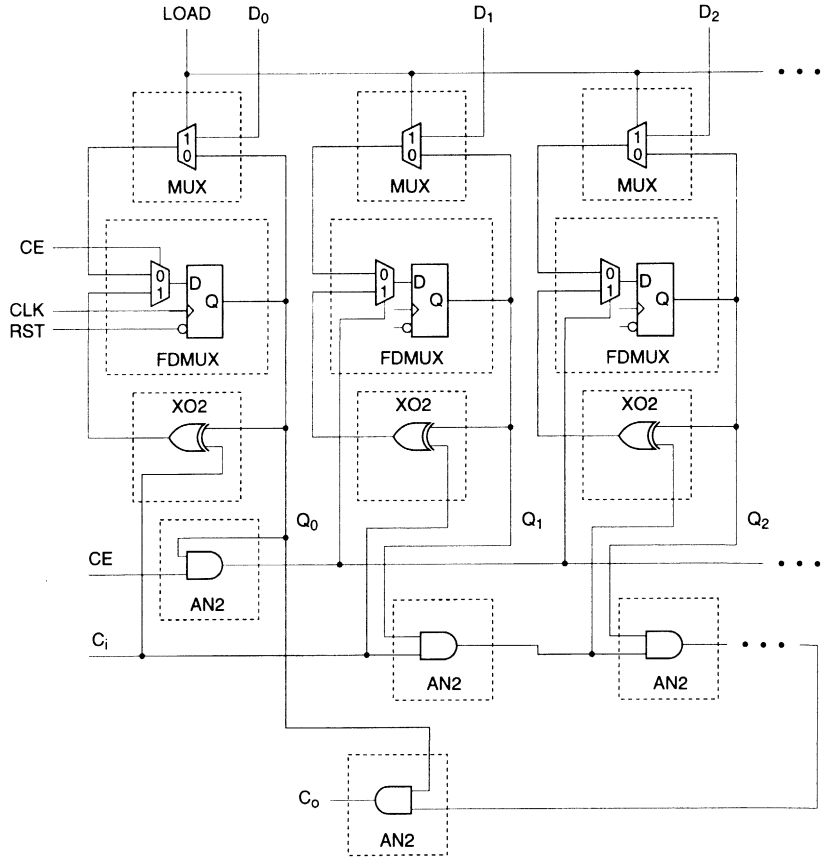


Figure 5. Layout of Counter Architecture

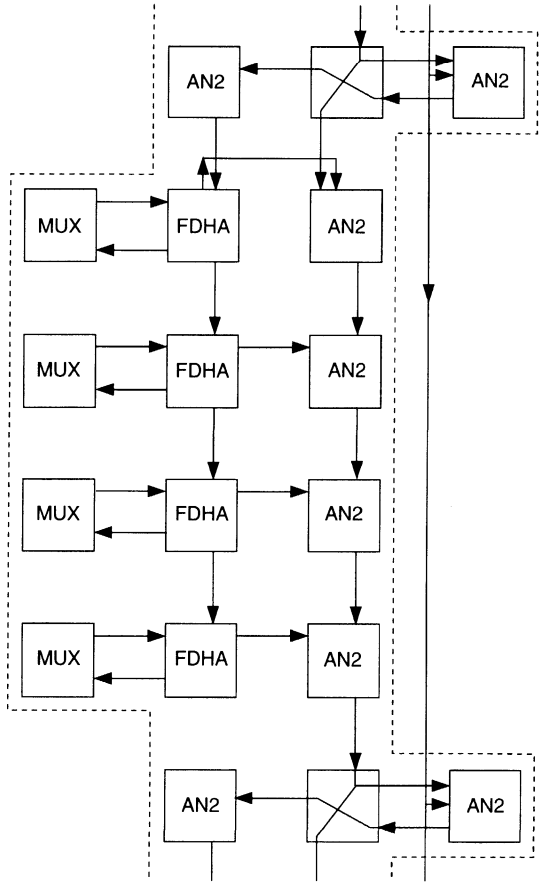


Table 1. Statistics for 16-Bit Counter Implementation

Counter	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Counting Speed[2]	Maximum Loading Speed[3]
16-Bit	96	17 x 7	14.2 ns / 70 MHz	22.7 ns / 44 MHz

Notes:
1. Includes cells used as wires.
2. Worst-Case Commercial Operating Conditions: CLK → C_0, 70°C, 4.75 V.
3. Worst-Case Commercial Operating Conditions: LOAD → $C_{0\text{-}15}$.

Compact, Loadable 16- and 32-Bit Binary Counters

Introduction

The AT6000 Series architecture accommodates dense, synchronous, loadable binary counters. A 16-bit counter counts at 42 MHz, and a 32-bit at 36 MHz in AT6000-2 devices. Both counters are very compact, yet their inputs and outputs are readily accessible.

Description

Figure 1 is a block diagram representation of the I/O and architecture for a 16- or 32-bit counter. Pin CLK is the clock signal, RST the reset signal, and LOAD the load data signal. CLK is a positive, edge-triggered synchronous signal, and LOAD is an active low, synchronous signal. Pins D_0 through $D_{15,31}$ are the load data inputs, and pins Q_0 through $Q_{15,31}$ are the count bits. Pin C_i is the carry in; C_o is the carry out.

4-bit synchronous loadable binary counters are used to compose larger 16- or 32-bit counters. These 4-bit counters toggle on the rising edge of CLK when their RST is high and LOAD is low.

Initial power-up of the AT6000 device resets all the registers. The counter begins counting on the first rising edge of CLK if C_i and RST are set high and LOAD is set low. The circuit counts by allowing each 4-bit counter stage to toggle in succession on the rising edge of CLK if the Q outputs of all prior stages are asserted. Asserting RST at any time inhibits counting, but also resets the 4-bit counters to low values.

Figure 1. Architecture and I/O of 16-Bit or 32-Bit Counter

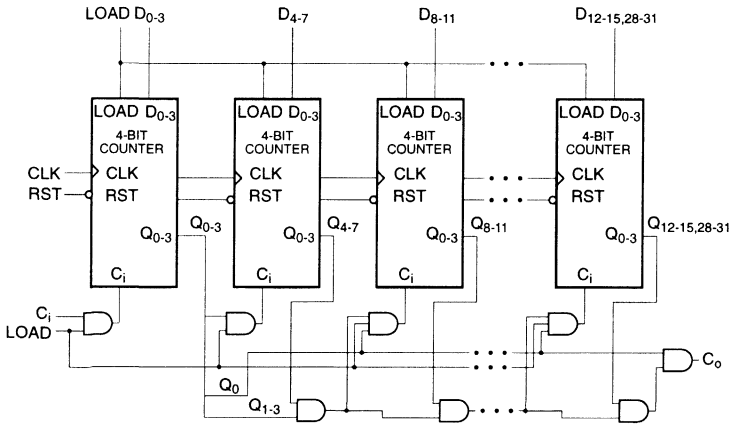


Figure 2 shows the implementation of the 4-bit counter stage used in the 16- and 32-bit counter architectures. A Q output in this circuit will toggle if C_i is high and LOAD is low, and all prior Q output are asserted upon the rising edge of CLK. If C_i and LOAD are low, then Q will not change. This circuit exists as a predefined marco library element called CRP4.

To load a value into a 16-bit counter, LOAD is set high prior to the rising edge of CLK. The value is latched into the CRP4 stages on the rising edge of CLK.

LOAD should then be held low until after the next rising edge of CLK to allow the carry-enable logic time to recalculate the carry-enable bit for each CRP4 stage. The carry-enable logic is the chain of two-input AND gates that generates the C_i signal inputs for each CRP4 stage. In Figure 3, if LOAD is asserted for two clock cycles the data at $D_{0\text{-}15}$ is loaded into the CRP4 macros on the first clock cycle, and counting continues from the newly loaded value two cycles later

During the LOAD cycle, when the data at $D_{0\text{-}15}$ is clocked into the 16-bit counter, the carry-enable logic must have time to generate and propagate the results to every bit. Since an arbitrary number at $D_{0\text{-}15}$ can cause a carry-enable signal to propagate along the entire length of the carry-enable chain, the critical path during a LOAD operation has the potential to pass through 17 AND gates (AN2) before entering the last register element. By holding the LOAD signal low an extra clock cycle to inhibit the counting operation (as shown in Figure 3), the carry-enable logic will have additional time to propagate the correct values to each bit.

Figure 4 shows the detailed schematic of a 16-bit counter partitioned into four stages. During normal operation Q_0, the least-

Figure 2. Schematic of a 4-Bit Counter Macro CRP4

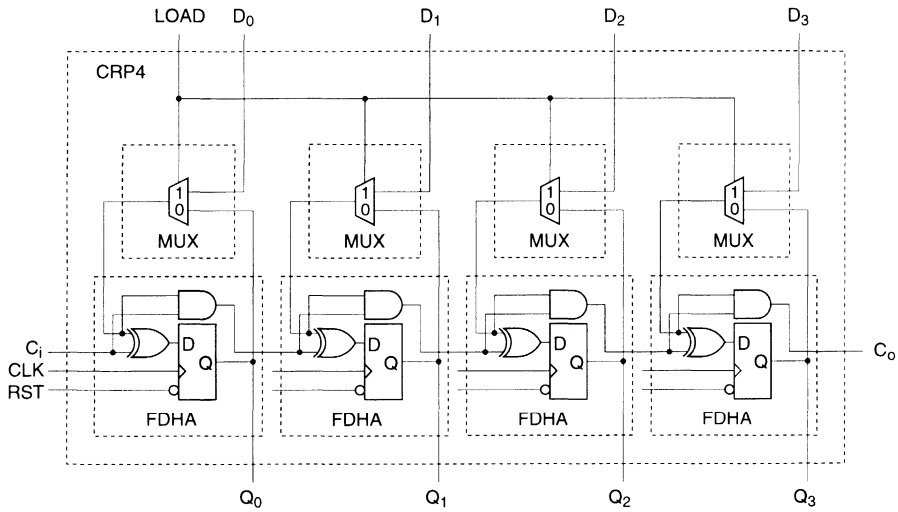
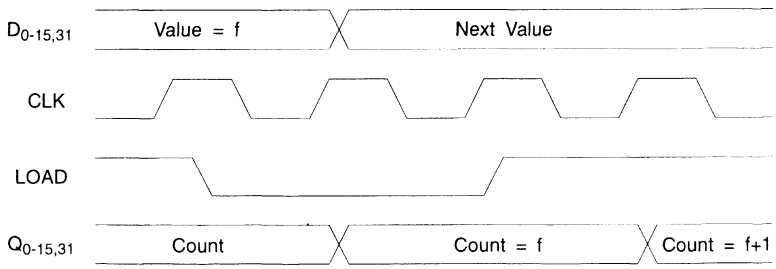


Figure 3. Timing Diagram of Counter Load Cycle



significant bit of the counter, is also a fast carry-enable signal. All bits greater than Q_0 must wait for Q_0 to switch logic levels before their carry-enable logic stabilizes. Q_0 is distributed to all four CRP4 macros in an attempt to balance and minimize the propagation delay of Q_0 to the C_i of the more significant CRP4 macros. For example, as the more significant bits in the first stage are asserted, their values trickle through the two-input AND gates (AN2) that form part of the carry-enable logic. When all the more significant bits are asserted and Q_0 switches from low to high on the rising edge of CLK, the carry-enable signal to the C_i input of the second CRP4 is enabled. While its C_i signal is asserted, the CRP4 in the second stage counts on the rising edge of CLK.

By replicating and concatenating the circuitry surrounded by the dotted box, larger counter functions are realized. The performance and utilization statistics for the 16- and 32-bit counters are given in Table 1. Both implementations are available in schematic and layout form.

Figure 4. Schematic of Counter Architecture

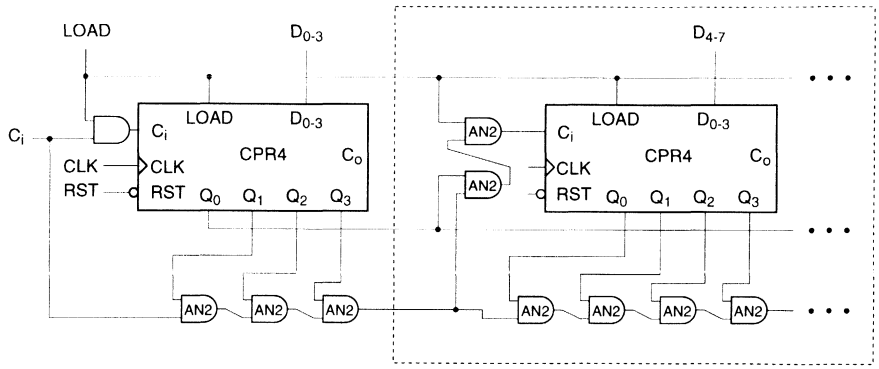


Table 1. 16- and 32-Bit Counter Performance Comparison

Counter	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Counting Speed[2]	Maximum Loading Speed[3]
16-Bit	76	10 x 8	22 ns / 45 MHz	55.5 ns / 18 MHz
32-Bit	136	18 x 8	35.7 ns / 28 Mhz	83.3 ns / 12 MHz

Notes:
1. Includes cells used as wires.
2. Worst-Case Commercial Operating Conditions: CLK → C_o, 70°C, 4.75 V.
3. Worst-Case Commercial Operating Conditions: LOAD → $Q_{0\text{-}15,31}$.

16-Bit Up/Down Counter/Shift Register

Introduction

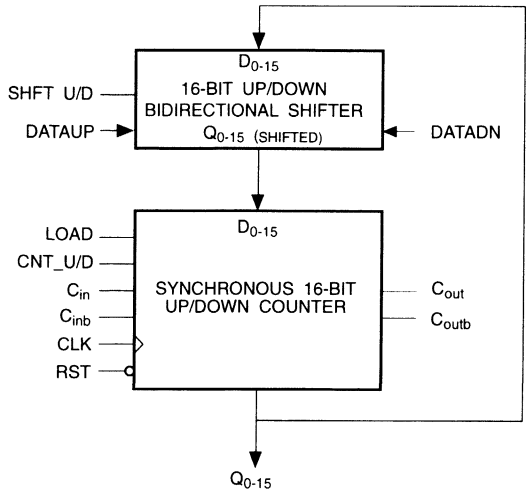
The AT6000 Series field programmable gate array (FPGA) lets the designer implement a synchronous, 16-bit Up/Down Counter/Shift Register that operates at 22 MHz under the worst commercial operating conditions. In this circuit is most of the combined functionality of the 74193 Up/Down Counter and 74194 Bidirectional Shift Register TTL components. It would take eight discrete TTL components to implement an 16-bit Up/Down Counter/Shift Register. Nearly the same function can be achieved in a AT6005 using less than 8% of the available logic.

Description

Figure 1 shows a block diagram of the counter/shifter. Pin CLK is the clock signal, RST the reset signal, and LOAD the count/shift control signal. CLK is a positive, edge-triggered synchronous signal, RST an active low, asynchronous signal, and LOAD an active low, synchronous signal. Pins Q_0 through Q_{15} are the count bits. Pins C_{in} and C_{out} are the carry-in and carry-out signals. Pins C_{inb} and C_{outb} are the carry-in borrow and carry-out borrow signals. SHFT_U/D and CNT_U/D control the direction of the shift and count operations. DATAUP and DATADN are the shift-up and shift-down serial data inputs for the shifting operation.

The output of a 16-bit fast ripple-carry counter is input into a bidirectional shifter that shifts the data inputs up or down one bit position. The output of the shifter is fed back to the parallel data inputs (D_{0-15}) of the counter. When LOAD is set high, the output of the shifter is ignored and the counter increments or decrements depending on the CNT_U/D. If LOAD becomes unasserted, the counting operation is inhibited, and the shifter provides the shifted count at Q_{0-15} to the parallel data inputs of the counter. While LOAD remains low, the

Figure 1. 16-Bit Up/Down Counter/Shifter



Field Programmable Gate Array

Application Note

7

0465A

counter essentially acts as a shift register, and will shift the data at Q_{0-15} either up or down depending on SHFT_U/D.

Initial power-up of the AT6000 device resets all the registers in the counter/shifter. While LOAD and RST are asserted, incremental counting commences if CNT_U/D and C_{in} are asserted before the rising edge of CLK. Decrement counting commences if CNT_U/D is unasserted and C_{inb} is asserted before the rising edge of CLK.

If LOAD is set low, the circuit becomes a shift register on the rising edge of CLK. The CNT_U/D, C_{in}, and C_{inb} signals are ignored, and control of the circuit is determined by SHFT_U/D, DATAUP, and DATADN. If SHFT_U/D is asserted, the data at Q_n will be shifted to Q_{n+1} on the rising edge of CLK. The value present at DATAUP is shifted to Q_0. Down shifting occurs when SHFT_U/D is set low.

The Up/Down Counter/Shifter must be serially loaded with a starting value.

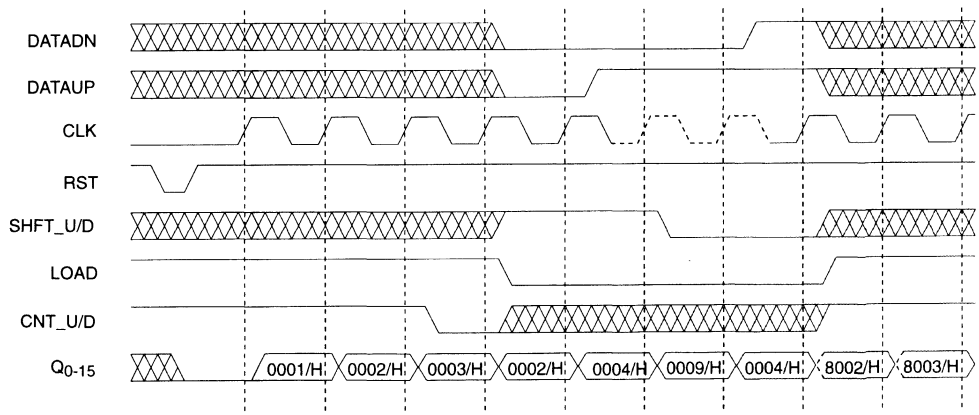
Although Figure 1 shows that the 16-bit counter has a parallel load capability, the data inputs of the counter are already driven by the shifter. While LOAD is low, counting is inhibited. With the proper control of SHFT_U/D, any 16-bit value can be shifted serially into the register through the inputs DATAUP or DATADN. When the register is loaded with the correct value, Up/Down counting can begin on the first rising edge of CLK after LOAD is set high. Parallel loading of the start value is the only feature not inherent in the circuit that is present in the 74193 TTL device. Figure 2 shows the timing of the count/shift operation.

The schematic in Figure 3 shows the detailed implementation of the circuit. The FDHA macro is a half-adder sum that feeds a D-type flip-flop. Together with the MUX two-to-one multiplexer macros and the SELBUFS selector macros, an Up/Down counter with parallel load is constructed using only six cells per bit. SELBUFS macros enable the carry generation logic for each bit of the counter to be implemented in only one cell. The chain of SELBUFS macros that forms the carry-generation logic is also the critical path of the circuit. In the layout of this counter the least-significant bit Q_0 is distributed to the carry-enable logic of the other more significant bits. Distributing Q_0 will improve the performance by minimizing the delay through the critical path for both up-counting and down-counting.

MUX macros are used to form the shifter portion of the circuit. The inputs into each MUX of the shifter will be the Q_{n-1} and Q_{n+1} outputs of the counter, and the output of the shifter will feed the n^{th} parallel data input of the counter. At the least- and most-significant bits, the MUX macros will use DATAUP and DATADN as inputs.

The performance and utilization statistics for the 16-bit Up/Down Counter/Shifter are given in Table 1. This implementation is available in schematic and layout form.

Figure 2. Timing of Load/Count Operation



NOTE: $C_{in} = C_{inb} = 1$

Figure 3. Schematic of Counter Figure

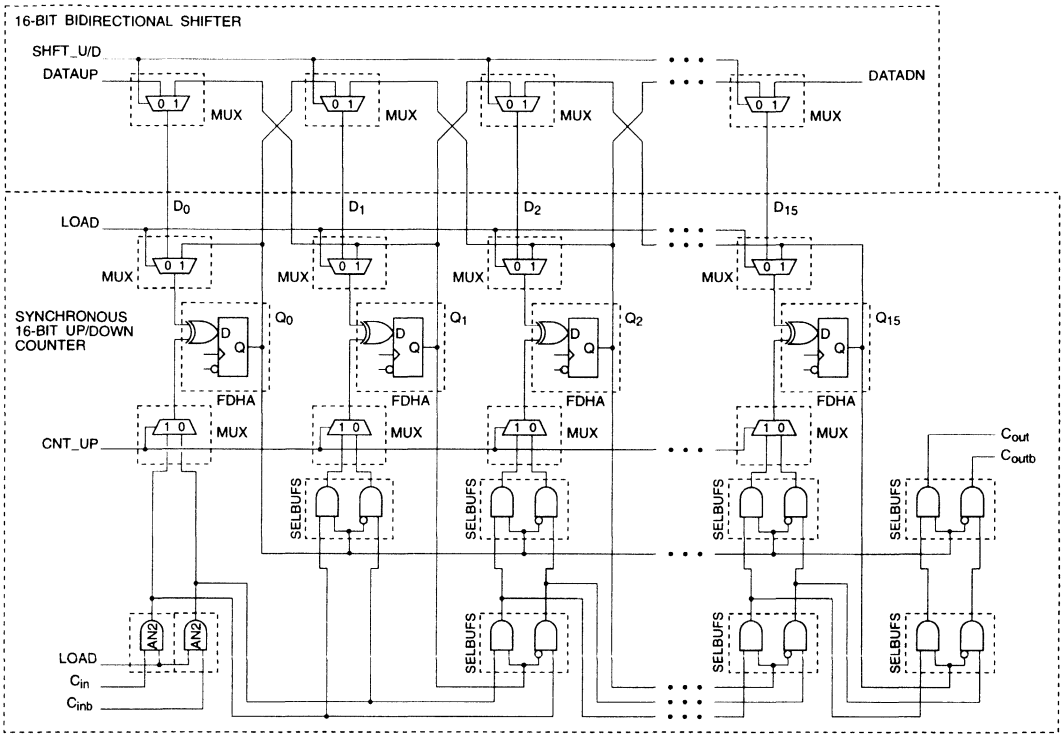


Table 1. Statistics 16-Bit Up/Down Counter/Shift Register

Counter/Shift Register	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Speed[2]
16-Bit	215	13 x 18	45.5 ns / 22 MHz

Notes:
1. Includes cells used as wires.
2. CLK → $C_{out,outb}$. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

9-Bit Programmable Terminal Counter

Introduction

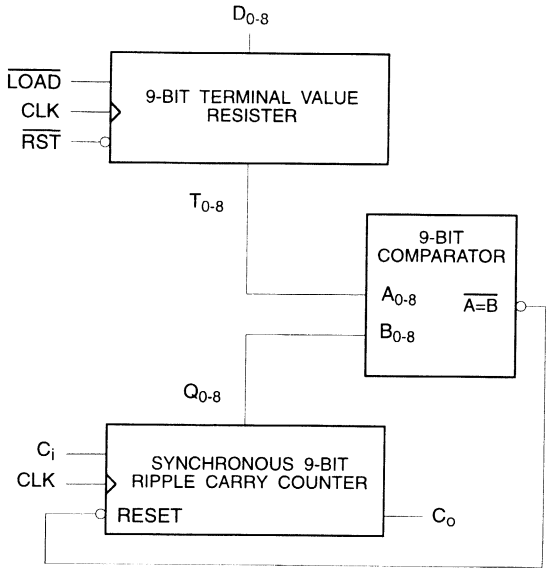
The AT6000 Series field programmable gate array (FPGA) lets the designer implement synchronous, programmable 9-bit terminal counters optimized for speed or layout area. A high-performance version is available that can operate at 33 MHz under the worst commercial operating conditions. If layout area is a consideration, a 33% smaller version is available that can still operate at 28 MHz worst case. An additional feature inherent in both counters is the ability to continue counting while a terminal value is being loaded into the terminal register.

Description

Figure 1 shows a block diagram of the counter. Both versions have essentially the same architectural structure. Pin CLK is the clock signal, RST the reset signal, and LOAD the load terminal value signal. CLK is a positive, edge-triggered synchronous signal, RST an active low, asynchronous signal, and LOAD an active low, synchronous signal. Pins D_0 through D_8 are the terminal value inputs, and pins Q_0 through Q_8 are the count bits. Pins C_i and C_o are the carry-in and carry-out signals.

Initial power-up of the AT6000 device resets all the registers in the counter and terminal register. Counting does not commence until a terminal value has been

Figure 1. 9-Bit Programmable Terminal Counter



7

0466A

loaded into the terminal register. Any 9-bit value can be loaded into the terminal register through the inputs D_{0-8} by holding LOAD low during the rising edge of CLK. Assuming C_i is asserted, the counter increments on the rising edge of CLK until the terminal value is reached on the outputs Q_{0-8}. On the next rising edge of CLK, the counter is synchronously reset to zero. Figure 2 shows the timing of the terminal value load and count operations for the circuit.

The schematic in Figure 3 shows the detailed implementation of the high-speed version of the circuit. The FDMUX macro is a two-to-one multiplexer that feeds a D-type flip-flop. A terminal value register composed of FDMUX macros lets a terminal value be loaded synchronously through D_{0-8}. The terminal value register holds the previously loaded value at its outputs. Counting does not commence until a non-zero value is loaded into the terminal value register.

A synchronous ripple-carry counter begins counting after a terminal value has been loaded into the terminal register. The counter is composed of FD, XO2, and AN2 macros—D-type flip-flops, two-input exclusive OR gates, and two-input AND gates respectively. Outputs Q_{0-8} feed into a comparator circuit composed of INV inverter gate, X02, and AN2 gates. The output of the comparator controls the initialization of the counter by checking Q_{0-8} against the terminal value. When Q_{0-8} is equivalent to the terminal value, the counter is reset to zero on the next rising edge of CLK.

The critical path of the circuit starts at Q_0, the first bit of the counter, travels through the comparator, and then back to the input of the first counter bit. Performance is enhanced by breaking the chain of AN2 gates in the comparator into three- and four-gate segments (Figure 4), then combining the output of each segment with a two-input NAND macro called ND2. By gating the D-type flip-flops of the counter with the output of the comparator, path delay is minimized and performance is enhanced.

Figure 5 shows the detailed schematic for the compact version. The terminal value register is exactly the same as in the high-speed version, but the outputs of the register are not inverted as they enter the 9-bit comparator. Instead, the outputs of the counter are inverted as they enter the comparator, thus improving layout compactness. An FDXOAN3 macro, a complex gate structure feeding a D-type flip-flop, is used to implement the 9-bit synchronous ripple-carry counter in only nine cells. As in the high-speed version, the critical path also resides in the comparator portion of the circuit.

The performance and utilization statistics for both versions are given in Table 1. Both implementations are available in schematic and layout form.

Figure 2. Timing of Load/Count Operation

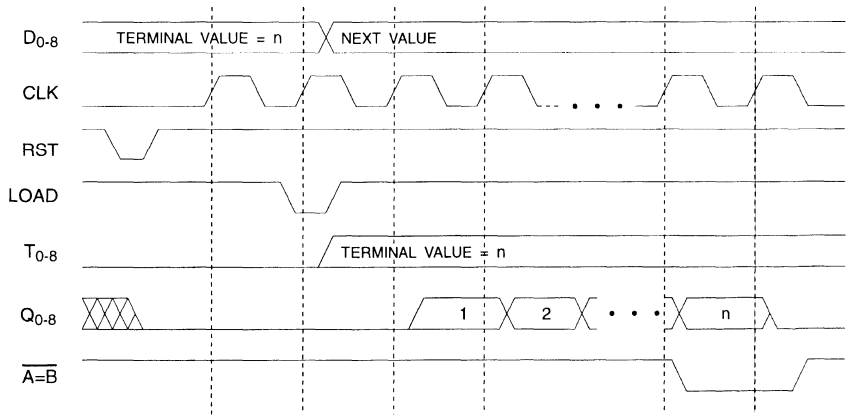


Figure 3. High-Speed Programmable Terminal Counter Architecture

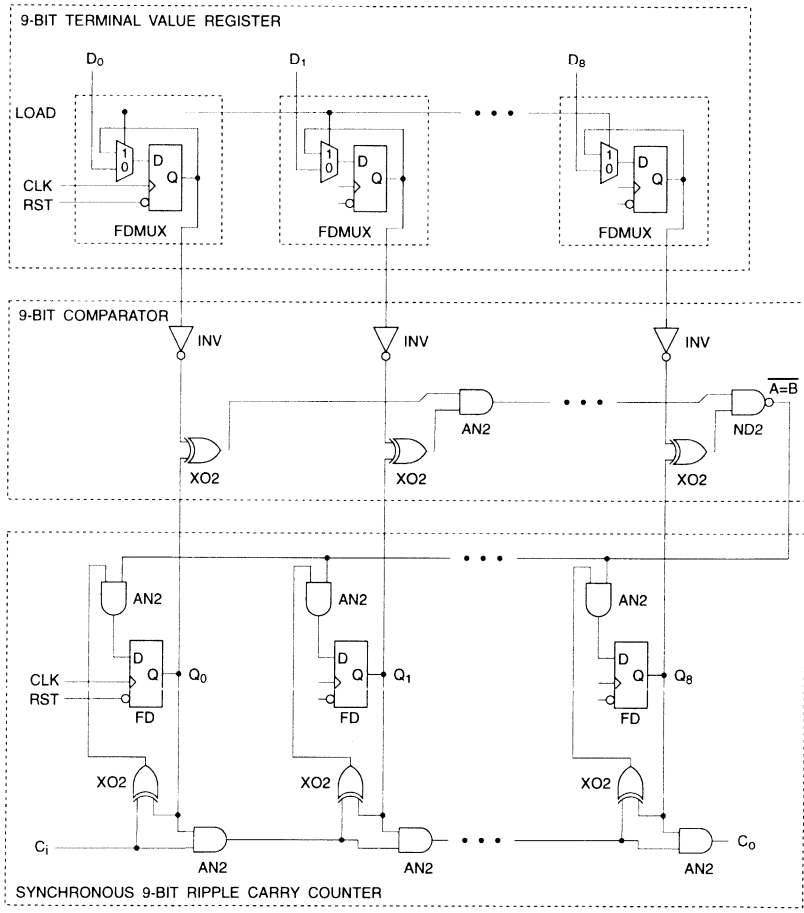


Figure 4. Schematic of Comparator Circuit

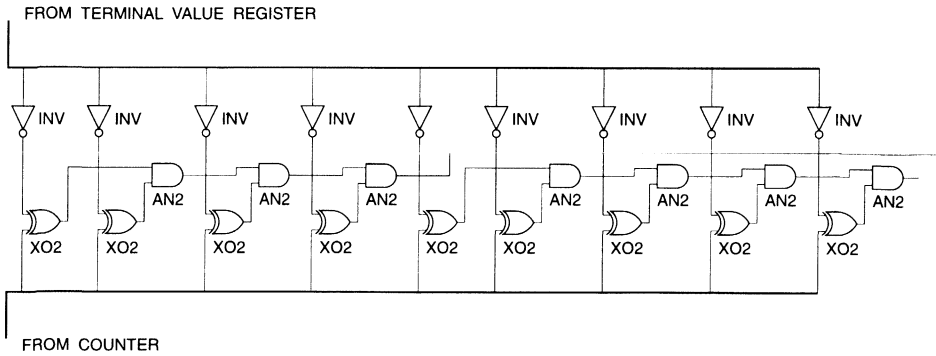


Figure 5. Compact Programmable Terminal Counter Architecture

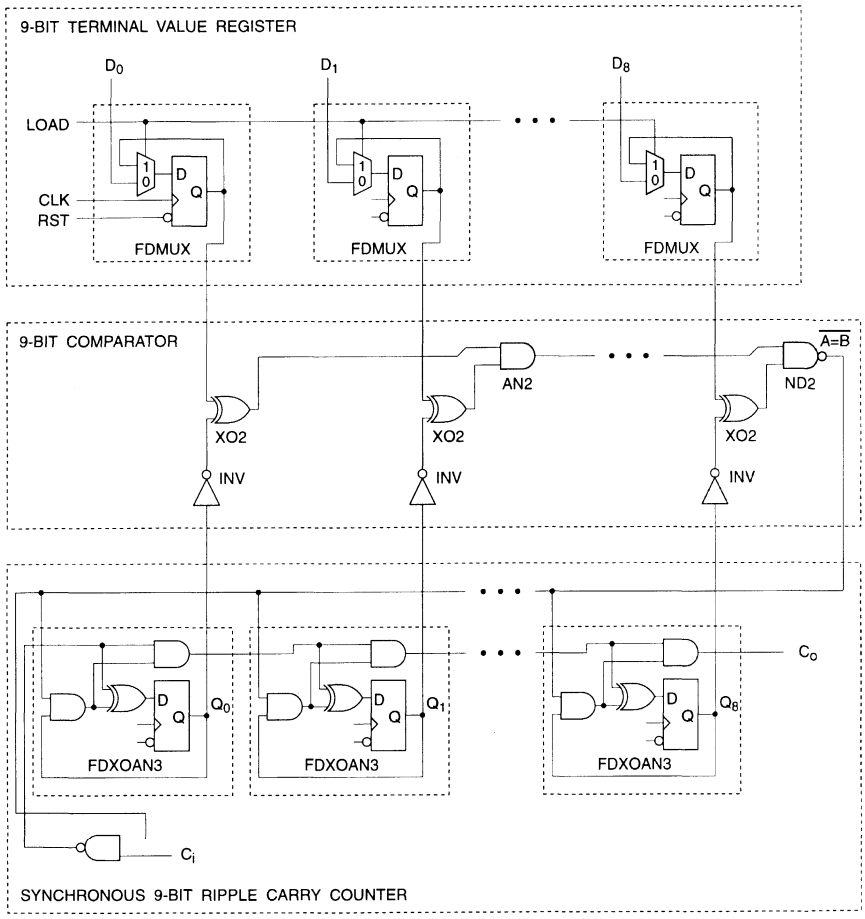


Table 1. Statistics for 9-Bit Programmable Terminal Counters

Programmable Terminal Counter	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Speed[2]
9-Bit (Compact)	69	10 x 7	35.7 ns / 28 MHz
9-Bit (High-Speed)	100	10 x 10	30.3 ns / 33 MHz

Notes:
1. Includes cells used as wires.
2. CLK → C_o. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

16-Bit Carry-Select Adder

By Frederick Furtek

Introduction

Ripple-carry adders are the simplest and most compact adders (they require as little as four cells per bit in the AT6000 architecture), but their performance is limited by a carry that must ripple from the least-significant to the most-significant bit. A carry-select adder implemented in the AT6000 achieves speeds 40% to 90% faster by performing additions in parallel and reducing the maximum carry path.

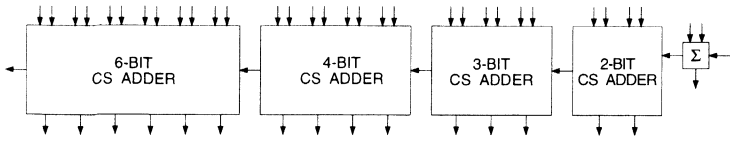
Description

A carry-select adder is divided into sectors, each of which—except for the least-significant—performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. The 16-bit carry-select adder of Figure 1, for example, is divided into sectors of lengths 1, 2, 3, 4, and 6, proceeding from least-significant to most-significant bit. The 4-bit sector of Figure 2 illustrates the general principle.

Within the sector, there are two 4-bit ripple-carry adders receiving the same data inputs but different carry-ins. The upper adder has a carry-in of zero; the lower adder a carry-in of one. The actual carry-in from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected.

Logically, the result is no different than if a single ripple-carry adder were used. The difference, of course, is in performance. Instead of having to ripple through four full adders, the carry now only has to pass through a single multiplexer. In the AT6000 implementation (Figure 3), that multiplexer is implemented in a single cell, and the carry path through the sector incurs only a wire delay, a local-bus delay, and a multiplexer delay. Table 1 lists sizes and speeds for 16-bit ripple-carry and carry-select adders implemented in the AT6000.

Figure 1. 16-Bit Carry-Select Adder



7

0467A

Figure 2. 4-Bit Sector (Schematic)

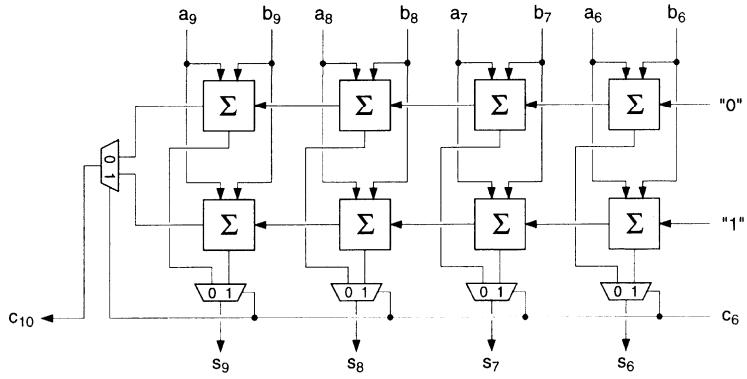


Figure 3. 4-Bit Sector (Layout)

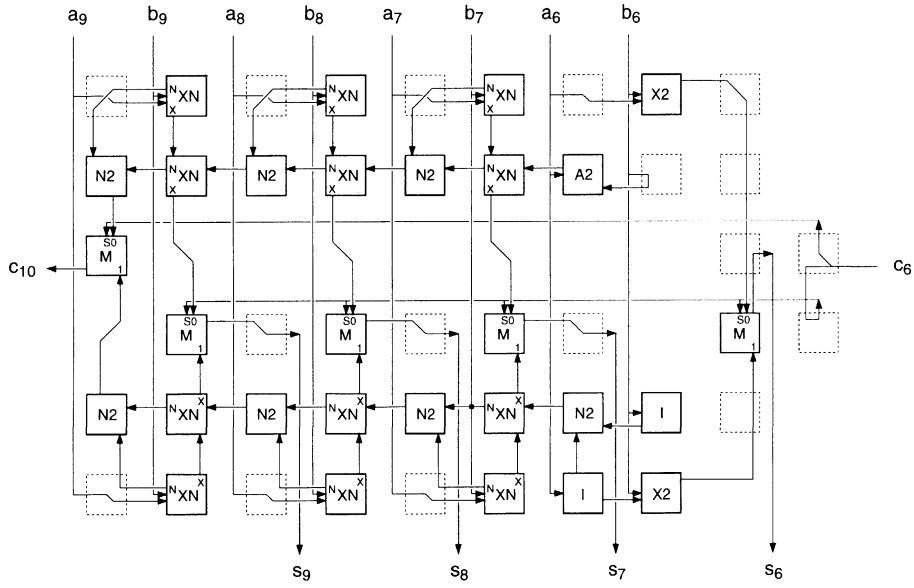


Table 1. Statistics for 16-Bit Adders

16-Bit Adder	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Speed (-4)[2]	Maximum Speed (-2)[2]
Ripple Carry	64	2 x 32	111.9 ns / 8.9 MHz	67.7 ns / 14.7 MHz
Fast Ripple Carry	96	6 x 16	87.2 ns / 11.4 MHz	51.6 ns / 19.3 MHz
Carry Select	222	6 x 37	63.4 ns / 15.7 MHz	35.8 ns / 27.9 MHz

Notes:
1. Includes cells used as wires.
2. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

Ripple-Carry Adders

By Frederick Furtek

Introduction

With a NAND and an XOR available simultaneously in a single cell, the AT6000 architecture is ideally suited for implementing arithmetic operations, including parallel adders. Ripple-carry adders—the simplest and most compact parallel adders—require as little as four cells per bit, and one layout has a carry delay of only one cell per bit.

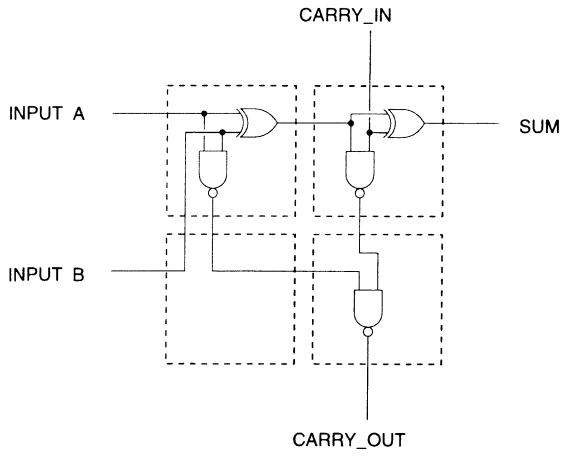
Description

In the AT6000 architecture, a NAND and an XOR—basic building blocks of binary arithmetic—are available simultaneously in a single cell. The NAND/XOR is used in making full adders (FAs), which, in turn, are used in creating parallel adders.

A full adder has three binary inputs—two addends and a carry_in, and two outputs—sum and carry_out. The sum is the exclusive OR (XOR) of the three inputs, while carry_out is the majority (two out of three) of the three inputs. The simplest and most compact full-adder layout in the AT6000 architecture uses just four cells (Figure 1). The carry_in and carry_out, moreover, are aligned so that an n-bit adder occupying $4n$ cells is created by simply abutting n full adders. An 8-bit parallel adder constructed from these adders uses only 32 cells (Figure 2).

A second full-adder layout (Figure 3) uses six cells, plus a local bus, but the carry now

Figure 1. Full Adder: Compact Layout



propagates through only one cell per bit instead of the two cells per bit of the adder in Figure 1. This reduced delay in the carry path produces ripple-carry adders that run about one-third faster. An examination of the circuit shows that the sum output is still the XOR of the three full-adder inputs (the adder has only three distinct inputs and two distinct outputs; the carry_in and carry_out signals are replicated to satisfy the needs of the lay-out). The carry_out is still the majority of the three inputs although it is now constructed from two AND gates feeding an XOR. A little Boolean algebra shows that the function is identical to the three NAND gates used above (Figure 1) to produce the carry_out.

The size and performance of various ripple-carry adders are summarized below for the -4 and -2 speed grades (Table 1).

Figure 2. 8-Bit Ripple-Carry Adder

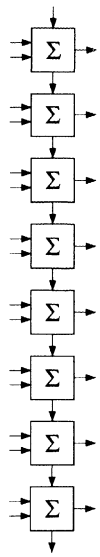


Figure 3. Full Adder: Fast Layout

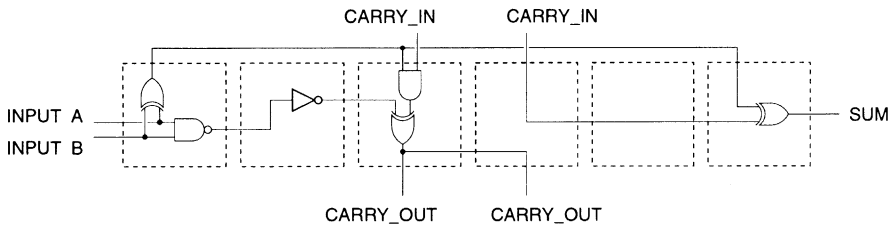


Table 1. Statistics for Ripple-Carry Adders

Adder	Cell Count)[1]	Minimum Bounding Box (X x Y)	Maximum Speed (-4)[2]	Maximum Speed (-2)[2]
8-Bit Ripple Carry	64	2 x 16	59.1 ns / 16.9 MHz	35.7 ns / 28.0 MHz
8-Bit Fast Ripple Carry	48	6 x 16	51.2 ns / 19.5 MHz	30.0 ns / 33.3 MHz
16-Bit Ripple Carry	64	2 x 32	111.9 ns / 8.9 MHz	67.7 ns / 14.7 MHz
16-Bit Fast Ripple Carry	96	6 x 16	87.2 ns / 11.4 MHz	51.6 ns / 19.3 MHz
32-Bit Ripple Carry	128	2 x 64	217.5 ns / 4.5 MHz	131.7 ns / 7.5 MHz
32-Bit Fast Ripple Carry	192	6 x 32	159.2 ns / 6.2 MHz	94.8 ns / 10.5 MHz

Notes:
1. Includes cells used as wires.
2. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

Barrel Shifter

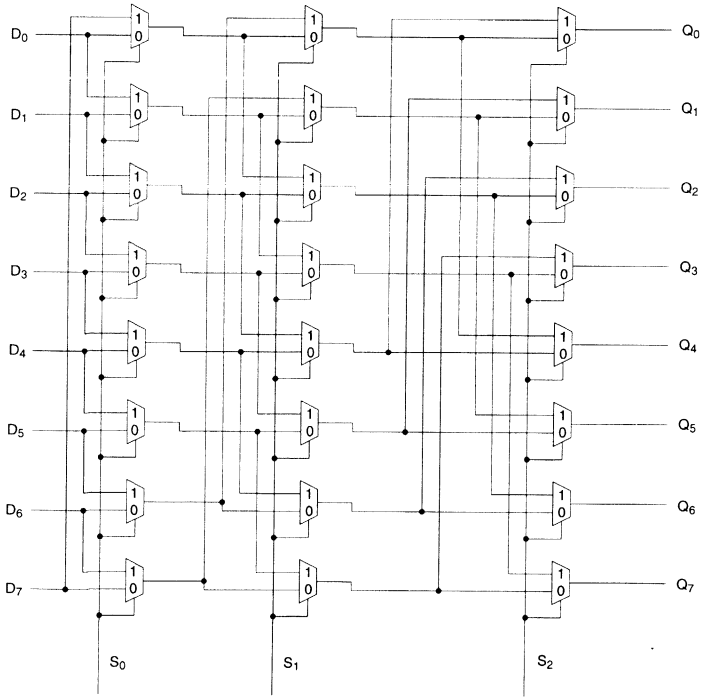
Introduction

The AT6000 Series field programmable gate array (FPGA) allows the designer to implement fast compact 8-bit barrel shifters, and modular shifters that can be easily sized for specific needs. Performance is enhanced by a unique feature of the busing architecture that enables the select control lines to be distributed across the data path with minimal skew, and a cell architecture that allows a two-to-one multiplexer (MUX) to be realized in just one cell.

Description

Figure 1 shows the fast, compact barrel shifter. Depending on the encoded shift control lines, $S_{0\text{-}2}$, the data inputs $D_{0\text{-}7}$ are shifted when they reach the outputs $Q_{0\text{-}7}$. If S_0 is asserted and S_1 and S_2 are unasserted, the value at $D_{0\text{-}7}$ is passed to the next most significant Q output. For example, D_0 is passed to Q_1, and D_1 passed to Q_2, while D_7 wraps around and is passed to Q_0. If none of the shift controls are asserted, the data inputs $D_{0\text{-}7}$ are passed to the corresponding outputs $Q_{0\text{-}7}$ without being shifted.

Figure 1. Fast, Compact Barrel Shifter with Encoded Shift Control



Field Programmable Gate Array

Application Note

7

0469A

Figure 2 shows the modular barrel shifter. The shift line S_{0-6} is coded such that the data is shifted one bit position for every shift line that is asserted. The bit-width and depth of the modular barrel shifter can be easily expanded because of the efficient interconnections network. Each multiplexer output connects to its two nearest neighbors in the next column. The multiplexers on the borders are easily connected via a local bus wire. Bit-slice structures of arbitrary bit-width can be composed and then concatenated to form barrel shifters tailored to specific design needs.

The implementation in Figure 1 is faster because it contains fewer multiplexers. The critical path of the second implementation has more than twice as many MUX cells in series. The delay through a multiplexer cell is 2.7 times the delay through a wire cell, so the delay through three wire cells is approximately equal to the delay through one multiplexer cell. With both implementations being approximately the same size, and the critical paths containing about the same quantity of cells, the path with the lesser amount of multiplexers will be faster.

Figures 1 and 2 reflect the relative physical placement of the logical cells that compose the barrel shifter function and the busing structure that performs the interconnection.

Table 1 gives performance and utilization statistics for both implementations. Both implementations are available in schematic and layout form.

Figure 2. Modular Barrel Shifter with Non-coded Shift Control

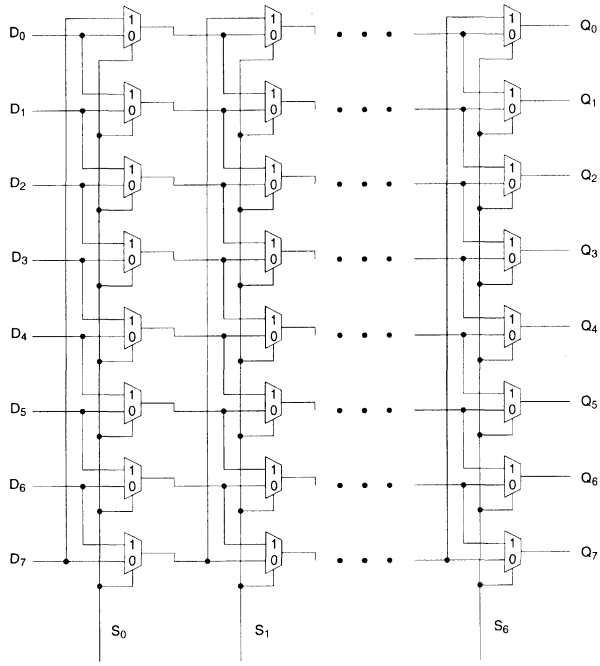


Table 1. Statistics for Barrel Shifter

Version	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Speed[2]
Fast (3 Control Bits, Encoded)	112	8 x 14	28 ns / 35.7 MHz
Modular (7 Control Bits, Encoded)	126	13 x 10	44 ns / 22.7 MHz

Notes:
1. Includes cells used as wires.
2. $D_{0-7} \rightarrow Q_{0-7}$. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

24-Bit Magnitude Comparator with 50 ns Response

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a magnitude comparator that can compare two 24-bit binary integers in 50 ns.

Description

Figure 1 shows the structure of the magnitude comparator. Given two numbers $A_{0\text{-}23} > B_{0\text{-}23}$, the output GT will become asserted. If $A_{0\text{-}23}$ is less than or equal to $B_{0\text{-}23}$, GT remains unasserted.

The logic necessary to compare two numbers can be derived iteratively according to four equations. The first two determine the largest number:

1. $T_n = A_n B_n'$

For $n = 0$, where n is the significant bit.

2. $T_n = A_n B_n' + T_{n-1}(A_n + B_n')$

For $n = 1$ *to* 23, where n is the significant bit.

The second two determine if the numbers are equal:

3. $E_n = A_n' B_n + A_n B_n'$

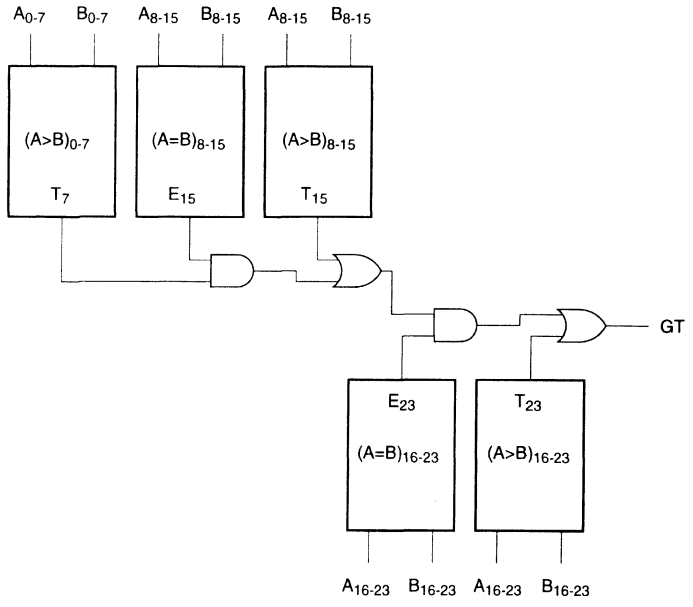
For $n = 0$, where n is the significant bit.

4. $E_n = (A_n' B_n + A_n B_n') + E_{n-1}$

For $n = 1$ *to* 23, where n is the significant bit.

Equation T_n could be used exclusively to generate the logic for GT, but the circuit would have a delay equivalent to 48 two-in-

Figure 1. Structure of 24-Bit Magnitude Comparator



Field Programmable Gate Array

Application Note

7

0470A

put NAND (ND2) gates for the worst-case comparison conditions.

To improve performance, the comparator is partitioned into three stages that each compare 8-bit portions of the two numbers. Thus, the parallel comparison of the three 8-bit portions of both numbers is faster than a single 24-bit implementation. The delay through an 8-bit stage is equivalent to 16 two-input NAND (ND2) gates.

Within each stage, the circuitry performs a bit-wise comparison starting between the most significant A_n and B_n bits within each stage, and asserts stage $T_{(m+1)(N/3)-1}$ (where stage m is 0 through 2, and $N = 24$ the bit-width of the compared numbers), if the most significant A_n is asserted and B_n is unasserted ($A_n > B_n$). If the most significant A_n and B_n bits are equal, then a pair of lesser significant bits within the stage must determine if the magnitude of the aggregate quantity of A bits is greater than the B bits in stage m. Also, the circuitry within each stage performs a bit-wise comparison on each pair of bits and asserts $E_{(m+1)(N/3)-1}$ if the 8-bit portions are equivalent.

The $T_{(m+1)(N/3)-1}$ and $E_{(m+1)(N/3)-1}$ outputs from each 8-bit stage are fed into some logic to derive GT. This logic can be determined according to the equation:

Figure 2. Implementation of Magnitude Comparator

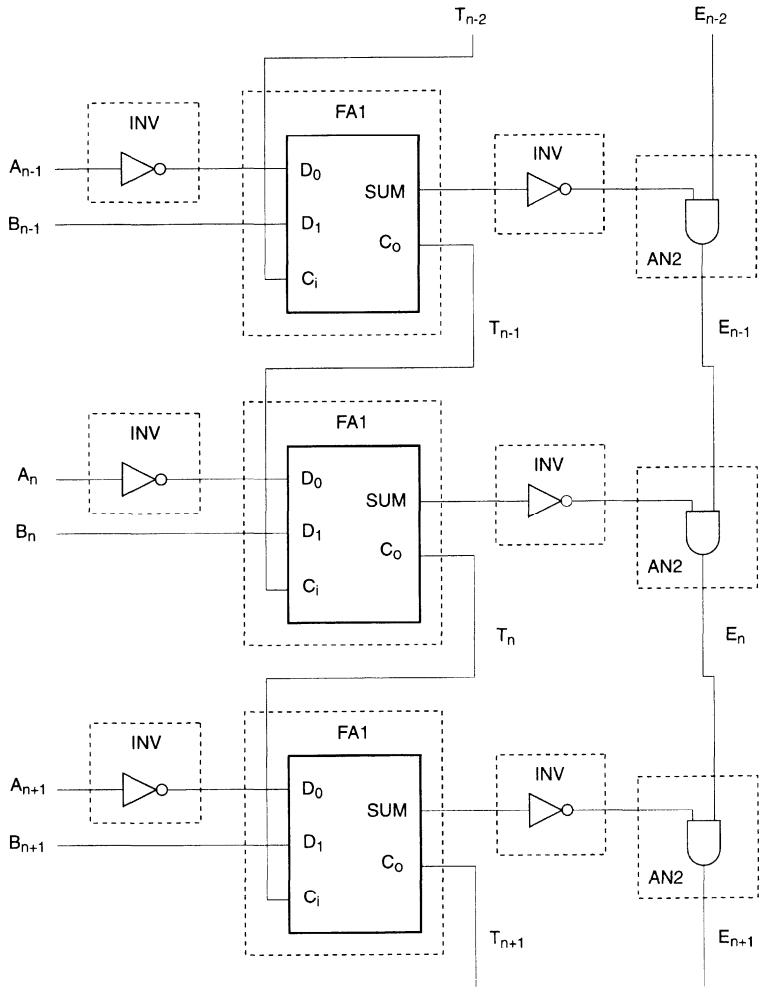
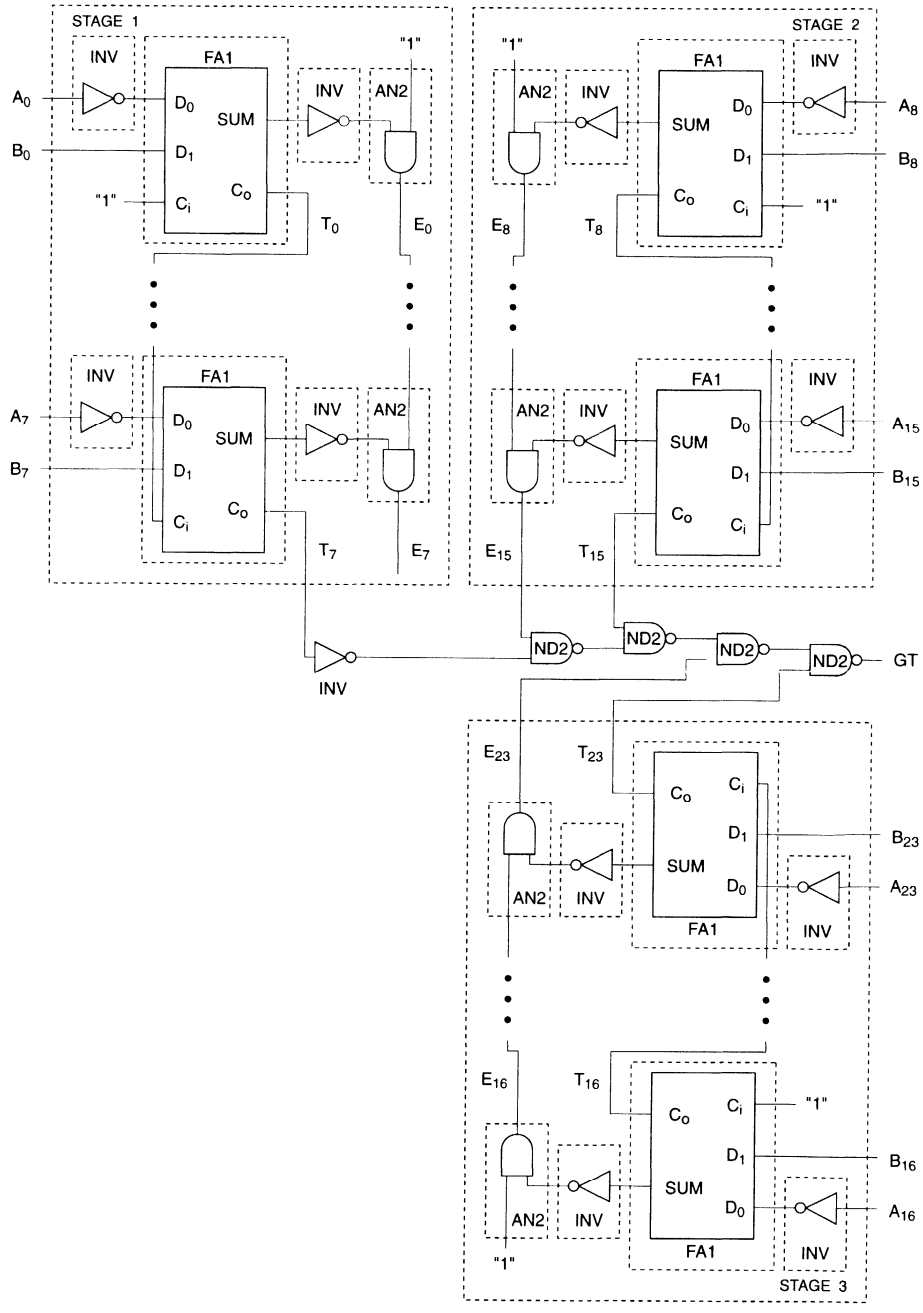


Figure 3. Magnitude Comparator is Composed of Three 8-Bit Stages



1. $S_m = T_{(m+1)(N/3)-1}$

Where $m = 0$ is the significant stage and $N = 24$ the total number of bits.

2. $S_m = T_{(m+1)(N/3)-1} + E_{(m+1)(N/3)-1}S_{m-1}$

For $m = 1$ *to* 2, where $m = 0$ is the significant stage and $N = 24$ the total number of bits.

The final result S2 is equivalent to GT.

Precedence in determining magnitude is given to the most significant stage in which the bit portions are different when all other more significant stages have equivalent bit portions. For example, if T_{15} and E_{15} become unasserted, which means that the B bits are of greater magnitude than the A bits, and E_{23} asserts that the A and B bits in its more significant stage are equivalent, then GT will remain unasserted regardless of the results in the less significant stages.

The equations for T_n and E_n can be implemented as shown in Figure 2. FA1 is a single-bit full-adder macro that is combined with inverters (INV) and two-input AND gates (AN2) to realize the function for T_n and E_n. A 24-bit comparator is built as shown in by composing three 8-bit stages and using the S_n logic to link each stage (Figure 3).

Performance and utilization statistics for the magnitude comparator are given in Table 1. This implementation is available in schematic and layout form.

Table 1. Statistics for 24-Bit Magnitude Comparator

Comparator	Cell Count[1]	Minimum Bounding Box (X x Y)	Wire Cells	Maximum Delay[2]
24-Bit	246	12 x 33	98	50 ns / 20 MHz

Notes:
1. Includes cells used as wires.
2. $A_0 \rightarrow$ GT. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

16-Bit Four-to-One Multiplexer with 15-ns Delay

Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a 16-bit, four-to-one multiplexer with a 15-ns delay from the select control to the most significant output bit. Performance is enhanced by a unique feature of the busing architecture that enables the select control lines to be distributed across the multiplexer data path with minimal skew.

Description

Figures 1 and 2 show the relative physical placement of the logical cells that compose the multiplexer function and the busing structure that performs the interconnection. Four 16-bit input buses, $A_{0\text{-}15}$, $B_{0\text{-}15}$, $C_{0\text{-}15}$, and $D_{0\text{-}15}$, can be multiplexed to a 16-bit output bus $F_{0\text{-}15}$. Two select lines S_0 and S_1 determine which of the input buses are multiplexed to the output. Figure 1 shows several four-to-one multiplexer bits, each implemented in four cells. A cell can be configured as a two-to-one multiplexer (MUX21). Every MUX21 is tied to either the S_0 or S_1 select lines. S_0 controls 32 MUX21 cells, and S_1 controls 16 MUX21 cells.

Typically, distribution of a signal to such a large number of cells would cause unacceptable skew between the cells closest and furthest from the source. By aligning the multiplexers, and routing a single wire to every one, the most efficient signal distribution method is realized. However, the load on the wire might unacceptably decrease its slew rate. Buffering the wire after routing it to a certain number of multiplexers would improve the slew rate, but additional cells would be required for the buffering. Skew would also be introduced as buffer stages are added to the distribution network. Other signal distribution methods have been shown to have minimal skew and optimal slew rate, but they require more logic resources.

Using express buses, skew is minimized and slew is improved by segmenting the load along each signal. Figure 2 shows that the express and local buses can distribute S_0 and S_1 without using additional logic cells. S_0 passes from a local bus into a repeater—a programmable cross-bar buffer—and is routed onto the express bus. At each repeater stage, taps are taken off onto the local bus and into the multiplexers. Since the express bus is essentially an unloaded wire, its delay is much less than that of the local bus, which is loaded by multiplexer select inputs. Although signal propagation of S_0 and S_1 is serialized from the source output through several repeater stages to the final inputs, this distribution method is the most efficient for performance and cell utilization.

Table 1 gives performance and utilization statistics for the multiplexer. It is available in schematic and layout form.

Figure 1. Schematic of Multiplex Function for Several Output Bits

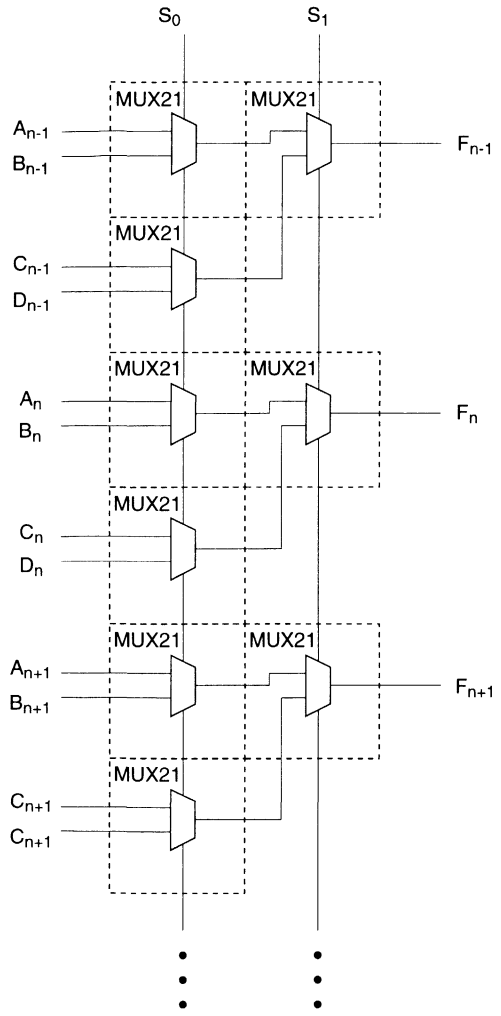


Figure 2. Equivalent Layout with Busing Structure

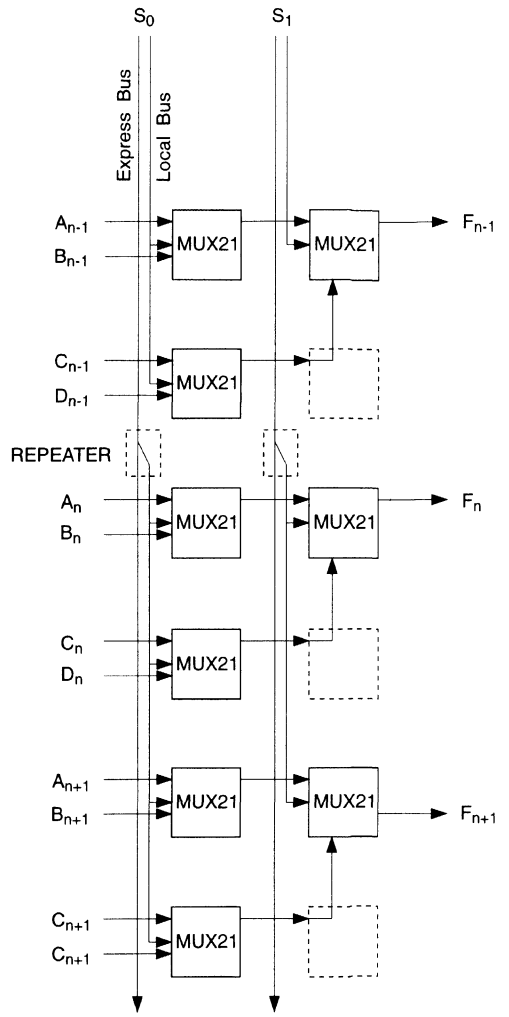


Table 1. Statistics for Four-to-One Multiplexer

Multiplexer	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Delay[2]
16-Bit	64	2 x 32	15 ns / 66.7 MHz

Notes:
1. Includes cells used as wires.
2. $S_0 \rightarrow F_{15}$. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

8-Bit, S-P/P-S "Corner-Bender" Data Converter

Introduction

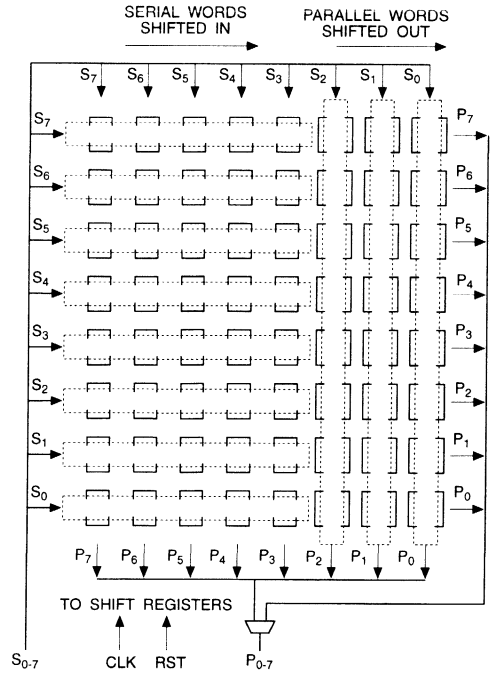
With the proliferation of computer and voice networks that carry digitized analog data, data conversion applications have become commonplace. For example, the use of time-division multiplexing in broadcasting and receiving circuitry requires fast serial-to-parallel (S-P) and parallel-to-serial (P-S) data conversion. Using the AT6005 device, two S-P/P-S corner-bender circuits were implemented: one optimized for area and power consumption, the other for speed and expandability.

Description

Figure 1 is the functional representation for an 8-bit corner-bender. CLK is the clock input signal and RST is the asynchronous reset. RST is active low. Pins S_0 through S_7 are the data inputs; pins P_0 through P_7 are the converted data outputs.

The corner bender accepts 8-by-8 blocks as input. Each block is eight bits wide and arrives serially over eight clock cycles. The corner bender transforms each input block into an 8-by-8 output block such that bits aligned in parallel in the input block are aligned serially in the output block, and vice versa.

Figure 1. Functional Representation of Corner Bender



0472A

The two implementations—low-area/low-power and high-speed/expandable—are functionally identical. Initial power-up of the AT6005 device resets all user registers, so the circuit begins data conversion on the first rising edge of CLK after configuration.

In serial-to-parallel mode, the P_{0-7} outputs remain low for the first seven clock cycles. After the rising edge of the eighth clock cycle, the first 8-bit serial data word from S_0 is available at the P_{0-7} outputs. The S_1 serial word is available after the rising edge of the next clock (Figure 2). Subsequent serial words are available on the rising edge of every clock until RST is asserted. Asserting RST at any time clears the registers and inhibits the conversion.

The first implementation minimizes area and power consumption, but still operates at up to 22 MHz in the AT6005-4 and 31 MHz in the AT6005-2.

Figure 3 shows the gate-level equivalent of the register block structure used for conversion. A single AT6005 cell is configured as a two-input multiplexer feeding a D-type flip-flop (FDMUX).

After the rising edge of every eighth clock cycle, two-to-one multiplexers switch the direction of the data flow into the register from west-to-east to north-to-south. The boundary registers that feed the outputs, P_{0-7}, are also switched after the rising edge of every eighth clock cycle. Pins P_{0-7} receive parallel (or serial) data from the boundary registers on the axis perpendicular to, and on the opposite side of, the serial (or parallel) data input.

The second implementation maximizes throughput and can operate at 52 MHz (AT6005-4) and 75 MHz (AT6005-2), but requires almost twice the area and 25 percent more power per MHz than the first.

A secondary set of registers is used to latch a parallel (or serial) 8-bit word from a serial (or parallel) data register on the rising edge of every eighth clock cycle. Figure 4 shows the gate-level equivalent of the register block structure used for the conversion. The shift registers employ D-type flip-flops (FD); the secondary registers use FDMUX macros.

At the rising edge of every eighth clock cycle, the secondary registers load a parallel (or serial) 8-bit data word from the serial (or parallel) shift registers. On subsequent clock cycles, the parallel (or serial) words are shifted from each set of secondary registers until the words reach P_{0-7}.

The slower implementation requires fewer cells and uses less area, but has a longer critical path delay and hence less throughput than the faster implementation. In the first implementation, the longest interconnection occurs between the registers containing the most significant bit, S_0, which feeds the two-to-one multiplexer driving P_7, MUX21 (Figure 5).

The longest path between the register and multiplexer spans nearly half the circumference of the layout, which is four times longer than the longest path in the second implementation. Each flip-flop in the second circuit connects to only its two nearest neighbors, making the interconnects fairly equal in length. As a result, the second implementation can be expanded without significant performance loss. Table 1 gives a comparison of the performance and utilization statistics for the two corner benders. Both circuits are available in schematic and layout form.

Figure 2. Timing Diagram of Serial-to-Parallel Corner-Bender Operation

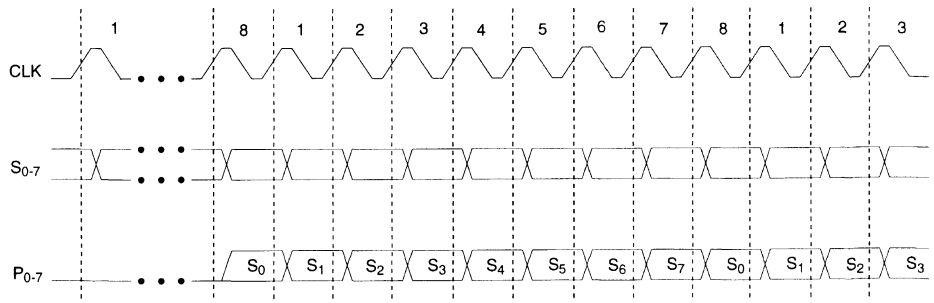


Figure 3. Schematic of Low-Area/Low-Power Core

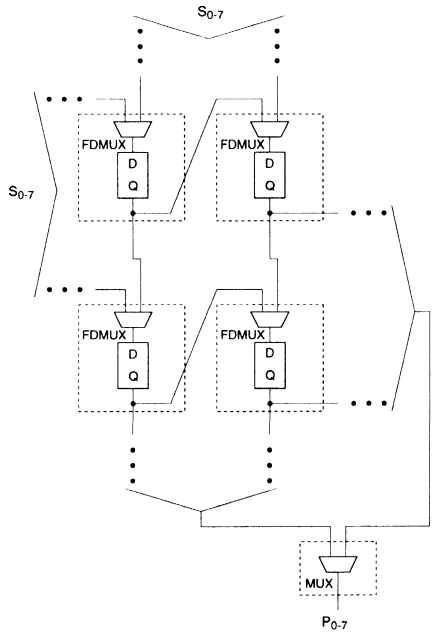


Figure 4. Schematic of High-Speed/Expandable Core

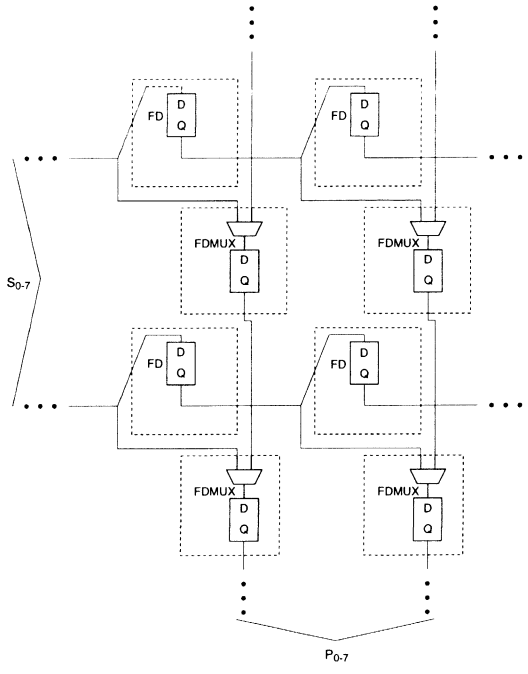


Figure 5. Interconnect Scheme of First Implementation

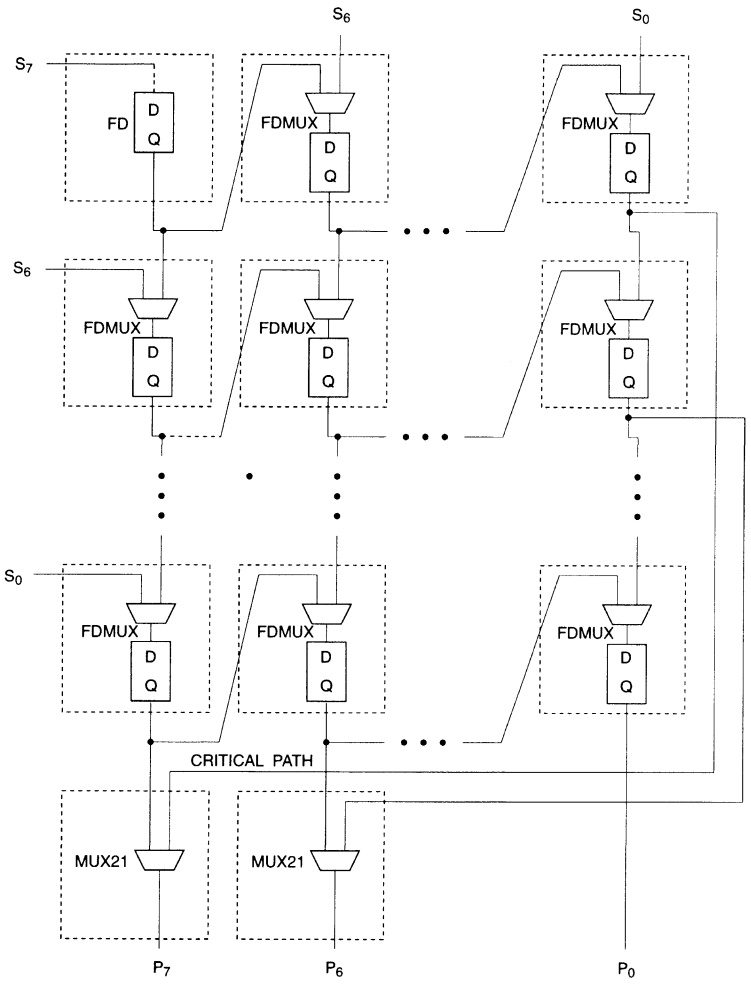


Table 1. Statistics for Corner Benders

Corner Bender	Cell Count[1]	Minimum Bounding Box (X x Y)	Maximum Speed AT6005-4[2]	Maximum Speed AT6005-2[2]
Low Area/Low Power	164	16 x 12	45.5 ns / 22 MHz	32.3 ns / 31 MHz
High Speed/Expandable	260	15 x 19	19.2 ns / 52 Mhz	13.3 ns / 75 MHz

Notes:
1. Includes cells used as wires.
2. CLK → P_0. Worst-Case Commercial Operating Conditions: 70°C, 4.75 V.

16-Word by 8-Bit FIFO

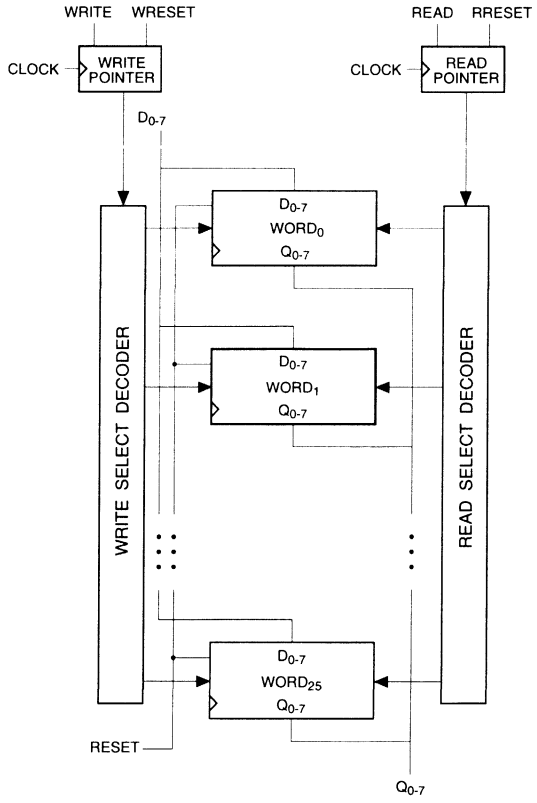
Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a synchronous first-in, first-out (FIFO) register buffer with a word width and depth tailored to specific design needs. A 16-word FIFO with each word being eight bits is constructed and analyzed in the AT6005-2 device, and shown to have 15 MHz performance

Description

Figure 1 shows a functional block diagram of the FIFO architecture. Data on inputs D_{0-7} is latched into a particular word register on the rising edge of CLOCK when WRITE is asserted. When READ is asserted, the outputs Q_{0-7} are driven by a new word register. The write and read pointers, together with the select decoder logic, determine the particular register or registers that are the target of the write operation and the source of the

Figure 1. Architecture of 16 x 8 FIFO



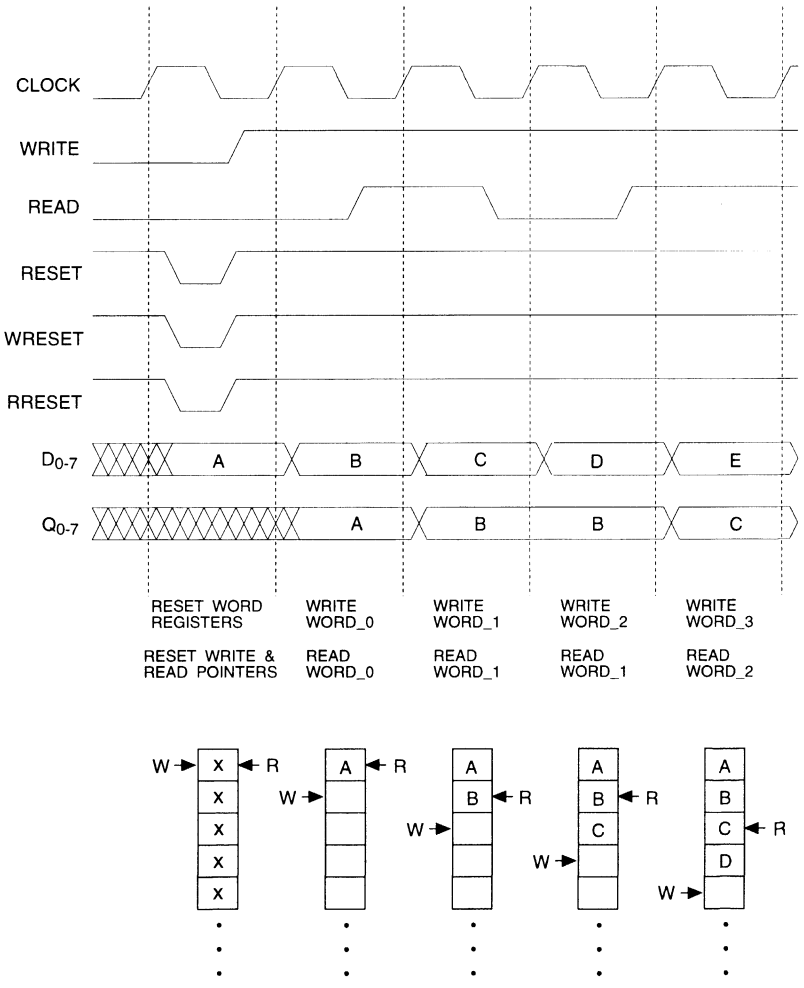
0473A

read operation. Individual read or write operations can be executed every clock cycle when either the READ or WRITE signals are asserted. Simultaneous write and read operations are also possible to any one word register or combination of two registers. If neither the READ or WRITE signals are asserted, the pointers maintain their current address. After a write operation occurs, the write pointer is automatically updated to point to the next word register, and then awaits the next write operation. The read pointer allows the data of a particular word register to be continuously available until the next read operation, after which new data from the next word register is accessed. Essentially, the read pointer points to the last word that was read and the write pointer points to the next word to be written.

The RESET, WRESET, and RRESET signals control the initialization of various portions of the FIFO. When RESET is set low, the word registers are immediately cleared. RESET is an asynchronous signal that causes all bits within each word register to be set low. WRESET and RRESET are synchronous initialization signals for the write and read pointers. If WRESET is taken low and then high before the rising edge of CLOCK, the write pointer is set to the first word register. A write operation can then commence on the next rising edge of CLOCK if WRITE is asserted. The RRESET signal controls the read pointer in the exact same manner. Figure 2 shows the operation of the FIFO from the relative timing of the control signals.

A schematic of the word registers is shown in Figure 3. Each bit of the data word is stored in an FDMUX macro, which is a two-

Figure 2. Relative Timing of FIFO Control Signals



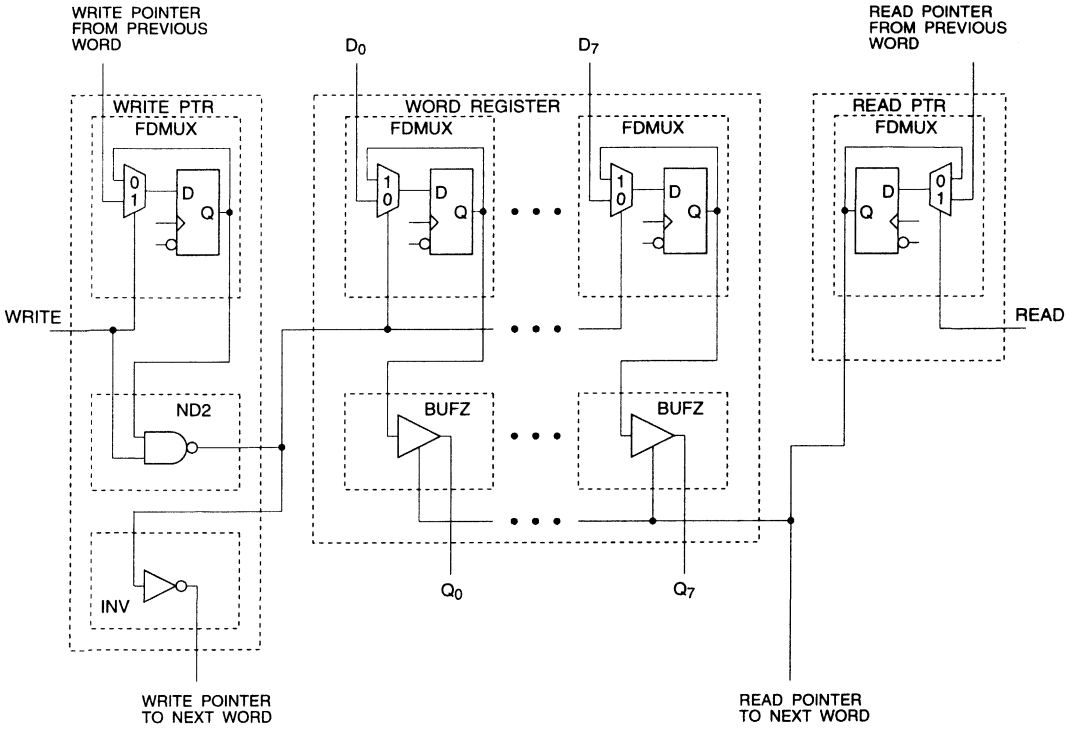
to-one multiplexer feeding a D-type flip-flop. If the word register is selected for a write operation, the two-to-one multiplexer chooses D_{0-7} as the input to be latched into the D-type flip-flop on the next rising edge of CLOCK. If the word register is not chosen for a write operation, the two-to-one multiplexer recirculates the data value already present in the D-type flip-flop. When a READ operation is initiated, the logic values present at the D-type flip-flop outputs are passed through the tri-state output buffers BUFZ onto an internal tri-state bus that ties together the output of every word register. Since the inputs D_{0-7} and outputs Q_{0-7} enter and exit on different wires, simultaneous write and read operation can occur on the same clock cycle.

Incorporated into each word register is a portion of the read and write pointer logic. The write pointer is a controlled shift register that is 16 bits in length. Upon initialization the first bit in the shift register is set to a logical "one" value, and all other bits are reset low. After a write operation occurs to the first word register, the "one" is passed to the next bit in the write pointer shift register at the rising edge of CLOCK. This "one" bit will continue to loop around the shift register whenever WRITE is asserted upon the rising edge of CLOCK. As the "one" is passed along, it allows a write operation to occur to the word register. The read pointer is implemented in essentially the same manner.

In the AT6000 architecture, implementing the write and read pointers as controlled shift registers has several advantages over controlled counter/decoder methods. For example, several 5-bit modular 16 counters together with several 5-bit to 16-bit decoders could be used to implement the read and write pointers in a controlled counter/decoder approach. Although the counters would use far less flip-flops, the decoder logic would be five times as large as in the controlled shift register method. More control signals would also have to be bused to every word register since in the controlled counter/decoder method every output bit of the counters must be used as a select control for the decoders of both the read and write pointers. The additional decoder logic and busing necessary for the controlled counter/decoder makes it ostentatiously large. Since every cell in the AT6000 architecture contains a D-type flip-flop, the controlled shift register approach is more efficient than the controlled counter/decoder approach.

Figure 4 shows the initialization logic along with several word registers. The initialization logic synchronously allows either the write or read pointers to be individually or simultaneously

Figure 3. Modular Word Register Schematic



reset to point to the first word register. The word registers can be asynchronously cleared. For this example, 16-word registers are linked together to form a 16-word FIFO, with each word being eight bits in length. The modular construction allows the concatenation of word registers to form a FIFO of any length. The word registers can also be widened as long as the portions of the write and read pointers are maintained on either side. Only one unique register is needed to hold the initialization logic to mark the first word of the FIFO.

The performance and utilization statistics for the 16-word by 8-bit FIFO are given in Table 1. This implementation is available in schematic and layout form.

Figure 4. Architecture of 16-Word x 8-Bit FIFO

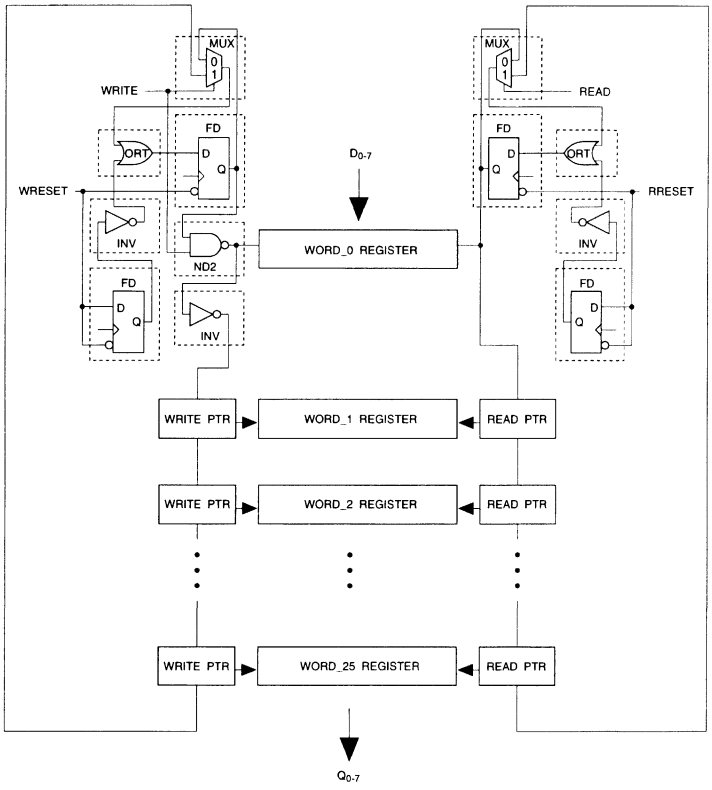


Table 1. 16 x 8 FIFO

FIFO	Cell Count[1]	Minimum Bounding Box (X x Y)	Cells Per Bit-4[2]	Maximum Speed[3]
16-Word by 8-Bit	653	20 x 35	5	66.7 ns / 15 MHz

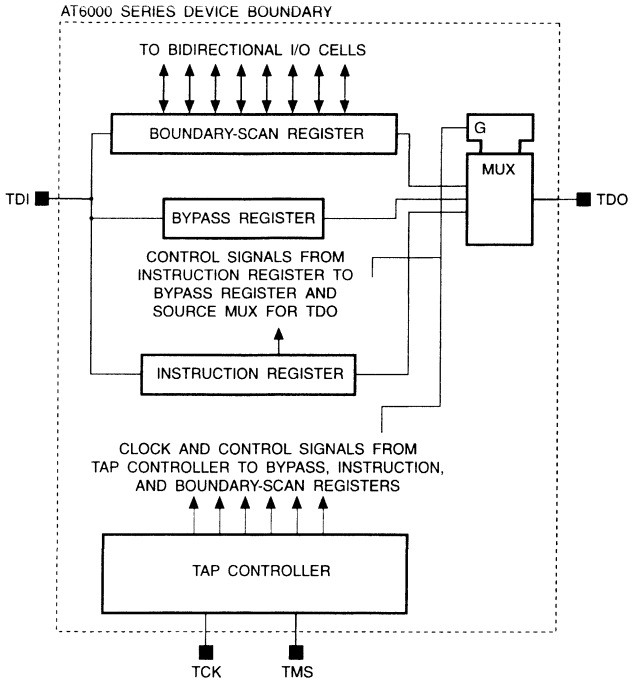
Notes:
1. Includes cells used as wires.
2. Amortizes the quantity of cells used for write and read pointers in each 8-bit word register over the cell count for each bit of the register. A 16-bit word register would use 4.5 cells per bit.
3. READ → Q_{0-7}. Worst-Case Commercial Operating Conditions: CLK → C_o, 70°C, 4.75 V.

IEEE 1149.1-1990 Standard Test Access Port and Boundary-Scan

Introduction

For system or board diagnostics, AT6000 Series devices can be programmed with the 1149.1 standard test logic and then reprogrammed for normal operation when the diagnostics are complete. The area and performance overhead of the test logic does not impact normal operation in the device because it is replaced by the logic for normal function. All mandatory test instructions can be executed with this portable test logic configuration, which guarantees conformance to the 1149.1 standard. The 1149.1 standard provides a consistent mechanism for confirming that each component in a system performs its required function. Since AT6000 devices are factory- tested with test patterns that exercise all the programmable features, integrity is insured without having to rely on standard test logic. Standard test logic is best suited for checking the interconnections between devices on the board. Boards are often multi-layer and double-sided, making traditional board test methods, like the bed-of-nails approach, expensive and impractical.

Figure 1. Block Diagram of 1149.1 Test Logic Architecture



0474A

Recommended Test Procedure

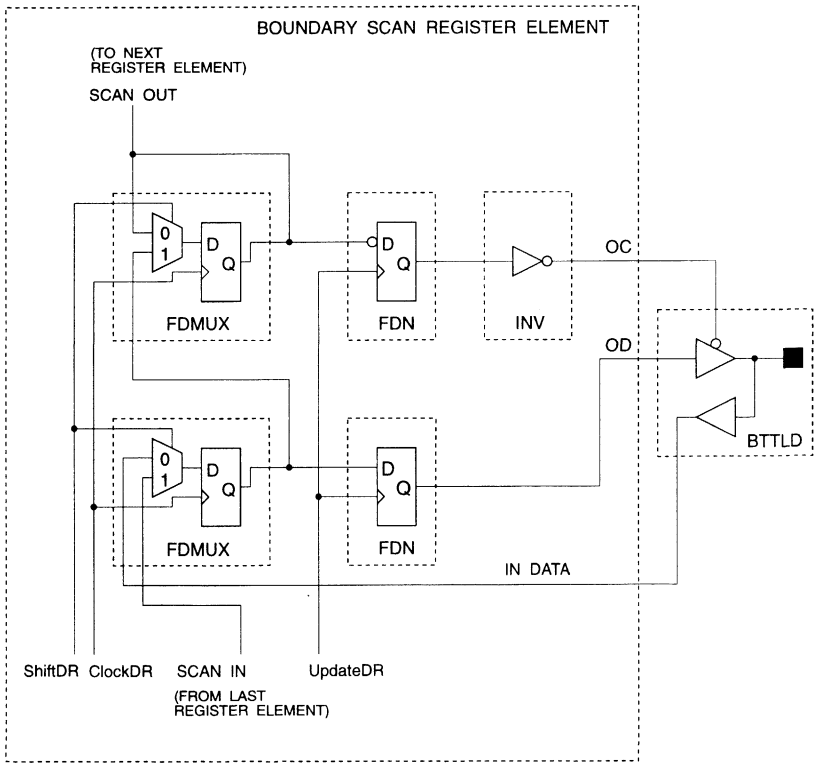
Figure 1 shows the test logic architecture with dedicated I/O pins TCK, TMS, TDI, and TDO for the 1149.1 standard. TCK and TMS control the Test Access Port controller, a state machine that regulates the flow of serial test patterns and results from TDI to TDO. The boundary-scan register communicates with all usable I/O pins, which are configured as bi-directional drivers. The bypass register enables data to be moved more quickly through the device by bypassing the boundary-scan register. The instruction register holds the test instruction that activates either the boundary-scan or bypass register, and also helps control the MUX that supplies the source for TDO.

The recommended procedure for using 1149.1 Boundary Scan is to program the part with the test logic during a system diagnostics routine, then initiate boundary scan testing for the system or board. When the test is done, reload the AT6000 device with system logic for normal operation. This test method eliminates the optional test capabilities defined in the standard. For example, using the SAMPLE/PRELOAD test instruction to capture the state of the I/O for on-line diagnostics during normal operation is not possible since the test logic is replaced with system logic.

Other optional instructions facilitating internal fault testing and the execution of built-in self testing procedures (BIST) also cannot be supported with this test methodology.

For example, INTEST isolates the device, allows patterns to be serially shifted in and applied to the internal logic, then captures the output results within the device so that they can be shifted out for fault analysis. RUNBIST enables proprietary, built-in self-test procedures to be initiated by the standard test logic. The intended test capabilities of both these instructions are already covered by the factory testing performed on each AT6000 device. Therefore, eliminating these instructions and their associated overhead by loading and unloading the standard test logic does not increase the risk of overlooking a fault in the device.

Figure 2. Boundary Scan Cell



Description of Boundary Scan Operation

As shown in Figure 2, the boundary-scan register element shifts data in through Scan In on the rising edge of ClockDR when ShiftDR is asserted. Since every I/O pin is configured as a bi-directional driver during the test sequence, two shift register bits are needed to control the output signal OD and the output control OC of the bi-directional driver. Each bit in the shift register is then latched to a secondary register that directly drives an output pin or output control of the bi-directional driver. UpdateDR loads the secondary registers from the shift register. If the bi-directional I/O BTTLD is set as an input (OC=1), the signal present at the pin is latched into the shift register on the rising edge of ClockDR when ShiftDR is unasserted.

A mandatory 1149.1 requirement for programmable components is that the length of the boundary-scan register be independent of the way the component is programmed in normal system operation. Configuring every I/O to be bi-directional eliminates the dependency of the test logic on the particular I/O pin assignment utilized during normal operation. The test logic has the flexibility to set the direction of any I/O pin according to the patterns shifted in and transferred to the secondary registers that drive the output control pins. These patterns are formulated by the test engineer based on specific knowledge about the I/O pin assignment of the device during normal operation, and how the device is interconnected with other components on the board.

These secondary registers hold a pattern at the output pins while the results are sampled at the chip inputs and stored in the shift register. ShiftDR controls sampling and shifting of the data in the shift register. The secondary registers hold the output control pins stable during sampling and shifting out of the result for interpretation because the values in the shift register change. If the secondary registers were eliminated, then the shift-register element might incorrectly drive the output control during data shifting. More than one output from different devices might accidentally drive the same wire for a substantial period of time, which could damage the devices. Having a secondary register to hold the bi-directional output control signals during shifting prevents this.

Sampling and shifting is controlled by a synchronous state machine within the device. Control signals ClockDR, UpdateDR, and ShiftDR originate from this state machine, called a test-access-port (TAP) controller. External TAP signals—which might originate from automated test equipment (ATE) or a diagnostic processor—enter the capitalize controller through dedicated input pins and initiate state-to-state transitions. The following TAP signals go into the controller:

TCK:Test Clock input provides an independent clock signal for the test logic (i.e., boundary-scan register, instruction register, bypass register, and state machine)

TMS:Test Mode Select input controls the transitions of the TAP state machine, which determines when data is sampled, loaded, and shifted.

TDI:Test Data Input is the serial data input into the shift register for the test pattern.

TDO:Test Data Output is the serial data output from the shift register.

The signals TDI and TDO, although considered part of the TAP, do not initiate or affect the state-to-state transitions in the TAP controller. They provide the serial link to and from other components on the board. For a detailed state diagram of the TAP controller, refer to Chapter 5 of the JTAG (Joint Test Action Group) standard.

Composing a Test Pattern for the AT6005

The test pattern has two purposes: first, to set the I/O as either inputs to or outputs from the device, and second, to provide a logical value ("1" or "0") to the output drivers from the device. The designer or test engineer is responsible for composing the pattern so that the proper inputs and outputs will be present on the device boundary. By performing the following tasks, any designer or test engineer somewhat familiar with the 1149.1 standard can prepare the patterns for boundary-scan testing:

1. Determine which pins are inputs and outputs based on how the AT6005 device is used in the board during normal system operation.
2. Compose a test pattern that will set the I/O to match the pin assignment according to the following assumptions:

a. The AT6005 has 104 usable I/O because four dedicated I/O are needed for the TAP signals TCK, TMS, TDI, and TDO.

b. Since a pair of bits are needed to set the direction of each of the 104 I/O, each pattern must be 208 bits in length.

c. Since the pattern is loaded serially starting at TDI, the first bit-pair loaded sets the last I/O pins.

d. For each pair of bits, the first serially loaded bit determines the I/O direction (input or output). A logical "1" sets the I/O as an input, a logical "0" sets the I/O as an output.

e. For each pair of bits, the second serially loaded bit of the pair is relevant only if the first serially loaded bit of the pair was a "0". The second bit can be either a "0" or a "1" and it will drive the output pin.

f. Any unused pin should be driven to a high-impedance state by setting the first bit of its corresponding bit-pair to a "1" value.

g. While the pattern is being loaded, the output pins are set to the high-impedance state until the secondary registers (see Figure 2) are updated with the test pattern value.

h. The TAP signals TCK, TMS, TDI, and TDO use pins 131, 129, 132, and 128, respectively.

Figure 3 shows a test pattern in the boundary-scan register and its effect on the BTTLD bi-directional I/O. Pin 2 is set as an input because the output enable signal of BTTLD is set to "1." Since the I/O is set as an input, the value of the first bit in the corresponding bit-pair in the boundary-scan register that drives the output buffer portion of BTTLD really does not matter (it is represented as an "X"). Pins 5 and 127 are also set as inputs because their output enable bits for BTTLD are also set as "1" in the boundary-scan register.

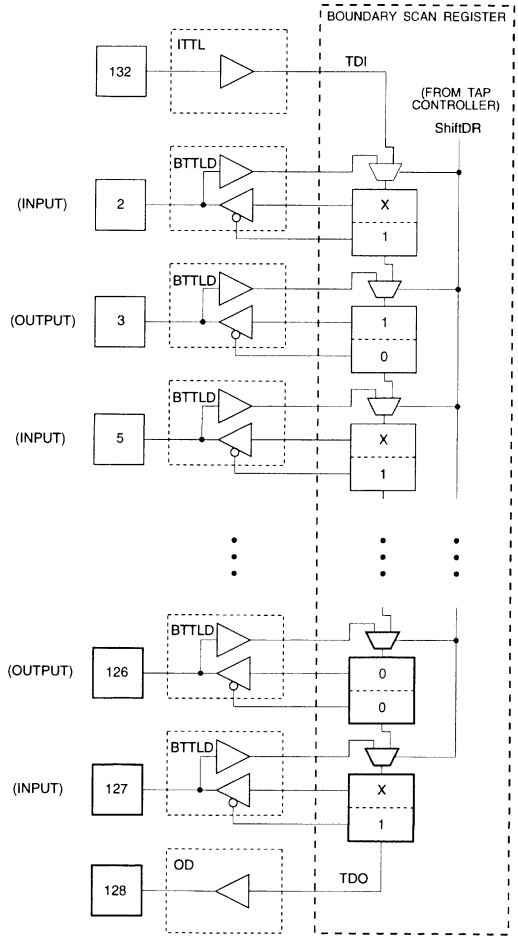
If the second bit of the bit-pair that controls the BTTLD I/O macros were a "0," as is the case with Pins 3 and 126, the BTTLDs are set as outputs. The outputs of BTTLD for Pins 3 and 126 are both driven by the first bit of the corresponding bit-pair in the boundary-scan register. A "1" from the boundary-scan register drives Pin 3, and a "0" drives Pin 126.

A test pattern is serially shifted in through Pin 132. For example, the first bit-pair is shifted through the entire boundary-scan register until it is in position to set the BTTLD macro of pin 127. While the pattern is being shifted through the register, the outputs of the secondary registers that the drive the output enable pins of the BTTLD macros are set to "1" so that every I/O in the device is in the high-impedance state (see Figure 2). This precautionary measure prevents device pins from driving a signal onto a board wire that might contend with a signal from another chip. When the pattern is completely shifted into the boundary-scan register, the secondary registers are updated with the pattern, thus setting the direction of the BTTLD macros.

Test Logic Architecture

Figure 4 shows a more detailed schematic of the test logic. The TAP controller performs boundary-scan by first capturing signals at the input pins of the bi-directional drivers and loading them into a corresponding shift register element. The TAP controller sets ShiftDR low and takes ClockDR from low to high to perform the capture. The captured input signals originate from the outputs of other chips on the board as the result of a previous test pattern. Shifting the captured pattern out of the device occurs when the TAP controller sets ShiftDR high and toggles ClockDR. While the result is being shifted out through TDO, a new test pattern is simultaneously being shifted in through TDI.

Figure 3. Test Pattern in Boundary-Scan Register



The new pattern is loaded into the secondary registers when the TAP controller toggles UpdateDR. Any bi-directional driver that is set as an output will then drive the board wires leading to the inputs of other chips.

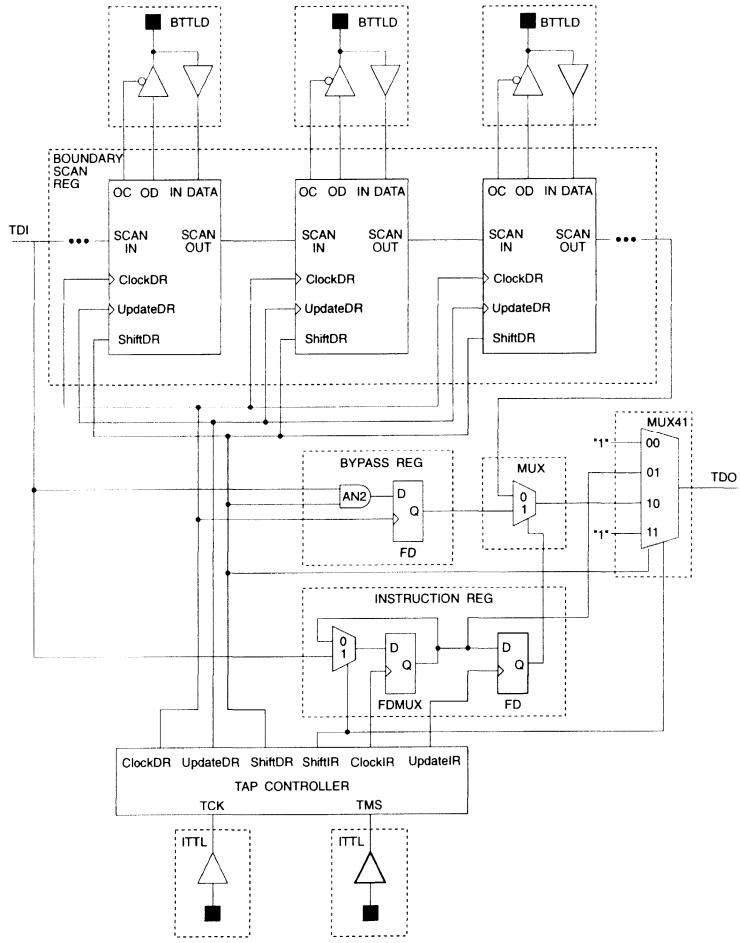
Also shown in Figure 4 are bypass and instruction registers. The bypass register quickly passes test patterns through the device if the patterns are designated for another component on the board. Captured test pattern results also flow through the bypass register to hasten their arrival to another part of the diagnostics system. Depending on the instruction loaded into the instruction register, either the bypass register or the boundary-scan register provides the source for TDO. The logical value loaded into the instruction register controls the multiplexer MUX that selects either the boundary-scan or bypass register to drive TDO.

The following mandatory instructions are necessary to conform to the standard (as described in Chapter 7 of the JTAG standard):

BYPASS: Causes a serial test pattern being shifted into TDI to be passed through a single bit register (called the bypass register) and then to TDO. The purpose of this instruction is to allow rapid serial movement of test patterns and results between components on a board. The instruction register should be load with a logical "1" value to initiate BYPASS.

SAMPLE/PRELOAD: Allows a snapshot of the data present at the input pins of a device to be stored in the shift register, and then allows the snapshot to be shifted out through TDO. While the data is being shifted out, a new test pat-

Figure 4. Schematic of 1149.1 Test Logic Architecture



tern can be simultaneously shifted in through TDI. The instruction register should be load with a logical "0" value to initiate SAMPLE/PRELOAD.

EXTEST: Allows the test pattern held in the shift register to be loaded into secondary registers that drive the output pins of the device. The application of this instruction lets the outputs of a device to drive the board traces so that the inputs of other devices can take a snapshot of the values on those traces, and thus determine if the board traces were manufactured properly. The instruction register should be loaded with a logical "0" value to initiate EXTEST.

The TAP controller loads the instruction register the same way it loads the boundary-scan register. A functionally analogous but independent set of signals, ClockIR, UpdateIR, and ShiftIR are used to control loading and shifting in the instruction register. Changing the level of TMS before the rising edge of TCK initiates state-to-state transitions in the TAP controller for every TCK cycle, causing the outputs of the controller (ClockDR, ShiftDR...) to change. A particular sequence of level changes in TMS over several TCK cycles results in the execution of either SAMPLE/PRELOAD or EXTEST if the value in the instructions register is a logical "0."

The TAP controller also chooses the register (boundary-scan, bypass, or instruction) that drives TDO. When the ShiftDR signal is asserted either the boundary-scan register or the bypass register is selected. The instruction register must then determine the register to drive TDO. If the instruction register is loaded with a "1," meaning that the BYPASS instruction should be executed, then the bypass register is selected. A logical "0" in the instruction register means that either the EXTEST or SAMPLE/PRELOAD should be executed, and that the boundary-scan register is selected.

When the ShiftIR signal is asserted the instruction register is selected to drive TDO regardless of the current instruction. If both ShiftIR and ShiftDR are unasserted, then driving a logical "1" through the multiplexer deactivates TDO.

Operating Conditions

The minimum recommended cycle time for TCK is 100 ns (10 MHz) for correct operation. With careful floor planning of critical path control signals, TAP controller the performance could be improved to 15 MHz. In the AT6005, at a TCK speed of 10 MHz, two bits are needed for each of the 104 bi-directional I/O. Shifting in a new test pattern takes 20 µs. When the boundary-scan test is complete, the device is reconfigured for normal operation in 6.4 ms by serially loading the stream of bits into the SRAM that programs the logic and interconnections. The device can be reconfigured in 808 µs if the bit stream is loaded as 8-bit bytes. A complete 1149.1 circuit is available in schematic and layout form.

References:

IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990, Joint Test Action Group (JTAG), Institute of Electrical and Electronic Engineers (IEEE), New York, May 21, 1990.

Digital Frequency/Phase Comparator (DFPC)

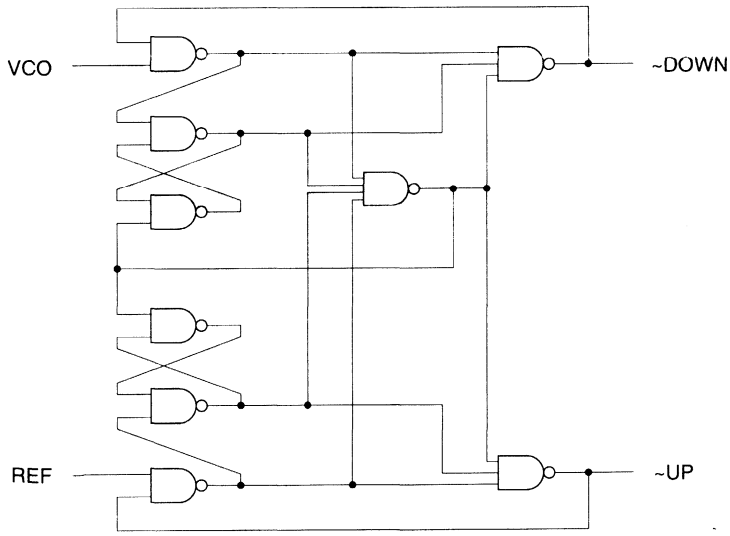
Introduction

The AT6000 Series field programmable gate array (FPGA) lets the designer implement a digital frequency/phase comparator (DFPC) that interfaces to a voltage controlled oscillator (VCO).

Description

The DFPC has two periodic input signals, a reference frequency of some desired value and a variable frequency from the VCO. Two output signals from the DFPC, ~UP and ~DOWN, control the VCO. These two signals change the VCO output frequency so as to match the reference frequency entering the DFPC. Once the reference and the variable signals have the same phase and frequency, the DFPC continues to make small adjustments to the VCO frequency to maintain the match.

Figure 1. Digital Frequency/Phase Comparator Circuit



A representation of the circuit is shown in Figure 1. The exact implementation of the circuit in the AT6000 architecture is shown in Figure 2. The performance of the DFPC was determined with the aid of another specially designed test circuit, which measures three performance characteristics of the DFPC:

1. The minimum phase difference in nanoseconds which the DFPC can detect between the reference and variable VCO signals;
2. The width of the common mode time when both ~UP and ~DOWN are asserted during the reset operation of the DFPC; and
3. The operation of the circuit when the reference and VCO output frequencies are an octave apart. Since the circuit is symmetrical the test need only be done once for either case where the reference is twice that of the VCO frequency, or vice versa.

Figure 3 shows the test circuit for generating signals of different frequencies. A ring oscillator circuit contained within the device generates a base frequency that is used as the reference signal into the DFPC. The reference signal is fed into a frequency divider and the output of the divider drives the VCO input into the DFPC.

Figure 3 also shows the circuit for generating signals with a phase difference. The same ring oscillator used in the previous test circuit is used to generate a base frequency that provides the reference signal. This reference is also used as the input into a programmable phase shifter. The phase shifter is controlled using the standard device down-loading software normally used for loading the device bit stream from a personal computer. Phase adjustments are made in increments of 100 ps.

This phase shifted signal, which has the same base frequency as the reference, is used as the VCO input for the DFPC.

When compared to a stable reference frequency, initial tests show that at typical operating conditions, the DFPC has a common mode pulse width, t_{CMPW}, of approximately 10.5 ns. Figure 4 shows the time difference between a level change in ~UP and ~DOWN, t_{DPW}, is exactly equal to the phase shift of the two input signals, t_{DIP}. The symmetry of the circuit layout in the AT6000 device enables the difference between t_{DPW} and t_{DIP} to be less than 500 ps.

The performance and utilization statistics are given in Table 1. The DFPC implementation is available in schematic and layout form.

Figure 2. DFPC Implementation

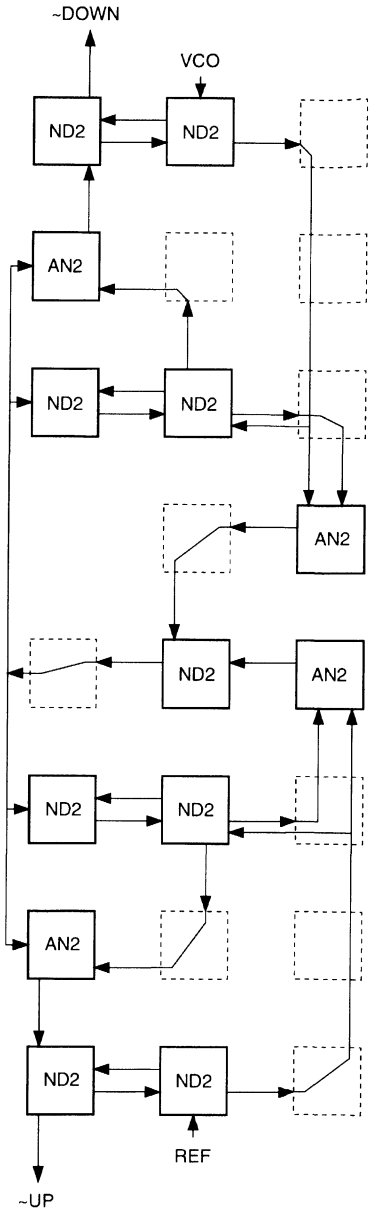


Figure 3. DFPC Test Circuits

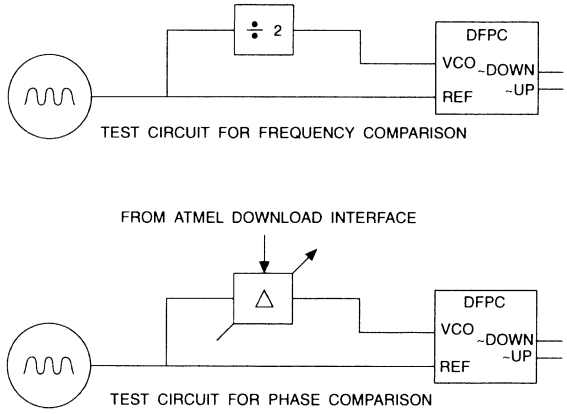


Figure 4. DFPC Timing Diagram

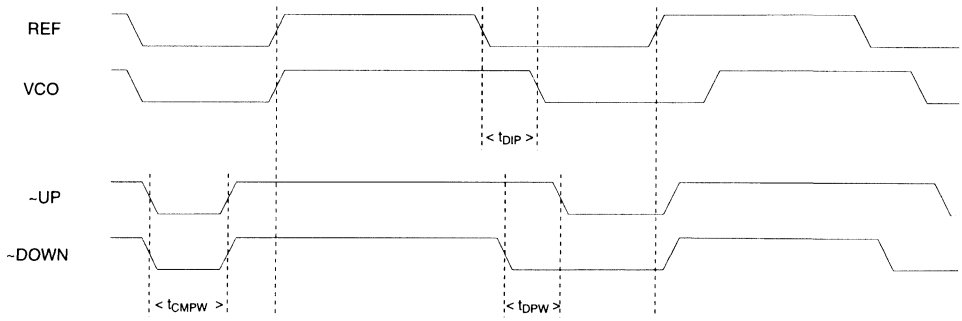


Table 1. 16 x 8 FIFO

	Cell Count[1]	Minimum Bounding Box (X x Y)	t_{CMPW}[2]	$t_{DPW} - t_{DIP}$[2]
DFPC	24	3 x 8	10.5 ns	0.5 ns

Notes:
1. Includes cells used as wires.
2. Typical Operating Conditions: 25°C, 5.0 V, AT6000-4.

Configuration Compression Algorithm

Introduction

AT6000 Series FPGAs are SRAM-based and can be reconfigured to perform different applications in a system. Formulas show how the act of reconfiguration affects system performance. A proprietary compression algorithm reduces reconfiguration time and improves system performance. This algorithm is incorporated into the bit stream generation software provided in the Integrated Development System.

Description

Two factors determine configuration time—the frequency of the configuration clock and the configuration mode used.

The configuration clock, CCLK, regulates the loading of data. The higher the clock frequency, the faster data is loaded. Modes 4 and 5 use an internally supplied clock that runs at only 1 MHz. The other modes employ a user-supplied clock. The user-supplied clock can run as fast as 10 MHz.

Of the two kinds of configuration, serial and parallel, parallel configuration is faster. Serial configuration loads one bit per clock cycle, while parallel configuration loads eight bits per clock cycle. As a result, a serial configuration mode takes eight times longer to load a bit stream. Table 1 gives equations that determine configuration times for the AT6002 and AT6005.

Partial configuration is naturally faster than full configuration. A configuration compression algorithm, supplied with Atmel's development system, filters full-configuration data to produce a partial configuration bit stream. The bit stream produced by the compression algorithm only programs memory that is different from the present configuration. On power-up, for example, each cell in the array is a zero. The compression algorithm can remove all the zeros from the bit stream to be used after power-up—in some cases reducing the size of the bit stream by as much as 50%.

This reduction provides a proportional reduction in configuration time, as shown in Table 1.

Table 1. Configuration Timing Equations

Without Compression	**AT6002**	**AT6005**
Serial	2678 x 8 x 1/Frequency	8077 x 8 x 1/Frequency
Parallel	2678 x 1/Frequency	8077 x 1/Frequency
With Compression	**AT6002**	**AT6005**
Serial	(1 - % Reduction) x 2678 x 8 x 1/Frequency	(1 - % Reduction) x 8077 x 8 x 1/Frequency
Parallel	(1 - % Reduction) x 2678 x 1/Frequency	(1 - % Reduction) x 8077 x 1/Frequency

Modeling Device Power Consumption

Introduction

The following provides a simple method for modeling the active and static power consumption of a AT6005 design.

Active Power Consumption

Active power consumption is a function of the distribution of resources in a design and the number of nets switching each second. The distribution of resources is calculated by counting the instances in the design database. The Integrated Development System (IDS) reports this information in the list files generated by programs like placement, routing and bit stream generation. The switching of some nets, like clock signals and flip-flop outputs, is determined by clock frequency and can be tabulated exactly. The switching of other nets, especially combinatorial logic, is input-dependent and not solely determined by the clock. As a result, the activity of these nodes can only be estimated. Combinatorial signals are typically half as active as the clock. Test vectors representative of actual design operation can give a more accurate calculation. Viewlogic's "activity" command calculates the number of active nodes in a design during logic simulation.

The equation for active power consumption is as follows:

POWER = Frequency x (Aa x Ka x Na + Ab x Kb x Nb + Al x Kl x Nl + Ax x Kx x Nx + Ac x Kc x Nc + Kg x Ng + Ai x Ki x Ni
+Ao x Ko x No) x V_{CC}

The N coefficients represent the design resources reported by the IDS:

Na number of A-type nets used (individual cell function is not important)
Nb number of B-type nets used (individual cell function is not important)
Nl number of local-bus type nets used
Nx number of express-bus type nets used
Nc number of clock columns used
Ng 1 if global clock is used
Ni number of I/O inputs
No number of I/O outputs with no output load used

The A coefficients represent the estimated activity of combinatorial logic.

The K coefficients represent the weighting factor of each component:

Ka = 2 µA/MHzKb = 2 µA/MHz
Kl = 4 µA/MHzKx = 3 µA/MHz
Kc = 100 µA/MHzKg = 200 µA/MHz
Ki = 4 µA/MHzKo = 60 µA/MHz

The amount of activity possible is based on the number of each cell type used. The AT6005 has the following available:

Na = 3136 Nb = 3136
Nl = 1568 Ne = 1568
Nc = 56 Ng = 1
Ki = 64 (84-pin) or 108 (132-pin)
Ko = 64 (84-pin) or 108 (132-pin)

If every node were active at 10 MHz, the device would use about 293 mA of current (1466 mW).

A more typical example would be:

Na = 2000 Ab = 2000
Al = 1200 Ae = 700
Ac = 27 Ag = 1
Ki = 54 Ko = 54

Yielding an active power consumption of:

POWER = 2000 x 0.5 x 2 + 2000 x 0.5 x 2 + 1200 x 0.5 x 4 + 300 x 0.5 x 3 + 27 x 1 x 100 + 1 x 1 x 200 + 54 x 0.5 x 4 + 54 x 0.5 x 60
= 11.5 mA/MHz

Or, 115 mA at 10 MHz (575 mW at 10 MHz).

Quiescent Power Consumption

The AT6005 is a CMOS device. Once programmed, the SRAM used to store the configuration requires no static power. The programmable interconnect points use complementary CMOS pass gates; this insures that all signals eventually reach V_{CC} or GND and dissipate no static power. There are no passive pull-ups on any internal nodes. Unused nets and buses are tied to V_{CC} and GND, and dissipate no power. Tri-states without active drivers dissipate some static power, but this is easily avoided.

Static power dissipation, measured after power-up in modes 1, 2, 3, or 6, but before programming, is 2 mA. After power-up, the device is programmed as a large array of registers with no inputs connected. Modes 4 and 5 generate a clock output signal. The power dissipation of modes 4 and 5 is 2 mA plus the power dissipation of the CCLK output driver, which is a function of the pin's loading capacitance. CCLK is typically 1 MHz.

The primary source of static power dissipation is not the core array, but the SRAM configuration circuitry. It has two blocks which consume static power—a power supply voltage monitor and an internal oscillator. The voltage monitor is used to initiate reboot when V_{CC} is first applied or when V_{CC} goes below a critical voltage. The monitor can not be disabled. The internal oscillator can be turned off by setting the B5 bit in the configu-

Table 1. AT6005 Static Power Dissipation

		Min	Typ	Max
ICC1	Modes 1, 2, 3, 6 Measured after reboot			2 mA
ICC1	Modes 4, 5 With 50p load on CCLK		5 mA	
ICC2	Modes 1, 2, 3, 4, 5, 6 B5 Bit set with CONN=CSN=VCC		900 µA	

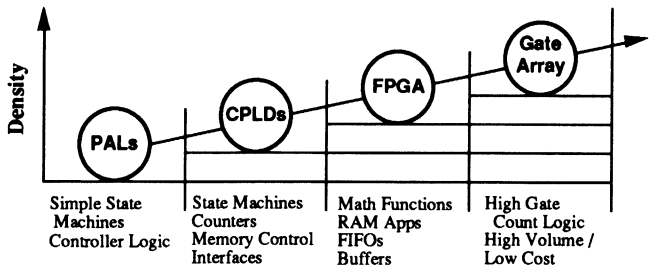
Converting FPGAs and PLDs to Atmel Gate Arrays

Introduction

Atmel is one of the only companies that designs and manufactures field programmable gate arrays (FPGAs), programmable logic devices (PLDs) and high performance gate arrays. Atmel offers a seamless, direct conversion path for designs implemented on most PLDs and FPGAs to its gate array families. The potential benefits to the system designer of such a capability are fourfold:

- Component cost savings. Atmel's conversion process will convert a single FPGA or PLD into a lower cost gate array that is a pin-for-pin compatible replacement.
- Board space savings. Atmel converts to a true gate array, not a hardwired FPGA/PLD. Multiple FPGAs or PLDs can be converted and consolidated into a single gate array, reducing system component count and providing even more cost savings.
- Enhanced performance. Conversion to a gate array grants the designer access to all of the macrocells and functions contained in the cell library. Included are higher order logic functions, inclusion of SRAM, PCI and other buffers and testability improvement circuitry that cannot be realized on an FPGA or PLD. Gate array routing schemes allow a greater degree of flexibility to optimize timing performance or logic area.
- Reduction in design cycle time. An ASIC design can be prototyped using programmable logic and migrated to a gate array for production without the time and cost of a redesign.

In all cases, Atmel uses the existing FPGA or PLD design database so that little additional engineering effort is required from the customer. This application note discusses some factors to consider when deciding to convert, describes the conversion process, and details the required information for selected FPGA and PLD products.



FPGA/PLD to Gate Array Conversion

Application Note

7

ATL80 Array Organization - 0.8 μ CMOS

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O Pins	Gate[1] Speed
ATL80/2	2,000	1,000	36	28	256 ps
ATL80/5	5,000	3,000	68	60	256 ps
ATL80/10	10,000	6,000	80	72	256 ps
ATL80/15	17,000	10,200	100	92	256 ps
ATL80/25	26,000	15,600	120	112	256 ps
ATL80/40	39,000	23,400	144	136	256 ps
ATL80/50	50,000	30,000	160	152	256 ps
ATL80/75	75,000	45,000	184	176	256 ps
ATL80/95	94,000	60,000	208	192	256 ps
ATL80/150	150,000	75,000	256	236	256 ps
ATL80/220	220,000	110,000	304	280	256 ps
ATL80/280	280,000	140,000	340	310	256 ps
ATL80/350	350,000	175,000	380	350	256 ps
ATL80/450	450,000	225,000	424	384	256 ps
ATL80/600	600,000	300,000	480	440	256 ps

Notes: 1. Nominal two input NAND gate with a fan out of two at 5.0 volts.

ATLV Array Organization

Device Number	Raw Gates	Routable Gates	Max Pin Count	Max I/O[1] Pins	Gate[2] Speed
ATLV2	2,000	1,400	44	36	1.3 ns
ATLV3	3,000	1,600	68	60	1.3 ns
ATLV5	5,000	2,800	84	76	1.3 ns
ATLV7	7,000	4,400	100	92	1.3 ns
ATLV10	10,000	6,600	120	112	1.3 ns
ATLV15	15,000	8,000	144	136	1.3 ns
ATLV20	22,000	12,000	160	152	1.3 ns
ATLV35	35,000	18,000	208	192	1.3 ns

Notes: 1. Absolute maximum I/O pins is maximum pin count minus 8. Additional power and ground pins are assumed to be required to support simultaneous switching outputs as pin count increases.

2. Nominal two input NAND gate with a fan out of two at 1.5 volts.

Programmable Logic vs Gate Array

Programmable logic devices have enjoyed tremendous popularity and growth over the last several years, primarily because the user saves both time and money. Designers may work with multiple design tools that run on inexpensive platforms. Designs can be implemented in hours and modified easily, allowing for system performance evaluation in the same week. This instant feedback allows designers to validate system operation and rectify any errors without additional expense. Programmable logic devices provide an ideal solution for low to moderate production volumes and for fast prototyping of more complex logic designs. As volumes increase, however, programmable devices may become prohibitively expensive.

Gate arrays provide an efficient implementation of the design. They offer superior performance, higher density, and lower cost-per-gate in production volumes when compared to programmable logic devices. Design tools that support gate arrays are typically more comprehensive and expensive than FPGA/PLD design tools. However, many ASIC design platforms now support FPGA design. The ability to simulate both the programmable device and the gate array in the same design environment allows the designer to compare and verify the conversion. However, while gate array prototypes can be delivered in days or weeks, that is still a much longer period than the verification cycle of a programmable logic device. Gate array designs typically require a nonrecurring expense for design implementation, and design revisions may require additional time and expense.

Why Convert?

There are four instances when converting from a programmable logic device to a gate array offers the user a direct benefit.

Save Money at High Volumes. If the cost of one year's supply of programmable devices approximates the cost of the nonrecurring expense plus the initial year's supply of a gate array device, serious consideration should be given to conversion. After the nonrecurring expense is amortized, the cost savings become even more dramatic.

Time To Market Versus Cost Reduction. Using a programmable device for logic verification and prototyping and then converting to a gate array gives the designer the best of both worlds - a fast, accurate design cycle and a low cost component in production.

Higher Performance. Gate arrays have lower standby and operating current, plus offer greater speed than an FPGA/PLD. The designer also has a greater selection of buffer types, drive currents, and a wide selection of higher order logic and memory (SRAM) functions.

Integration. Converting several FPGAs or PLDs and consolidating the logic into a single gate array uses less printed circuit board space, reduces the component count, consumes less power, and improves the reliability of the system.

Atmel Conversion Process

Summary of the Conversion Process

Atmel's FPGA/PLD to gate array conversion process is intended to minimize the amount of additional engineering effort required from the system designer. Figure 1 outlines the conversion process flow. The database inputs to the conversion process flow will vary depending upon the manufacturer of the FPGA(s) or PLD(s) and are covered in following sections.

The conversion of the programmable device's netlist into an Atmel cell library netlist is accomplished via Synopsys™. Synopsys tools can read a variety of formats, including our preferred formats of EDIF™ and Verilog™. Figure 2 outlines the process by which Synopsys converts the FPGA netlist into Verilog-XL™ format. The database is input to a proprietary Atmel mapping file for translation into Atmel cells. When the design is mapped in its entirety, a Verilog netlist in Atmel cells is produced. At this point the design process (Preliminary Design Review through Final Design Review, outlined later in this application note) is the same as any other gate array design.

Database Requirements

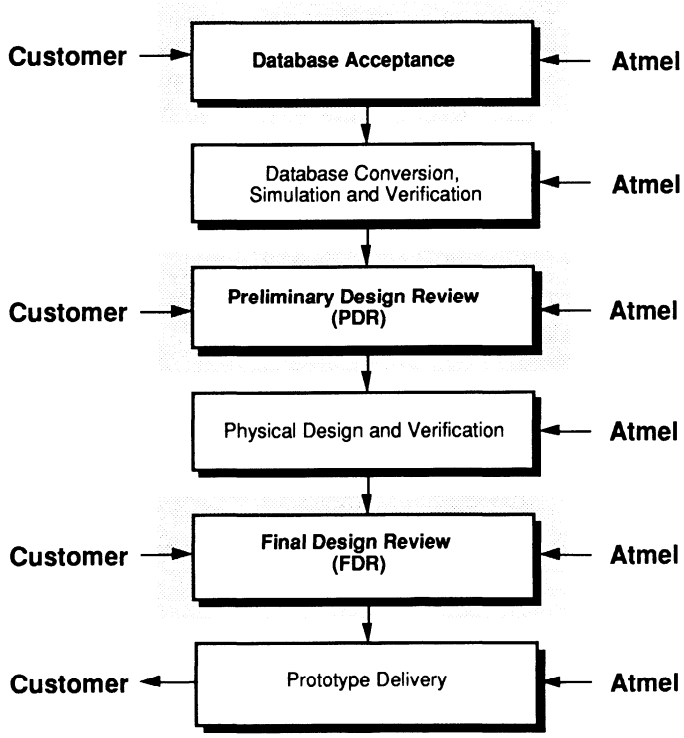
If your logic design philosophy includes the conversion of a progammable device to a gate array, effort should be dedicated to the generation of test vectors during the design of the programmable device. While test vectors are not required to verify a programmable logic device, a gate array cannot be verified without them. The final approval of the vectors to be used falls upon the original designer; one is best served to produce and verify the test vectors prior to database submission than to attempt to reconstruct them after the fact.

The designer will supply a database that is unique to the specific choice of FPGA/PLD as a part of the conversion process, as well as information that is independent of the FPGA/PLD choice. The exact files required from the CAD system used to develop a given manufacturer's device are listed in the following sections, however, a general list of database requirements include:

Netlist. The preferred netlist format is EDIF, Verilog is also acceptable. Other formats, such as those generated by Viewlogic™ or Mentor™ platforms, will ultimately be converted to EDIF for use with Synopsys.

Test Vectors. All vectors must be in the same five groups (Input, Output, Tri-state™, Bi-directional, and Enable) and have a stated purpose. Outputs are sampled once per clock cycle at the 75% cycle point. Test vectors must include a 1 MHz set for wafer probe and an "at speed" set for final test. "At speed" may be a 1 MHz set with certain critical paths identified for testing "at speed". Test vectors must pass Atmel's Test Vector Checker (tvc), a tool provided with our libraries to verify the format of the vector set.

Figure 1. FPGA/PLD to Gate Array Conversion



Specifications.

- Operating conditions of voltage and temperature
- System loading requirements by pin
- Operating clock speed and number of clocks
- I/O definition including pin out and enable for Tri-state and bi-directional buffers
- Identification of critical paths
- Definition of asynchronous behavior

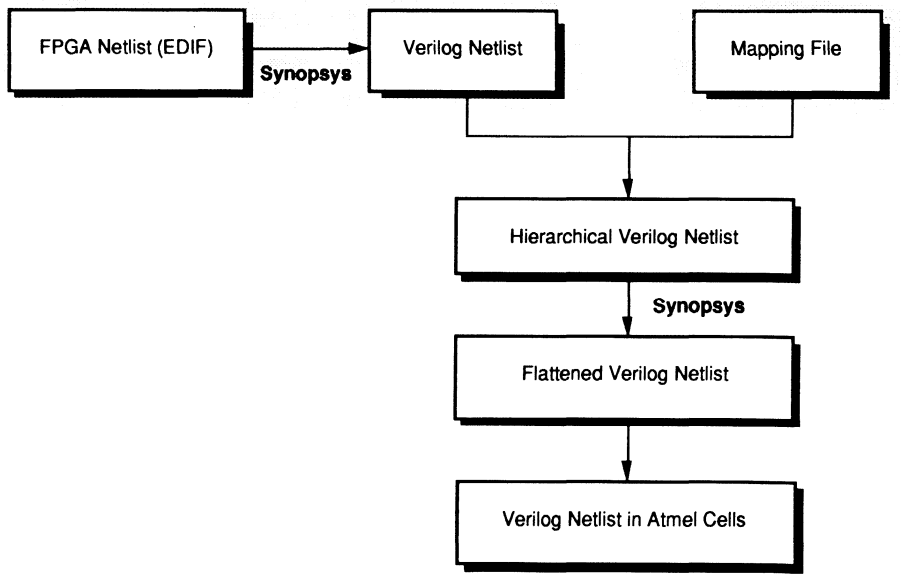
Documentation.

- Full hierarchical schematics
- Clock tree and reset diagram
- Timing diagrams showing relationship of clocks to data applied and valid outputs

Database requirements will depend upon the manufacturer and design platform for the FPGA or PLD device. These requirements will also be dependent on whether one or multiple devices are combined into a single gate array, and the performance expectations. The actual approach that Atmel takes to the conversion process will be driven by the these items.

Atmel's gate array families allow the designer flexibility in I/O placement. Eight power and ground pins, located in the corners of the die, are the only dedicated pins. All other pads on the die are fully programmable for input, output, bi-directional, Tri-state, power, or ground.

Figure 2. FPGA Conversion



Converting FPGAs

FPGAs are similar to a gate array in both design and physical implementation, making the conversion process relatively simple. Most FPGAs use only a few logic blocks which are typically found in most gate array cell libraries. This allows the FPGA netlist to be mapped directly into gate array primitive cells, simulated, validated, and routed in the standard gate array design flow. Any optimization that is required to meet performance objectives may also be implemented.

Required Database

Design Database Format

- EDIF 2.0.0
- Viewlogic Files
  - .CMD (Simulator Command File)
  - .EDN (EDIF Netlist)
  - .SCH (Schematics)
  - .SYM (Symbols)
  - .WIR (Wire List)
  - Viewdraw™ .INI
- Cadence™ Verilog-XL Files
  - EDIF Netlist
- Mentor Files
  - .MIF (Mentor Interface File - Netlist)
  - .LOG (Simulation Log File)
  - .LIST (Simulation Listing File)
  - .FORCE (Simulation Force File)
- Synopsys - .db files
- Altera™ - .RPT files

Simulation/Test Vector Format

- ASCII format - 1 vector per line, time stamp in left column
- Print-on-change format
- Bi-directional signals must be defined as input or output
- 1MHz wafer probe and at-speed final test
- Verified by Atmel's Test Vector Checker (tvc)

Tables 1, 2 and 3 list the recommended Atmel gate arrays for conversion from various Actel™, Altera™ and Xilinx™ programmable devices.

Table 1. Actel FPGA/Atmel Gate Array Cross Reference

Actel FPGA		Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
				ATL80 Series	ATLV Series
Act 1™	1010	1,200	57	ATL80/2 ATL80/5	ATLV2 ATLV3
	1020	2,000	69	ATL80/5 ATL80/10	ATLV3 ATLV5
Act 2™	1225	2,500	83	ATL80/5 ATL80/10	ATLV5 ATLV7
	1240	4,000	104	ATL80/15 ATL80/25	ATLV7 ATLV10
Act 3™	1280	8,000	140	ATL80/25 ATL80/40	ATLV15 ATLV20
	1415	1,500	80	ATL80/10 ATL8015	ATLV5
	1425	2,500	100	ATL80/15 ATL80/25	ATLV7 ATLV10
	1440	4,000	140	ATL80/40 ATL80/50	ATLV15 ATLV20
	1460	6,000	168	ATL80/50 ATL80/75	ATLV20 ATLV35
	14100	10,000	228	ATL80/95 ATL80/150	

Note: 1. Target array dependent on number of pins used, and pinout.

Table 2. Xilinx EPLD/FPGA to Atmel Gate Array Cross Reference

Xilinx EPLD	Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
			ATL80 Series	ATLV Series
XC7236A	1,600	36	ATL80/2 ATL80/5	ATLV2 ATLV3
XC7272A	3,200	72	ATL80/5 ATL80/10	ATLV3 ATLV5
XC7318	500	38	ATL80/2 ATL80/5	ATLV2 ATLV3
XC7336	1,000	38	ATL80/2 ATL80/5	ATLV2 ATLV3
XC7354	2,200	66	ATL80/5 ATL80/10	ATLV3 ATLV5
XC7372	3,000	84	ATL80/10 ATL80/15	ATLV5 ATLV7
XC73108	4,600	120	ATL80/15 ATL80/25 ATL80/40	ATLV10 ATLV15
XC73144	6,200	156	ATL80/25 ATL80/40 ATL80/50 ATL80/75	ATLV15 ATLV20 ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

Table 2 (continued). Xilinx EPLD/FPGA to Atmel Gate Array Cross Reference

Xilinx FPGA	Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
			ATL80 Series	ATLV Series
XC2064/L	0.6K - 1.0K	58	ATL80/5	ATLV3
XC2018/L	1.0K - 1.5K	74	ATL80/10	ATLV5
XC3020, XC3120	1.3K - 1.8K	64	ATL80/5 ATL80/10	ATLV3 ATLV5
XC3030, XC3130	2.0K - 2.7K	80	ATL80/10 ATL80/15	ATLV5 ATLV7
XC3042, XC3142	3.0 K - 3.7K	96	ATL80/15 ATL80/25	ATLV7 ATLV10
XC3064, XC3164	4.0K - 5.5K	120	ATL80/25 ATL80/40	ATLV10 ATLV15
XC3090, XC3190	5.0K - 7.5K	144	ATL80/40 ATL80/50	ATLV15 ATLV20
XC3195	6.0K - 9.0K	176	ATL80/50 ATL80/75	ATLV20 ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

7

Table 2 (continued). Xilinx EPLD/FPGA to Atmel Gate Array Cross Reference

Xilinx FPGA	Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
			ATL80 Series	ATLV Series
XC4002A	1.6K - 2.0K	64	ATL80/5 ATL80/10	ATLV3 ATLV5
XC4003, XC4003A	2.5K - 3.0K	80	ATL80/10 ATL80/15	ATLV5 ATLV7
XC4003H	2.5K - 3.0K	160	ATL80/50 ATL80/75	ATLV20 ATLV35
XC4004A	3.2K - 4.0K	96	ATL80/15 ATL80/25	ATLV7 ATLV10
XC4005, XC4005A	4.0K - 5.0K	112	ATL80/15 ATL80/25	ATLV7 ATLV10
XC4005H	4.0K - 5.0K	192	ATL80/75 ATL80/95	ATLV35
XC4006	5.0K - 6.0K	128	ATL80/25 ATL80/40	ATLV10 ATLV15
XC4008	6.5K - 8.0K	144	ATL80/40 ATL80/50	ATLV15 ATLV20
XC4010, XC4010D	8.0K - 10.0K	160	ATL80/50 ATL80/75	ATLV20 ATLV35
XC4013	10.0K - 13.0K	192	ATL80/75 ATL80/95	ATLV35
XC4020	16.0K - 20.0K	224	ATL80/95 ATL80/150	ATLV35
XC4025	20.0K - 25.0K	256	ATL80/150 ATL80/220	ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

Table 3. Altera FPGA/PLD/Atmel Gate Array Cross Reference

Altera PLD		Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
				ATL80 Series	ATLV Series
Max 5000™	5032	600	16	ATL80/2	ATLV2
	5064	1,200	28	ATL80/2	ATLV2
	5128, 5128A	2,400	52	ATL80/5 ATL80/10	
	5130	2,400	48, 64	ATL80/5 ATL80/10	ATLV3 ATLV5
	5192, 5192A	3,750	64	ATL80/5 ATL80/10	ATLV5 ATLV7
Max 7000™	7096	1,500	48, 60, 72	ATL80/5 ATL80/10	ATLV3 ATLV5
	7128E	2,500	64, 80, 96	ATL80/5 ATL80/10 ATL80/15 ATL80/25	ATLV5 ATLV7 ATLV10
	7160E	3,200	60, 80, 100	ATL80/25 ATL80/40	ATLV10
	7192E	3,800	120	ATL80/25 ATL80/40	ATLV10
	7256E	5,000	128, 160	ATL80/25 ATL80/40 ATL80/50 ATL80/75	ATLV10 ATLV15 ATLV20 ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

Table 3 (continued). Altera FPGA/PLD/Atmel Gate Array Cross Reference

Altera PLD		Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
				ATL80 Series	ATLV Series
Max 9000™	9320	6,000	56, 112, 128, 144	ATL80/10 ATL80/15 ATL80/25 ATL80/40 ATL80/50 ATL80/75	ATLV10 ATLV15 ATLV20 ATLV35
	9400	8,000	55, 135, 128, 144	ATL80/10 ATL80/15 ATL80/25 ATL80/40 ATL80/50 ATL80/75	ATLV10 ATLV15 ATLV20 ATLV35
	9480	10,000	113, 142, 171, 196	ATL80/25 ATL80/40 ATL80/50 ATL80/75 ATL80/95 ATL80/150	ATLV20 ATLV35
	9560	12,000	149, 187, 212	ATL80/25 ATL80/40 ATL80/50 ATL80/75 ATL80/95 ATL80/150	ATLV20 ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

Table 3 (continued). Altera FPGA/PLD/Atmel Gate Array Cross Reference

Altera FPGA		Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
				ATL80 Series	ATLV Series
Flex 8000™	8282, 8282A, 8282AV, 8282AV	2,500	64, 74	ATL80/5 ATL80/10	ATLV5
	8452, 8452A	4,000	64, 116	ATL80/10 ATL80/15 ATL80/25 ATL80/40	ATLV7 ATLV10 ATLV15
	8636A	7,000	64, 106, 132	ATL80/10 ATL80/15 ATL80/25 ATL80/40	ATLV7 ATLV10 ATLV15
	8820, 8820A	9,000	116, 148	ATL80/25 ATL80/40 ATL80/50	ATLV20
	81188, 81188A	12,000	144, 180	ATL80/25 ATL80/40 ATL80/50 ATL80/75 ATL80/95	ATLV20
	81500, 81500A	16,000	177, 204	ATL80/25 ATL80/40 ATL80/50 ATL80/75 ATL80/95	ATLV20
	8050M	50,000	360	ATL80/75 ATL80/95 ATL80/150 ATL80/220 ATL80/280 ATL80/350 ATL80/450	ATLV35

Note: 1. Target array dependent on number of pins used, and pinout.

Atmel FPGAs/PLDs - Required Database

The specific file requirements for converting from an Atmel FPGA or PLD are quite straightforward. Table 4 is a cross reference for Atmel PLD/FPGA and gate arrays.

- JEDEC Files (PLD)
  - ABEL
  - CUPL
  - LOGIC

- Viewlogic File (PLD, FPGA)
  - .GDF (Graphic File)
  - .TDF (Text File)
  - .HIF, .FIT (Fitter File)
  - .POF (Programmer Object File)
  - .SNF (Simulation Netlist File)
  - .VEC (Simulation Vector File)

- IDS File (FPGA)
  - .CDB

Table 4. Atmel PLD and FPGA/Atmel Gate Array Cross Reference

	Atmel PLD/FPGA	Equivalent Usable Gates	I/O Pins	Target Atmel[1] Gate Array	
				ATL80 Series	ATLV Series
PLD	AT22V10	300	10	ATL80/2	ATLV2
	AT18V8	250	8	ATL80/2	ATLV2
	ATV750	750	10	ATL80/2	ATLV2
	ATV2500	2,500	24	ATL80/2 ATL80/5	ATLV5
	AT3000	3,000	56	ATL80/5	ATLV5
	ATV5000	5,000	52	ATL80/10	ATLV7
FPGA	AT6002	2,000	96	ATL80/5 ATL80/10 ATL80/15	ATLV5 ATLV7
	AT6003	3,000	108	ATL80/5 ATL80/10 ATL80/25	ATLV7 ATLV10
	AT6005	5,000	108	ATL80/10 ATL80/15 ATL80/25	ATLV7 ATLV10
	ATL6010	10,000	160	ATL80/15 ATL80/25 ATL80/40 ATL80/50	ATLV15 ATLV20

Note: 1. Target array dependent on number of pins used, and pinout.

Converting PLDs

Two different methods can be used when converting from PLDs to gate arrays, each of which is intended to provide an optimal solution to a specific concern. These methods are deterministic and timing matching. Each method involves trading gate array utilization for matching the timing of the original design, as can be seen in Table 5.

Deterministic Conversion

PLDs have a uniform, deterministic architecture. Every signal within a PLD traverses a constant length path and avoids race conditions. If the converted design is to be a drop-in replacement, then it must meet the same specifications of the original PLD design, including minimum and maximum signal arrival times, set-up and hold times.

These system requirements become particularly critical when the PLD is driving a chip with a positive hold time. As Figure 2 demonstrates, a reduction in the clock-to-output time will cause a hold time failure within the system.

Using a deterministic approach, the gate array logic is implemented using blocks similar in structure to those used in the PLD, i.e., product terms and sum terms. This methodology eliminates the possibility of introducing the timing problem described above and is moderately efficient in terms of gate utilization and timing matching.

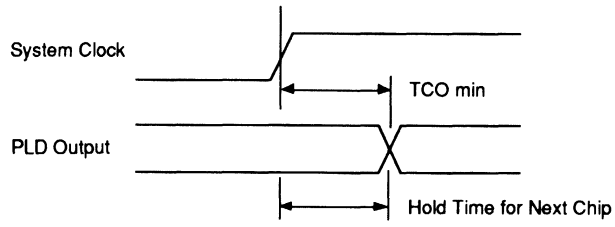
Timing Matching Conversion

If a PLD design is completely synchronous, timing optimization techniques can be used to find the minimum propagation delay for each path. This information can then be used to adjust delay to paths until the maximum signal arrival time of the path, as implemented in the gate array, matches that of the PLD. As the name of this approach implies, this method offers the best timing match between gate array and PLD, at the expense of additional buffers to adjust specific path timing.

Table 5. PLD to Gate Array Conversion Methodologies

Conversion Methodology	Gate Utilization	Timing Match	Comments
Deterministic	Moderate	Moderate	Eliminates internal timing concerns.
Timing Matching	Lowest	High	Eliminates both internal and system timing concerns.

Figure 2. System Timing Concerns (Positive Hold Times)



As discussed earlier, the type of conversion approach that is selected will determine how many of a particular PLD can fit onto an array. Atmel's ATL80/5 array, featuring up to 3,000 routable gates and 68 die pads, is used as the target array for the following example.

For a deterministic conversion, the percentage utilization is given by the formula:

$$\% \text{ utilization} = (0.15x + 0.008y + 1.5z)$$

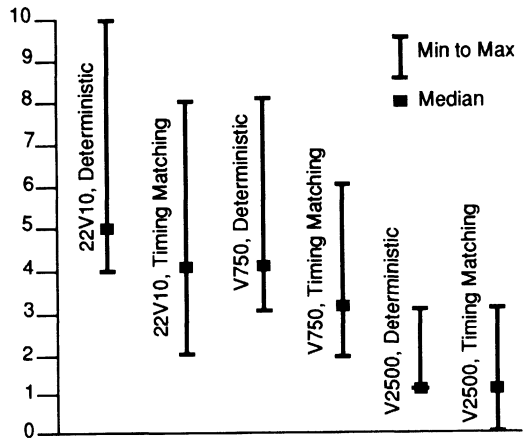
where x is the number of product terms, y the number of pins, and z the number of registers.

For a timing matching conversion, the percentage utilization is given by:

$$\% \text{ utilization} = (0.35x + 0.08y + 1.5z)$$

Figure 3 shows a range for the number of PLD designs which will fit onto an ATL80/5, for selected members of Atmel's ATLV family and for both deterministic and timing matching approaches. There will often be a wide range of PLD utilization within a given system configuration. The value shown for the "median" will provide a good benchmark when considering converting multiple PLDs into a gate array. The maximum number shown is typically a function of the number of I/O pins required.

Figure 3. Number of Specific PLD Designs which will fit in an ATL80/5 (Min, Median, Max)



Gate Array Implementation

After database acceptance, the design database is converted into an equivalent netlist of primitive cells from Atmel's gate array library. The vectors from the original FPGA or PLD design are also converted and are used as functional simulation vectors to validate the gate array netlist. As these vectors are used to perform any timing simulation and form the core of the gate array tester program, it is vitally important that an accurate and complete vector set is provided.

After the FPGA or PLD databases have been converted and validated, any additional circuitry, such as memory blocks, testability improvement elements, or higher order logic functions, can be incorporated into the netlist. Any optimization that is necessary to match timing or to improve performance can be performed at this point as well. At this point, boundary and internal scan can be added and ATPG vectors generated. A Preliminary Design Review is then held with the customer to review and to approve the results of the design conversion.

Preliminary Design Review (PDR)

The following items are reviewed at the PDR:

- Confirm Netlist Checker (v3) and Test Vector Checker (tvc) files correct
- I/O buffer listing and bonding diagram
- Preliminary testability compiler report
- Route clock tree and analysis of worst case and best case delay
- Verilog simulation at-speed
  - -nominal, worst case, best case (with no timing violations)
- Review critical path information (t_{SU}, t_{HOLD}, t_{PD})
  - -Verilog or Veritime estimates
- I/O electrical specifications
- Electromigration calculation

Final Design Review (FDR)

Beyond this point, the design process follows that of a traditionally designed gate array. The cells are placed and routed, a post-route simulation is performed, and checks are performed to verify conformance with electrical and design rules, and to confirm the Logic Versus Schematic (LVS) is correct. An FDR is held with the customer to review and approve the post route data, and to authorize mask making and prototype fabrication.

The FDR is the last joint review between Atmel and the customer before committing to prototypes. Prior to this meeting, both Atmel and the customer will have reviewed the post-route Verilog-XL simulation incorporating the back annotation data. The customer may receive back annotation data for complete post-route simulation on their CAE systems. Atmel guarantees silicon performance equal to or better than that predicted by the post-route Verilog-XL simulations. The items to be reviewed at FDR are as follows:

- Updates of cell mapping and timing (if any)
- Post-route netlist check (v3)
  - -post-route netlist changes
- Post-route timing simulation to specification
  - -review clock timing
  - -at speed
  - -clock skew (if required)
  - -listing of timing warnings with explanation
- Static path analysis (as specified)
- Electromigration calculation
- Bonding diagrams and pin list
  - -bond pad plot
- LVS/DRC/ERC

Prototype Delivery

Atmel will deliver 10 prototypes in ceramic or TQFP packages to the customer. The units are to verify the functionality and electrical performance of the gate array.

Synthesis from a Hardware Description Language (HDL)

There has been an increase in the use of HDLs to design FPGAs and PLDs as more of the design platforms offer this capability. Two of the most popular languages are VHDL and Verilog-HDL. Using a logic synthesis technique, the behavioral level description of an FPGA or PLD can be mapped into a functionally equivalent gate array netlist. Both hardware description languages are supported by the Synopsys Design Compiler. This FPGA/PLD to gate array conversion methodology requires the least amount of data conversion and allows the flexibility to incorporate such features as memory, testability, or higher order logic functions into the gate array. This technique is also effective when the need to consolidate several FPGA or PLD designs into one gate array exists. Synthesis from an HDL offers the most efficient utilization of the gate array, at the expense of timing matching. Should the user require them, VHDL descriptions of the converted FPGAs or PLDs, as well as the gate array implementation, can be provided by exporting the netlists through Synopsys.

Testability Improvement and Automatic Test Pattern Generation

The incorporation of testability improvement circuitry into an ASIC design becomes more important as the density of the design increases. The same can be said for conversion and consolidation of large numbers of dense FPGAs or PLDs into a gate array. The insertion of scan paths within an ASIC and testing via ATPG can provide an easy means of screening manufacturing-related defects during testing, with a relatively small silicon usage penalty. Using ATPG is only a supplement to functional test vectors, not a replacement.

The process consists of replacing existing flip-flops with scan flip-flops and connecting them up to form scan chains. An input pin and output pin must be identified for each scan chain. In general, scan chains should not exceed 64 flip-flops in length. Thus, for a design with 600 flip-flops, 10 input pins and their corresponding output pins must be identified. Existing pins may be multiplexed for this use if the design is pin limited. Additional pins are required for the Test Enable (TE) signal and a Test Mode (TM) signal. The TE pin is used to control the flip-flops, placing them in either normal mode or scan mode.

The TM pin is required to bypass violations of testability guidelines, an example of which would be gated clocks. During testing, all flip-flops in the scan chains must toggle on the same clock. If gated clocks exist in the design, logic must be designed so that it bypasses this gating when Test Mode is active. Since Test Mode is active only during ATPG test, the basic function of the design is unaffected.

Table 6 outlines other testability rules and suggested workarounds utilizing the Test Mode signal. When all test guidelines are followed, testability insertion and vector generation are easily accomplished. Past experience has shown extremely high fault coverage (up to 99%) with small ATPG vector sets. If these rules are not followed closely, incorporating scan and ATPG can require several weeks. It is highly recommended that the FPGA be designed using the rules in Table 6 if the customer intends to someday convert to a gate array and use scan/ATPG.

Table 6. Synopsys Test Compiler Guidelines

Testability Rule	Effects of Infraction	Workaround
Synchronous Design - No cross coupled gates - No unregistered feedback	Associated logic untestable	Break feedback path with test mode
Single Edge Clocking	Clocked device not allowed in scan chain - reduced fault	In test mode, create single edge clocking with inverters and MUXs
No Clock Gating	Clocked device not allowed in scan chain - reduced fault coverage	Use data disable flip-flops instead of clock enables, disable gating in test mode
No Latches	Not allowed in scan chain, reduced fault coverage	Use alternate test methods, force latches to transparent mode with test mode
Single External Reset - No asynchronous resets or presets generated on chip - No combinational logic in reset path	Not allowed in scan chain, reduced fault coverage	Reset OR'd with test mode
No Internal Tri-state Buses	Reduced fault coverage, possible Tri-state contention during scan test	Use MUXs or AOI gates, insert gating of controls to prevent contention
No Direct Q to D Connections	Dynamic Hazard	

Translation Of Existing ASIC Designs

ASIC Design Translation

Application Note

Introduction

It has only been in the last few years that designers and users of application specific integrated circuits (ASIC) have been able to obtain additional sources for these types of integrated circuits. The introduction of design synthesis software by CAD / CAE companies has made the task of converting from one ASIC vendor's library into another's, a feasible task even for the most dense designs.

The user of an application specific integrated circuit who desires the flexibility and security offered by having multiple sources for what are often key system components, or the user who requires an improvement in performance offered by advanced process technologies, now have an easy path to satisfy their needs. That path is Atmel's Design Translation ASIC design flow, shown in Figure 1. The Design Translation flow highlights the major steps that are taken in converting a netlist into Atmel's gate array cells, verifying the translation, performing the layout and realizing the desired circuit performance, and fabricating and testing the resulting silicon product.

This application note describes the types of data required from the ASIC user and the process steps followed by Atmel to successfully translate an existing ASIC design, and presents the results of two translation efforts. The first was an effort where the Atmel device performance was required to match that of the original ASIC. The second was a translation where the improved performance of Atmel's device was required. The process has been proven through successful translation of designs from such vendors as LSI Logic, NEC, Fujitsu, and Oki, into our 1.0 µ ATL series gate array family.

The Process

Simply stated, the Design Translation process maps cells from the original design into cells contained in Atmel's cell library. These cells may be equivalent primitives or may be soft macros which include several primitives. The choice of Atmel cell will depend upon the required performance objective, and, in some instances, hard macros may be created to replace soft macros to achieve performance goals for the design.

Once the mapping is complete, the process follows Atmel's normal ASIC design flow, including cell placement and routing, resimulation using Atmel's "golden" simulator, comparison of predicted versus desired performance and, after approval of the design by the user, PG tape out and prototype fabrication.

Database Required

ASIC design can be accomplished on a variety of platforms, and with a variety of software tools - some open, some proprietary. Designs are completed using generic and/or vendor-specific library cells as well. This level of flexibility available to the ASIC designer does not hinder the translation effort. Most design tools are capable of providing a netlist in EDIF (EDIF 2.0.0) format. Other netlist formats which are acceptable to Atmel are listed below:

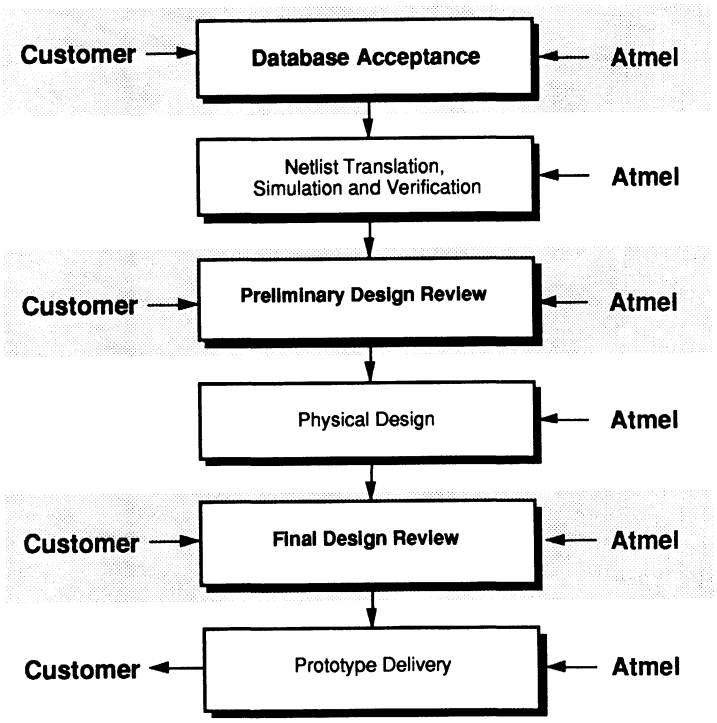
Cadence™ - Verilog-XL™, EDIF 2.0.0
LSI Logic - NDL™
Mentor™ - MIF™
Synopsys™ - db, EDIF
Viewlogic™ - EDIF 2.0.0

In addition to the netlist for the original design, several other pieces of information are needed to successfully translate the design. Also required are:

A description of the original design library
Functional test vectors, print-on-change format
Device specifications
Identification of critical and/or asynchronous paths
"As-routed" delay data from the original design

To make an assessment of whether the desired performance match or improvement has been achieved, an understanding of the starting point must be reached. The description of the original cell library, with its functional and timing information for each cell, is also essential to the definition of the starting point.

Figure 1. Design Translation Flow



If sample parts of the original design can be provided, performance data on the actual silicon can be used to help establish a baseline.

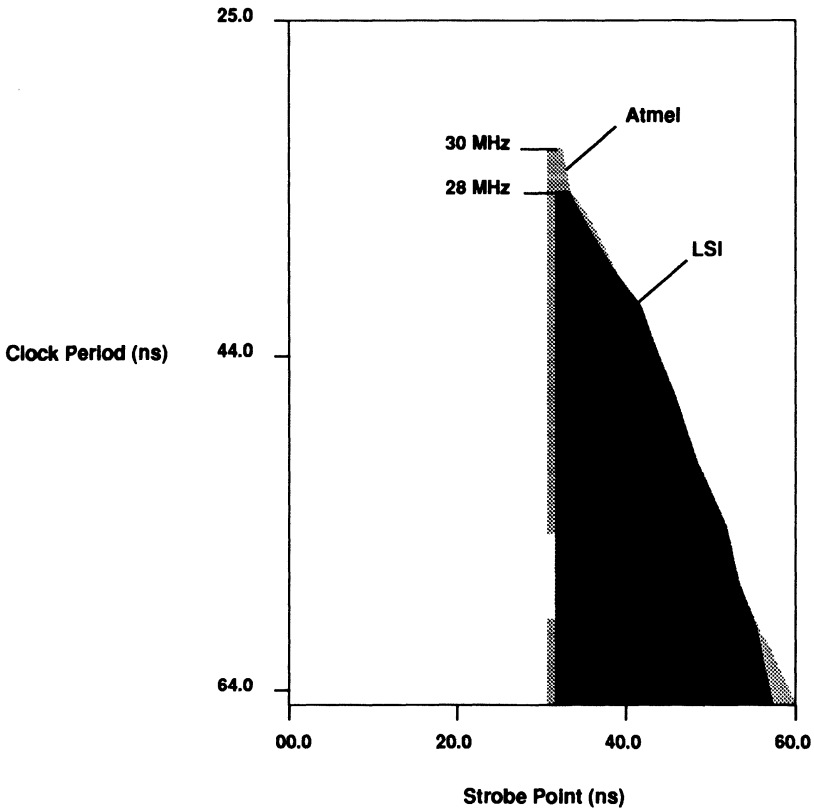
The functional vector set (in ASCII or TSSI, print-on-change format) serves two purposes. The functional vector set, when converted into tester-specific format and used in conjunction with the sample devices, provides a mechanism for establishing detailed performance attributes of the original design. These attributes, such as maximum frequency, path timing performance, and buffer characteristics to name a few, provide the base for cell and buffer selection to match or improve the design. Individual performance attributes can also be used as input to a waveform comparison tool. This tool, using the actual data and the functional test vectors, now converted to simulator format, permits the Atmel designer to determine when and where timing mismatches occur and adjust the netlist accordingly.

The device specification provides key information concerning the required device pin-out, system loading for each pin, the desired performance, and the range of operating conditions.

Performance Matching

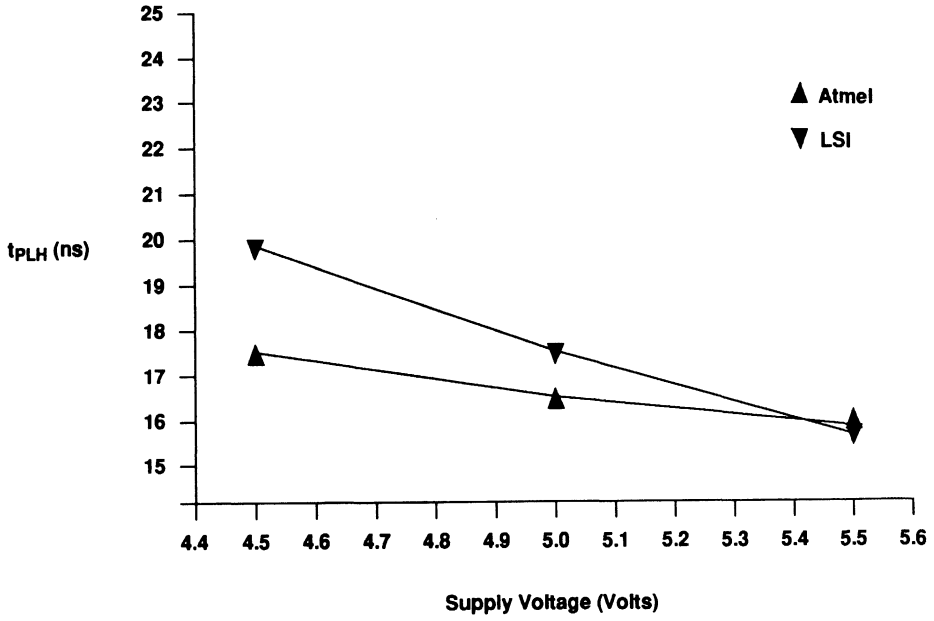
Our first example of ASIC translation presents the results of work performed for a military application, where interchangeability with the original designs was required. The original design was an LSI Logic 10K series gate array of approximately 5,000 gates. The design was asynchronous and had multiple clocks. Samples representing the original designs were available at the outset and were characterized to supplement the specification requirements. All the data

Figure 2. Maximum Operating Frequency, 25°C, V_{DD} = 5.0 V



presented is a direct comparison of LSI Logic and Atmel silicon. Figure 2, depicting maximum operating frequency for constant temperature and voltage, shows how closely the performance can be matched. Figures 3 and 4 depict the average performance for nine critical paths, for low-to-high transitions, both as a function of supply voltage and of temperature. And finally, Figures 5 and 6 depict rise and fall time of bidirectional buffers. The performance match is extremely close.

Figure 3. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, +25°C



The customer performed extensive tester-based characterization and qualification of the Atmel device to insure that it was pin-for-pin compatible, drop-in replacement of the original LSI Logic part. The parts were then assembled onto boards and tested again. The Atmel and LSI parts were interchanged and mixed and matched on boards. The complete system evaluation was performed and in all tests the Atmel parts proved to be equal or superior to the LSI gate array.

Figure 4. Atmel vs LSI Package Test Results for 9 Critical Paths, t_{PLH}, V_{DD} = 5.0 V

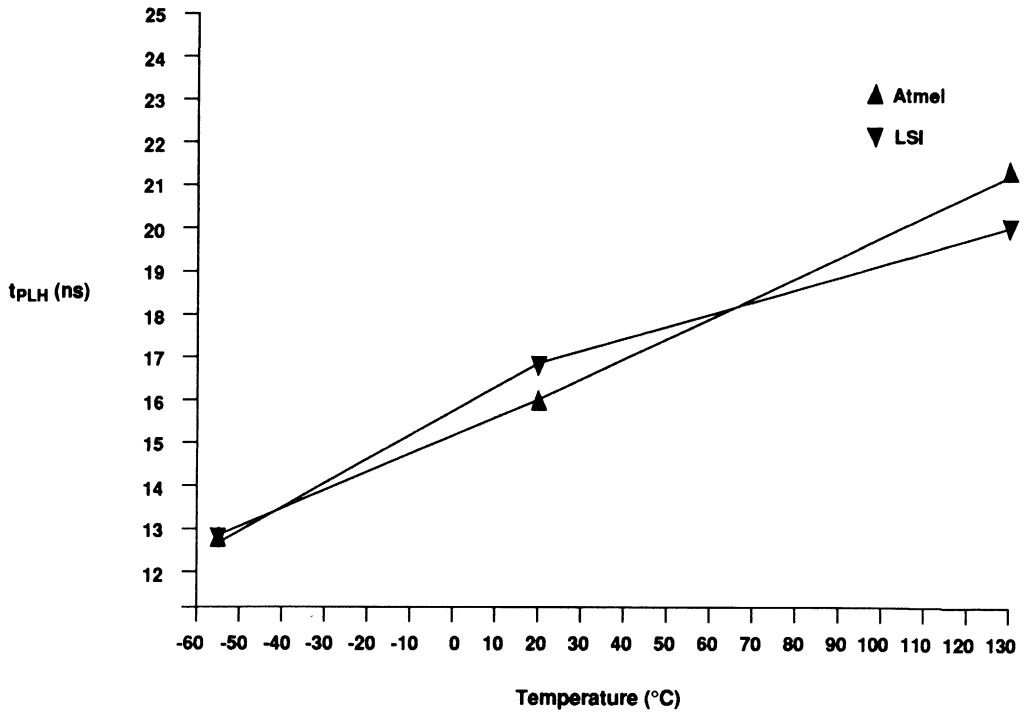


Figure 5. Output Rise Time, 8 mA Bidirectional Buffer, 25°C, 120 pF Load, V_{DD} = 5.0 V

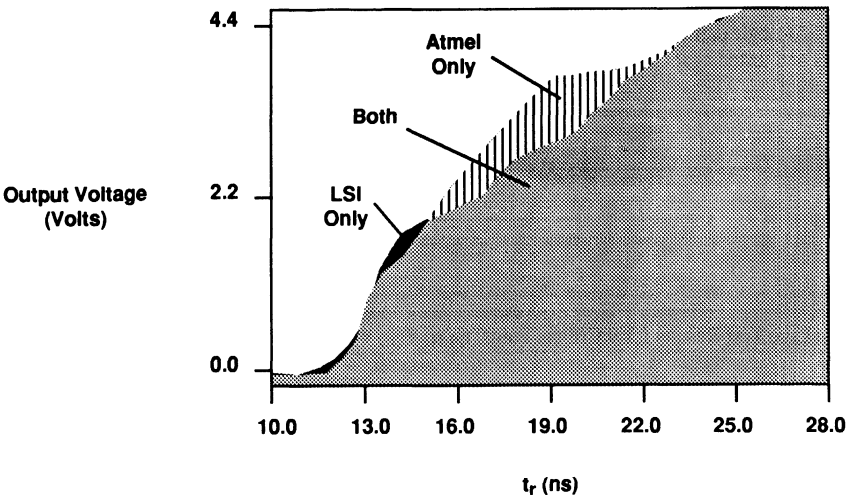
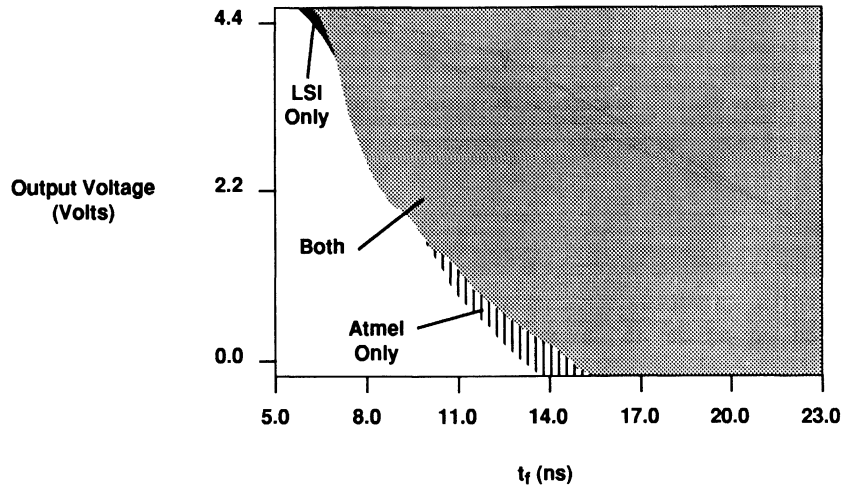


Figure 6. Output Fall Time, 6 mA Bidirectional Buffer 25°C, 120 pF Load, V_{DD} = 5.0 V



Performance Improvement

The second example of ASIC translation presents the results of work performed for a commercial application. This design required approximately 8,000 gates, was completely synchronous, and was operating at 25 MHz. The customer desired an improvement in performance to 33 MHz. To achieve this speed, Atmel compared the performance of its cells to those of the original design, as samples were not available. This evaluation indicated that a 30 to 35 percent speed improvement could be realized over the existing design. Atmel also employed higher drive cells where appropriate to further enhance performance. Extensive board level testing, performed by the customer, confirmed that the Atmel implementation exceeded the 33 MHz design goal over the rated voltage and temperature ranges.

Atmel's CMOS Gate Array Design Manual provides more detailed information about the gate arrays, design methodologies, and individual cell timing, and should be used as a reference for evaluating ASIC performance.

Designing ATL80 Series Gate Arrays For Mixed Voltage Operation

Introduction

As the demand for lower power consumption and voltage has increased the use of 3.3 volt systems, the need for components which can operate in a mixed voltage environment (generally, 3.3 volt and 5.0 volt) has also increased. Gate arrays which operate in a mixed voltage environment have found applications in a wide variety of systems:

- PCMCIA controllers for cards which interface with 3.3 volt and 5.0 volt power supplies
- Bus interfaces for 3.3 volt systems and 5.0 volt buses
- Battery and standard line power systems

Atmel has successfully met the needs of mixed 3.3 volt and 5.0 volt system designs with our ATL and ATL80 series gates. This documentation provides guidance to the gate array designer implementing a mixed voltage design and details the design rules to follow. The focus is on our ATL80 series gate arrays utilizing 3.3 volt and 5.0 volt supplies, but any of our gate array families may be used in a mixed voltage environment.

Overview

In designing gate arrays for mixed voltage operation, there are four primary concerns; speed, output drive, power dissipation and power supply isolation. Atmel has developed comprehensive cell libraries which are characterized for 3.3 volt and 5.0 volt operation in both the ATL and ATL80 series gate arrays. In general, expect a 50% decrease in speed from 5.0 volt to 3.3 volt operation. Likewise, there is approximately a 50% decrease in output drive for a given buffer at 3.3 volts versus 5.0 volts. However, Atmel has special buffers which will maintain equal output drive at both voltage levels. The upside to 3.3 volt operation is that power dissipation is approximately one third to one half of that at 5.0 volts. It is important that these factors are accounted for in the design, and that the designer successfully runs simulations at best and worst case for both voltages. Mixed voltage simulations are possible using the Slew Rate Correction Delay Calculator provided by Atmel for use in Cadence Verilog-XL™.

While the speed, output drive, and power dissipation performance are an inherent part of the 3.3 volt and 5.0 volt operation, power supply isolation must be designed into the gate array by the designer. Many design rules and recommendations in this application note deal with managing power supply isolation.

ATL80 Series Gate Array Mixed Voltage

Application Note

7

Mixed Voltage Options

Atmel provides several options for mixed voltage operation of both the I/O and the core. These options are all discussed in detail later in this application note.

The I/O buffers fall into three categories of mixed voltage operation:

- 3.3 volt and 5.0 volt I/O buffers mixed in the I/O ring
- I/O buffers with selectable 3.3 volt or 5.0 volt operation
- 3.3 volt and 5.0 volt I/O buffers, plus selectable 3.3 volt or 5.0 volt I/O buffers

The core cells fall into two categories of mixed voltage operation:

- a single power plane, 3.3 volt or 5.0 volt, throughout the core (combined with any I/O mixed voltage option)
- 3.3 volt and 5.0 volt isolated power supply columns in varied combination across the core

Design Flow

Designing a gate array for mixed voltage operation is not an automated task, and as a result the design cycle will be longer than for a gate array utilizing a single power plane. The design of all ASICs requires close coordination between the customer and the vendor and this is even more true of mixed voltage ASICs.

Synthesis or Schematic Capture

As with all gate arrays, the process begins with the customer developing a design. Atmel provides cell libraries consisting of schematic symbols, functional models and timing models as well as the v3 Netlist Checker and the tvc Test Vector Checker for the customer's work station. Design platforms supported include Mentor™, Viewlogic™, Cadence™ and Synopsys™. Schematic capture or synthesis is performed by the customer using Atmel libraries, targeting either the ATL or ATL80 series gate arrays.

Insertion of Level Shifters

The customer is responsible for appropriately isolating power planes in the mixed voltage environment. Several design rules direct the placement of level shifters (which is commonly done post synthesis or during schematic capture). There are three modes which are covered by these design rules: Multiple Fixed Isolated Power Supplies with No Power Down, Multiple Fixed Isolated Power Supplies with Power Down, Multiple Variable Isolated Power Supplies. Each mode is covered in more detail in the Mixed Voltage I/O Design Rules section of this application note. Level shifters are supplied by two separate power planes and, unlike any other macro cell provided by Atmel, have their supply pins represented on the schematic symbol and functional/timing model. The customer is responsible for connecting the correct supply to the V_{DD}IN pin (powers the input side of the level shifter) and the V_{DD}OUT pin (powers the output side of the level shifter). Detailed rules for insertion of level shifter follow later in this application note.

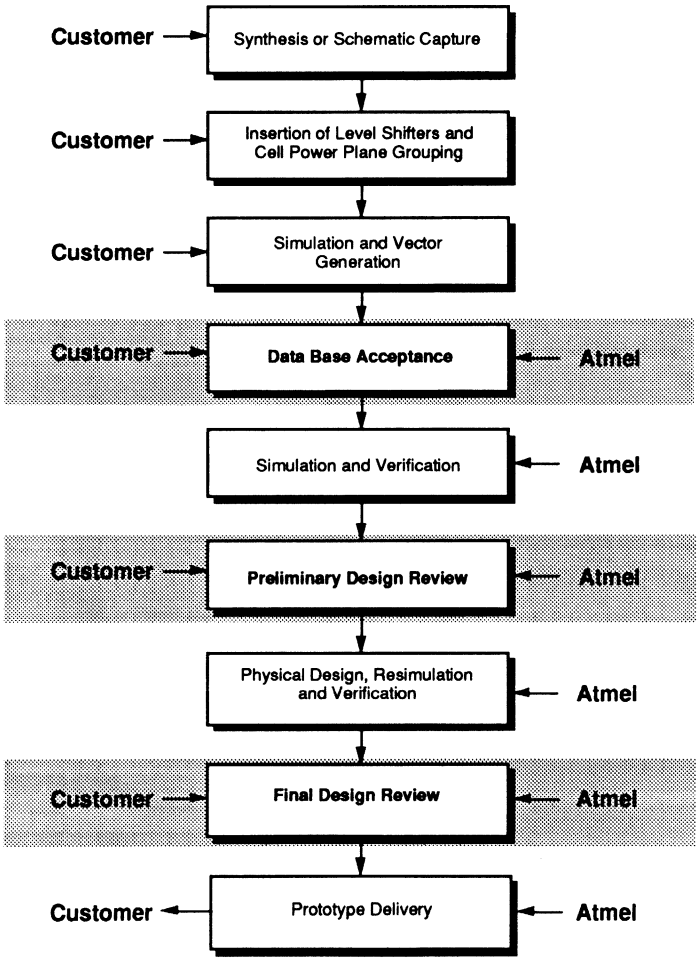
Cell Power Plane Grouping

The level shifters fall between power plane groupings and as such require explicit connection to given power planes. Cells (which receive only one power supply) must be assigned to a power plane group. There should be one group per power plane. The acceptable way to provide cell power plane grouping information for Data Acceptance is an ASCII text file listing "<supply> <instance> pairs (instances may be hierarchal blocks). It is necessary to provide <supply> to <instance> mapping files to the place and route tools as well as the mixed voltage delay calculator since standard macro cells and I/O buffers do not have power supply (or ground) pins represented on their schematic symbol and functional/ timing model.

Simulation and Vector Generation

While Atmel provides cell libraries for a variety of CAD systems, at the time of this printing (November 1994), only the Cadence Verilog-XL simulator (Atmel's golden simulator) and Viewlogic's ViewSim™ are capable of mixed voltage simulation. It will be used as the basis for Preliminary Design Review and Final Design Review approval. Customers can obtain fairly accurate results using other simulators by running separate 3.3 volt and 5.0 volt simulations and combining the results. The customer should simulate their design over the appropriate voltage and temperature ranges; both best case and worst case simulations should pass the same set of test vectors.

Mixed Voltage Gate Array Design Flow



Mixed Voltage Operation of the Core

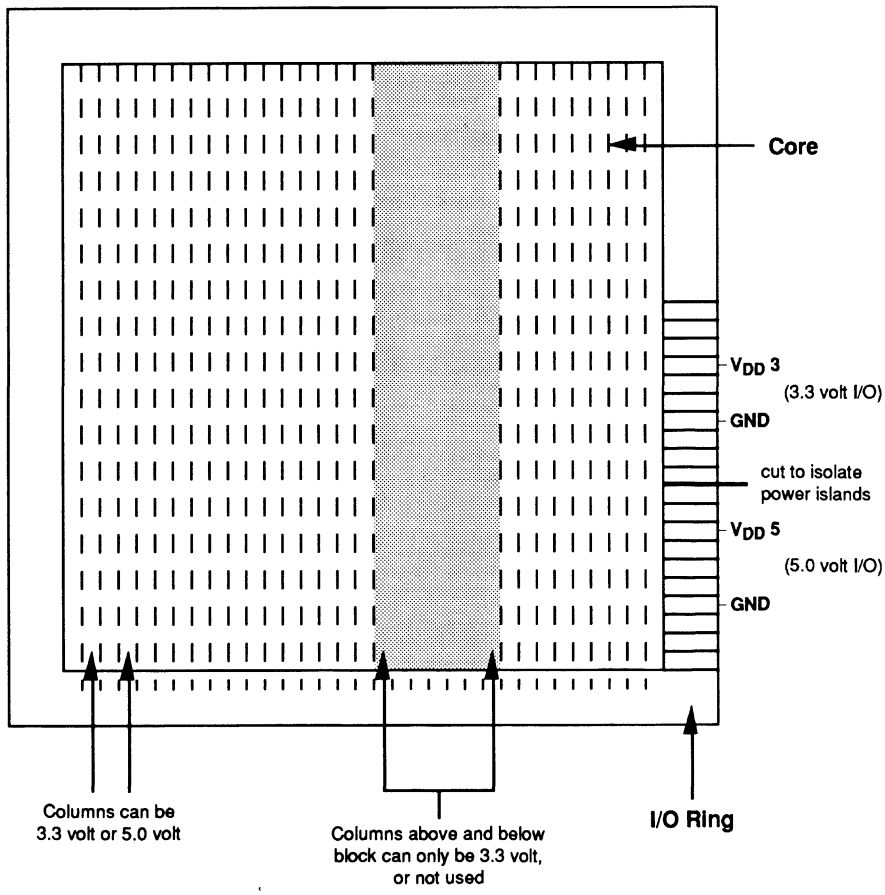
Atmel provides gate arrays in which the core can operate in a mixed voltage environment. However, there are several restrictions on mixed voltage operation based on the power structure of the gate arrays. The main core of the gate array is a sea of gates divided into columns by n-wells. As a result, individual columns must operate at a single voltage, although, the power supply level can vary from column to column. A large block (for example, an SRAM) placed across several columns will dictate the power supply level of these shared columns. This restricts placement above or below the block to cells in its power plane group. Hence, the utilization of the array may be less than if it were supporting one power plane. Also, care should be taken when assigning the I/O placement.

In the ATL80 series gate arrays it is recommended that I/O buffers be placed proximal to others sharing the same power plane. Atmel will cut the supply bus running through the I/O ring to isolate each required power plane. Therefore, each isolated "power island" will have its own power shunt, which uses one I/O site. Also, ESD protection decreases with smaller islands. In the ATL gate array family it is necessary that all I/O on any given side share the same supply.

Since placement of cells can no longer be globally automated, the time required for the physical design effort for a multiple supply gate array is longer than for a single voltage gate array.

Generic ATL80 Architecture

(not to scale)



Mixed Voltage I/O Design Rules

Multiple Fixed Isolated Power Supply (No Power Down)

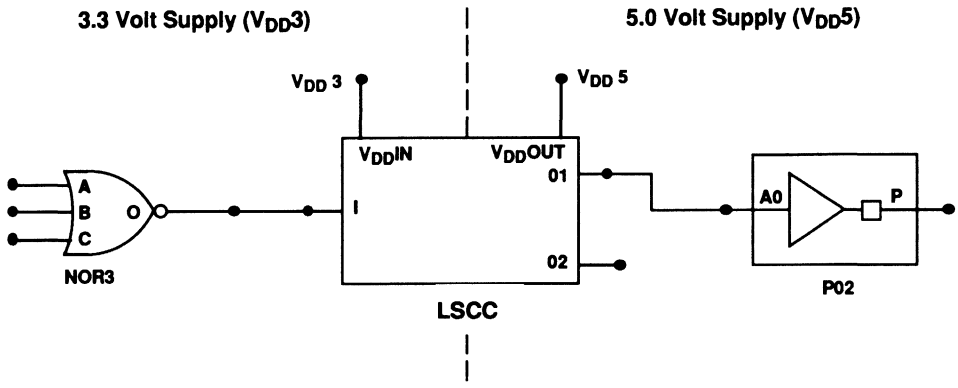
Definition: Each power supply remains at a constant level throughout all modes of operation; loss of any power supply prohibits correct operation. Leakage resulting from a power supply loss or a power supply pulled to ground is not a design concern. Typically, the core and most of the I/O are on one power plane and some bus I/O and associated core logic are on a second power plane.

Interface Requirement

3.3 volt to 5.0 volt (Figure 1):

- tristate buses not allowed across interface
- insertion of level shifter (LSCC) is required; the V_{DD}IN pin is explicitly connected to the 3.3 volt supply and the V_{DD}OUT pin is explicitly connected to 5.0 volt supply

Figure 1

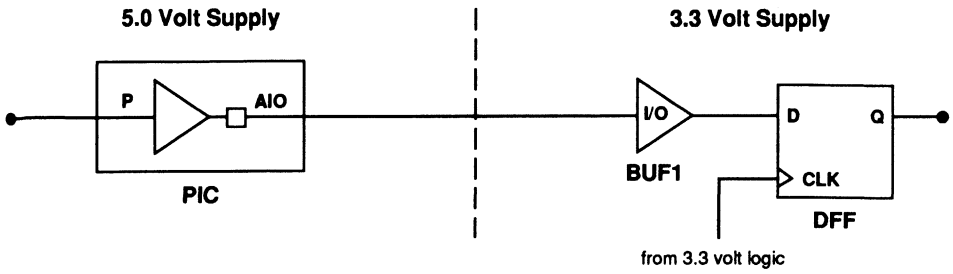


Interface Requirement

5.0 volt to 3.3 volt (Figure 2):

- tristate buses not allowed across interface
- 5.0 volt logic must drive transistor gate logic (such as INV, BUF, NAND, NOR); cannot drive flip flop or MUX directly (t-gate inputs result in forward biased PN-junction)
- level shifter not necessary (use INV or BUF to drive flip flop or MUX)

Figure 2



Multiple Fixed Isolated Power Supply (Power Down)

Definition: Each power supply remains at a constant level throughout its mode of operation; however, loss of a power supply (floating or grounded) requires correct operation with minimum power dissipation in the remaining supplied logic.

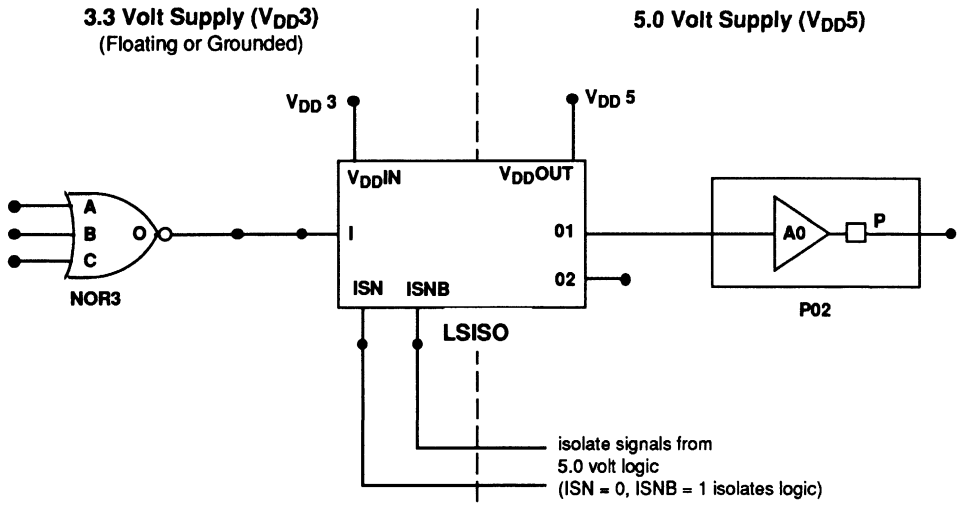
The designer must provide a logic signal (as a true/complement pair) from a still active power plane which indicates when power to another plane has gone. This true/complement pair must be explicitly connected to the isolating level shifter (LSISO) inserted between the anticipated power down plane and an active power plane. The isolating level shifter prevents floating gates on supplied logic from dissipating power.

Interface Requirement

3.3 volt to 5.0 volt — 3.3 volt floating or grounded supply (Figure 3):

- tristate buses not allowed across interface
- insertion of isolating level shifter (LSISO) is required; the V_{DD}IN pin is explicitly connected to the 3.3 volt supply and the V_{DD}OUT pin is explicitly connected to 5.0 volt supply; the true/complement pair indicating a power down is explicitly connected to the ISN/ISNB pins, respectively.

Figure 3

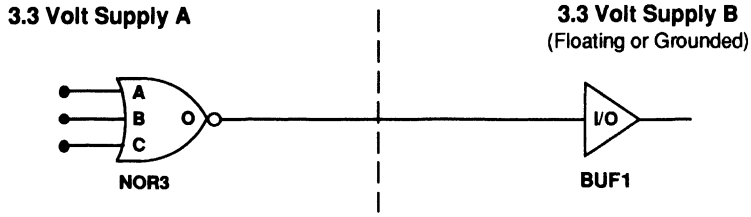


Interface Requirement

"A" volt to "B" volt — A > = B, B volt disappearing (Figure 4):

- tristate buses not allowed across interface
- "A" volt logic must drive transistor gate logic (such as INV, BUF, NAND, NOR); cannot drive flip flop or MUX directly (t-gate inputs result in forward biased PN-junction)
- level shifter not necessary (use INV or BUF to drive flip flop or MUX)

Figure 4



Multiple Variable Isolated Power Supply

Definition: A power supply may vary between two levels during operation; typically, the core and most of the I/O remain at a constant level while some bus I/O and associated core logic may or may not equal the constant supply level in some uses of the IC.

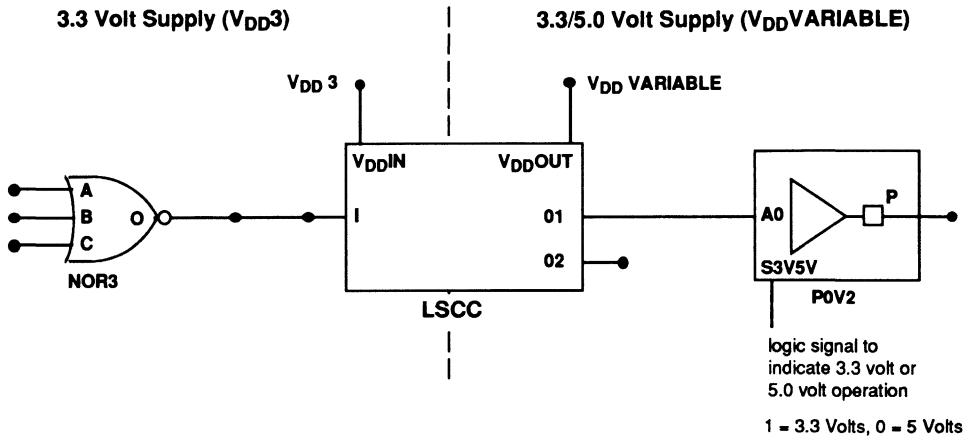
The designer must provide a logic signal to indicate 3.3 volt or 5.0 volt operation. Special input and output buffers are available which have a 3.3 volt/5.0 volt operation pin (S3V5V). With the selectable voltage output buffers the designer can be assured of a constant output drive at either level of operation. Note: CMOS input buffers do not require selectability; therefore, there are only TTL versions of these special input buffers.

Interface Requirement

3.3 volt to 3.3/5.0 volt (Figure 5):

- tristate buses not allowed across interface
- insertion of isolating level shifter (LSCC) is required; the V_{DD}IN pin is explicitly connected to 3.3 volt supply and the V_{DD}OUT pin is explicitly connected to 3.3/5.0 volt variable supply
- the level shifter will still operate across a 3.3 volt to 3.3 volt interface

Figure 5

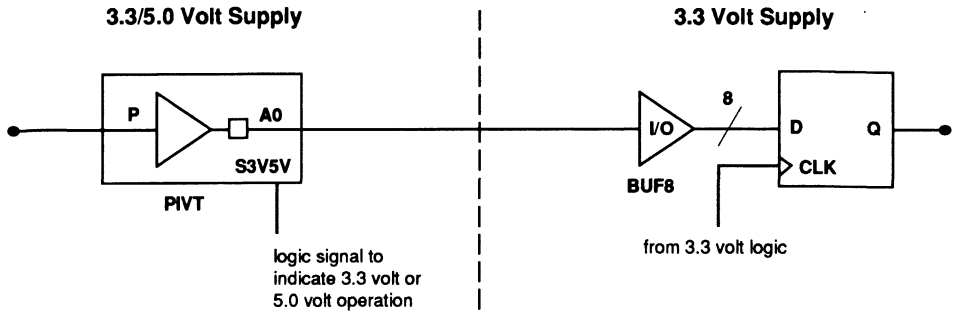


Interface Requirement

3.3/5.0 volt to 3.3 volt (Figure 6):

- tristate buses not allowed across interface
- 3.3/5.0 volt logic must drive transistor gate logic (such as INV, BUF, NAND, NOR); cannot drive flip flop or MUX directly (t-gate inputs result in forward biased PN-junction)
- level shifter not necessary (use INV or BUF to drive flip flop or MUX)

Figure 6



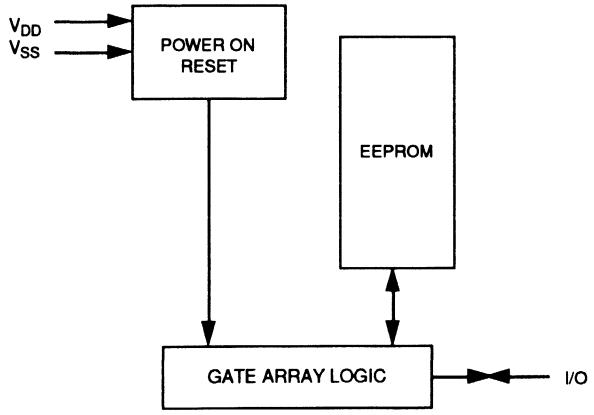
Contents

8

Features

- Parallel E²PROM Memory (8 bit word)
- Gate Array for Logic Design
- Up to 120 I/O
- Low Voltage Operation (2.7 to 5.5 Volts)
- Single Voltage Supply Operation
- Performs Page Write Function
- Manufactured Using Low Power CMOS Technology
- Write or Erase Time: 10 ms Maximum
- Temperature Range from -40°C to 85°C
- ESD Immunity > 4K Volts
- High Reliability and Endurance:
  - 10,000 Write/Erase Cycles
  - 10 Years Data Retention
- Ideal for Portable, Secure Applications Including PCMCIA Cards, Smart Cards, ID Tags, Keys, etc.

Block Diagram



Description

The AT88SCXXX provides 1K to 16K bits of E²PROM (Electrically Erasable and Programmable Read Only Memory) with 800 to 10K CMOS usable gates for use as personalization, security, and glue logic. The AT88SCXXX is ideal for new portable applications requiring an E²PROM with custom logic.

The outputs of the AT88SCXXX can sink and source up to 8 mA. There are up to 120 buffer sites which are configurable as inputs, outputs, bidirectional, CMOS or TTL operation. The device also provides pull-down and pull-up capability for floating signals. The AT88SCXXX is manufactured using low-power CMOS technology and features its own internal high voltage pump for single voltage supply operation. The devices are guaranteed to 10,000 erase/write cycles and 10 years data retention.

E² Logic ICs

Serial / Parallel E²PROM with Gate Array

AT88SC150
AT88SC200
AT88SC220
AT88SC250
AT88SC410
AT88SC450
AT88SC8100
AT88SC1610

Preliminary

8

0319B

Atmel or the customer can personalize the gate array as described in Figure 1. The customer's design can be accepted in one of three formats:

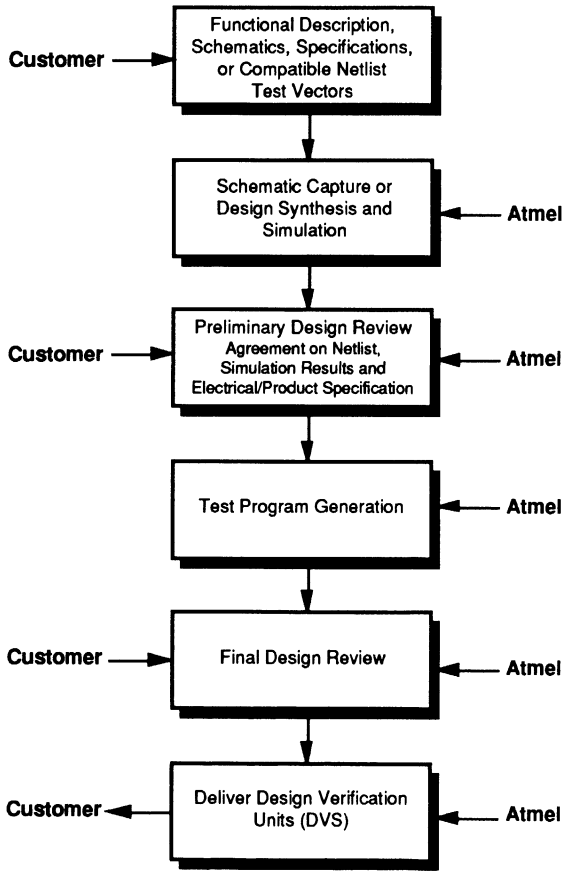
- Functional Description
- Schematic
- Compatible Netlist

Compatible netlists can be generated from Mentor™, Cadence™, Viewlogic™. The personalized devices are available in wafer, die, or standard packages.

E² Logic Family

Device Name	EEPROM Bits	Number of Usable Gates	Number of I/O	Package Type
AT88SC150	1,024	5,000	100	PQFP/TQFP/PLCC
AT88SC200	2,048	800	8	PDIP/SOIC
AT88SC220	2,048	2,000	64	PQFP/TQFP/PLCC
AT88SC250	2,048	5,000	100	PQFP/TQFP/PLCC
AT88SC410	4,096	1,000	24	PDIP/SOIC
AT88SC450	4,096	5,000	100	PQFP/TQFP/PLCC
AT88SC8100	8,192	10,000	128	PQFP/TQFP/PLCC
AT88SC1610	16,384	1,000	8	PDIP/SOIC

Figure 1. AT88SCXXX Design Flow



Cadence, Mentor, and Viewlogic may be trademarks of others.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Maximum Operating Voltage	6.1 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_{AMB} = -40°C to +85°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V (unless otherwise specified)

Symbol	Characteristics	Min	Typ	Max	Unit
I_{CC}	Supply Current on V_{CC} (t_{AMB} = + 25°C) (open output buffers)		TBD		mA
I_{CCP}	Supply Current on V_{CC} during E²PROM Program (t_{AMB} = + 25°C).		TBD		mA
V_{IL}	TTL Input Low Voltage			0.8	V
V_{IL}	CMOS Input Low Voltage			0.3 x V_{DD}	V
V_{IH}	TTL Input High Voltage	2.0			V
V_{IH}	CMOS Input High Voltage	0.7 x V_{DD}			V
V_{OL}	Output Low Level (I_{OL} = 8 mA)			0.4	V
V_{OH}	Output High Level (I_{OH} = 8 mA)	0.7 x V_{DD}			V
I_L	I/O Leakage Current	-50		50	µA

Packaging

All Atmel E² logic memory ICs are available in wafer, die, or standard packaging. Back grinding is an option.

Packaging Options

Package Type	Pin Count
PQFP	44, 52, 64, 80, 100, 120, 128
TQFP	32, 44, 64, 80, 100, 120, 128
PLCC	20, 32, 44, 52, 68, 84
PDIP	8, 16, 24, 32, 40
SOIC	8, 16, 32
Tested Die	Waffle Packs
Tested Die	Wafer Form

Contents

9

Introduction to the SMD Product Listing

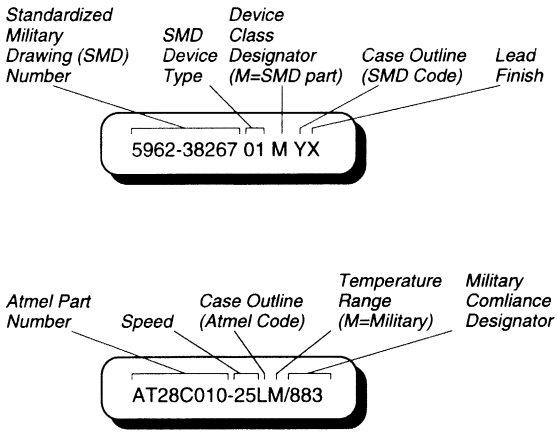
Each Standardized Military Drawing (SMD) part number that Atmel supplies corresponds to an Atmel /883 part number. SMD products are compliant to MIL-STD-883, paragraph 1.2.1 and to the requirements of the applicable standardized military drawing. The tables in this section list the currently approved Atmel SMD parts by Atmel part number (Table 1) and by SMD part number (Table 2). They define and cross reference the Atmel /883 part number with the SMD part number for your ordering convenience.

Figure 1 (below) shows how an Atmel SMD order number defines a part, compared to the components of the Atmel similar part number.

Please note that some SMD part numbers contain the letter "M" between the device type and the case outline designator. The "M" is part of the one part-one part number system, set up by DESC. It is a device class designator which indicates the part is an SMD part number as opposed to being a JAN part number.

Standard Military Drawing PLD Offering

Figure 1. Components of an SMD number (top) compared to the Atmel similar part number (bottom).



How to Use the Atmel Part Type Reference Table

The organization of Table 1 enables the purchaser to order a standardized military part by using the Atmel generic part type to locate the correct SMD drawing number. The SMD part number is the order number for SMD devices. The Atmel generic part type, which begins with the prefix "AT," heads Table 1. There are four sections in this table (see the sample table on page 2):

SMD Options

The first section lists the SMD options available at Atmel. It includes the industry generic part type, the SMD drawing number, and the SMD device type. The first section also lists the SMD case outline options, the lead finish options, the circuit description, and the access time that correspond to that device type.

0478A

Order Code Cross-Reference

The next section of the table cross-references each optionally complete SMD part number (see ❶ below) with the Atmel similar /883 part number (see ❷ below).

Case Outline Legend

The third section gives the SMD case outline options available for the device.

Lead Finish Legend

The last section lists the SMD lead finish options available for the device.

SMD Options with PartDescription and Specifications

Order Code Cross-Reference

Case Outline Legend

Lead Finish Legend

ATF22V10B

Generic Number	Standardized Military Drawing Number				Description	
22V10	Drawing Numbe	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89841	03	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15
	5962-89841	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25

Atmel Cage No. 1RN4I	Example: Atmel Order Number	Atmel Similar Part Number
	❶ 5962-89841 **01** LA	❷ ATF22V10B-15GM/883
	5962-89841 **01** 3X	ATF22V10B-15NM/883
	5962-89841 **05** 3X	ATF22V10B-10GM/883

Case Outline	
L	24D3, 24 Lead 0.300" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

How to Use the Atmel SMD Number Reference Table

Table 2 allows quick reference to the Atmel /883 similar part number when the purchaser knows the SMD part number. The head for Table 2 is the SMD drawing number (see the example table below). This table contains a cross-reference between the optionally complete SMD drawing number (see ❶ below) and the corresponding Atmel similar /883 part number (see ❷ below). It also includes the circuit description and access time for that part number.

Order Codes *Part Description and Specifications*

Order Code Cross-Reference

5962-89841

❶ Atmel Order Number	❷ Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-89841 03 LA	ATF22V10B-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 03 3X	ATF22V10B-15NM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 04 LA	ATF22V10B-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89841 04 3X	ATF22V10B-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89841 05 LA	ATF22V10B-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 05 3X	ATF22V10B-15NM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 06 LA	ATF22V10B-10GM/883	22-Input, 10-Output and-or-Logic Array	10
5962-89841 06 3X	ATF22V10B-10NM/883	22-Input, 10-Output and-or-Logic Array	10

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22V10

Generic Number	Standardized Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
C22V10	5962-87539	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-87539	05	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87539 **01 LA**	AT22V10-25DM/883
	5962-87539 **01 3X**	AT22V10-25LM/883
	5962-87539 **05 LA**	AT22V10-15DM/883
	5962-87539 **05 3X**	AT22V10-15LM/883

AT22V10B

Generic Number	Standardized Military Drawing Number				Description	
	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
C22V10B	5962-87539	06	L, 3, X	X, A, C	22-Input, 10-Output and-or-Logic Array	10

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-87539 **06 LA**	AT22V10B-10DM/883
	5962-87539 **06 3X**	AT22V10B-10LM/883
	5962-87539 **06 XX**	AT22V10B-10KM/883

Case Outline	
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22V10L

Generic Number	Standardized Military Drawing Number				Description	
C22V10L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88724	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88724	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88724 **01 LA**	AT22V10L-25DM/883
	5962-88724 **01 3X**	AT22V10L-25LM/883
	5962-88724 **04 LA**	AT22V10L-20DM/883
	5962-88724 **04 3X**	AT22V10L-20LM/883

Case Outline	
L	24D3, 24 Lead 0.300" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATF22V10B

Generic Number	Standardized Military Drawing Number				Description	
22V10	Drawing Numbe	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89841	03	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15
	5962-89841	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-89841	05	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15
	5962-89841	06	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	10

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89841 **01 LA**	ATF22V10B-15GM/883
	5962-89841 **01 3X**	ATF22V10B-15NM/883
	5962-89841 **02 LA**	ATF22V10B-25GM/883
	5962-89841 **02 3X**	ATF22V10B-25NM/883
	5962-89841 **04 LA**	ATF22V10B-15GM/883
	5962-89841 **04 3X**	ATF22V10B-15NM/883
	5962-89841 **05 LA**	ATF22V10B-10GM/883
	5962-89841 **05 3X**	ATF22V10B-10GM/883

Case Outline	
L	24D3, 24 Lead 0.300" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22LV10

Generic Number	Standardized Military Drawing Number				Description	
C22V10	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-93245	01M	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-93245 **01M LA**				AT22LV10-25DM/883	
	5962-93245 **01M 3X**				AT22LV10-25LM/883	

AT22LV10L

Generic Number	Standardized Military Drawing Number				Description	
C22V10	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-93245	03M	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	30
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-93245 **03M LA**				AT22LV10L-30DM/883	
	5962-93245 **03M 3X**				AT22LV10L-30LM/883	

Case Outline	
L	24DW3, 24 Lead 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

AT22V10 OTP

Generic Number	Standardized Military Drawing Number				Description	
C22V10 OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88670	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88670	05	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88670 **01 LA**	AT22V10-25GM/883
	5962-88670 **01 3X**	AT22V10-25NM/883
	5962-88670 **05 LA**	AT22V10-15GM/883
	5962-88670 **05 3X**	AT22V10-150NM/883

AT22V10L OTP

Generic Number	Standardizedized Military Drawing Number				Description	
C22V10L OTP	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-89755	01	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-89755	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-89755 **01 LA**	AT22V10L-25GM/883
	5962-89755 **01 3X**	AT22V10L-25NM/883
	5962-89755 **04 LA**	AT22V10L-20GM/883
	5962-89755 **04 3X**	AT22V10L-20NM/883

9

Case Outline	
L	24D3, 24 Lead 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV750

Generic Number	Standardized Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	03	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88726	04	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20
	5962-88726	08	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	10
	5962-88726	09	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15
	5962-88726	10	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88726 **03 LA**	ATV750-25DM/883
	5962-88726 **03 3X**	ATV750-25LM/883
	5962-88726 **04 LA**	ATV750-20DM/883
	5962-88726 **04 3X**	ATV750-20LM/883
	5962-88726 **08 LA**	ATV750-10DM/883
	5962-88726 **08 3X**	ATV750-10LM/883
	5962-88726 **09 LA**	ATV750-15DM/883
	5962-88726 **09 3X**	ATV750-15LM/883
	5962-88726 **10 LA**	ATV750-25DM/883
	5962-88726 **10 3X**	ATV750-25LM/883

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV750L

Generic Number	Standardized Military Drawing Number				Description	
V750L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-88726	07	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-88726	11	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	15
	5962-88726	12	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-88726 **07 LA**	ATV750L-25DM/883
	5962-88726 **07 3X**	ATV750L-25LM/883
	5962-88726 **11 LA**	ATV750L-15DM/883
	5962-88726 **11 3X**	ATV750L-15LM/883
	5962-88726 **12 LA**	ATV750L-25LM/883
	5962-88726 **12 3X**	ATV750L-25DM/883

Case Outline	
L	24DW3, 24 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
3	28LW, 28 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Y	28KW, 28 Lead, Windowed or Non-windowed, J Leaded Ceramic Chip Carrier (JLCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV750 OTP

Generic Number	Standardized Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-94524	02M	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
	5962-94524	03M	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	20
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-94524 **02M LA**				ATV750-25GM/883	
	5962-94524 **02M 3X**				ATV750-25NM/883	
	5962-94524 **03M LA**				ATV750-20GM/883	
	5962-94524 **03M 3X**				ATV750-20NM/883	

ATV750L OTP

Generic Number	Standardized Military Drawing Number				Description	
V750	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-94524	05M	L, 3	X, A, C	22-Input, 10-Output and-or-Logic Array	25
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-94524 **05M LA**				ATV750L-25GM/883	
	5962-94524 **05M 3X**				ATV750L-25NM/883	

Case Outline	
L	24D3, 24 Lead 0.300" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
3	28L, 28 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV2500H

Generic Number	Standardized Military Drawing Number				Description	
V2500	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	02	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	25

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-91545 **02M QA**	ATV2500H-25DM/883
	5962-91545 **02M XX**	ATV2500H-25LM/883
	5962-91545 **02M YX**	ATV2500H-25KM/883

ATV2500L

Generic Number	Standardized Military Drawing Number				Description	
V2500L	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	03	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	30

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-91545 **03M QA**	ATV2500L-30DM/883
	5962-91545 **03M XX**	ATV2500L-30LM/883
	5962-91545 **03M YX**	ATV2500L-30KM/883

ATV2500B

Generic Number	Standardized Military Drawing Number				Description	
V2500B	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	04	X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	15

Atmel Cage No. 1FN41	Example: Atmel Order Number	Atmel Similar Part Number
	5962-91545 **04M XX**	ATV2500B-15LM/883
	5962-91545 **04M YX**	ATV2500B-15KM/883

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV2500BL

Generic Number	Standardized Military Drawing Number				Description	
V2500BL	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	05	X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	20
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-91545 **05M XX**				ATV2500BL-20LM/883	
	5962-91545 **05M YX**				ATV2500BL-20KM/883	

ATV2500BQ

Generic Number	Standardized Military Drawing Number				Description	
V2500BQ	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	06	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	25
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-91545 **06M XX**				ATV2500BQ-25LM/883	
	5962-91545 **06M YX**				ATV2500BQ-25KM/883	
	5962-91545 **06M QA**				ATV2500BQ-25KM/883	

ATV2500BQL

Generic Number	Standardized Military Drawing Number				Description	
V2500BQL	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-91545	07	Q,X,Y	X, A, C	38-Input, 24-Output and-or-Logic Array	30
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-91545 **07M XX**				ATV2500BQL-30LM/883	
	5962-91545 **07M YX**				ATV2500BQL-30KM/883	
	5962-91545 **07M QA**				ATV2500BQL-30KM/883	

Case Outline	
Q	40DW6, 40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
X	44LW, 44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Y	44KW, 44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 1. Atmel SMD Part Types, Listed by Atmel Part Number *(continued)*

ATV5000

Generic Number	Standardized Military Drawing Number				Description	
V5000	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-93248	02M	X,Y	X, A, C	60-Input, 52-Output and-or-Logic Array	35
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-93248 **02M XX**				ATV5000-35KM/883	
	5962-93248 **02M YX**				ATV5000-35UM/883	

ATV5000L

Generic Number	Standardized Military Drawing Number				Description	
V5000	Drawing Number	Device Type	Case Outline	Lead Finish	Circuit Description	TPD (ns)
	5962-93248	03M	X,Y	X, A, C	60-Input, 52-Output and-or-Logic Array	35
Atmel Cage No. 1FN41	Example: Atmel Order Number				Atmel Similar Part Number	
	5962-93248 **03M XX**				ATV5000L-35KM/883	
	5962-93248 **03M YX**				ATV5000L-35UM/883	

Case Outline	
MX	68 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
MY	68 Lead, Windowed, Ceramic Pin Grid Array(PGA)
Lead Finish	
X	Allows Hot Tin Dip or Gold (AU)
A	Hot Tin Dip
C	Gold (AU)

Table 2. Atmel SMD Part Types, Listed by SMD Number

5962-87539			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**TPD (ns)**
5962-87539 01 LA	AT22V10-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 01 3X	AT22V10-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-87539 05 LA	AT22V10-15DM/883	22-Input, 10-Output and-or-Logic Array	15
5962-87539 05 3X	AT22V10-15LM/883	22-Input, 10-Output and-or-Logic Array	15
5962-87539 06 LA	AT22V10B-10DM/883	22-Input, 10-Output and-or-Logic Array	10
5962-87539 06 3X	AT22V10B-10LM/883	22-Input, 10-Output and-or-Logic Array	10

5962-88670			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**TPD (ns)**
5962-88670 01 LA	AT22V10-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 01 3X	AT22V10-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88670 05 LA	AT22V10-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88670 05 3X	AT22V10-15NM/883	22-Input, 10-Output and-or-Logic Array	15

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-88724

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-88724 01 LA	AT22V10L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 01 3X	AT22V10L-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88724 04 LA	AT22V10L-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88724 04 3X	AT22V10L-20LM/883	22-Input, 10-Output and-or-Logic Array	20

5962-88726

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-88726 03 LA	ATV750-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 03 3X	ATV750-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 04 LA	ATV750-20DM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88726 04 3X	ATV750-20LM/883	22-Input, 10-Output and-or-Logic Array	20
5962-88726 07 LA	ATV750L-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 07 3X	ATV750L-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 08 LA	ATV750B-10DM/883	22-Input, 10-Output and-or-Logic Array	10
5962-88726 08 3X	ATV750B-10LM/883	22-Input, 10-Output and-or-Logic Array	10
5962-88726 09 LA	ATV750B-15DM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88726 09 3X	ATV750B-15LM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88726 10 LA	ATV750B-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 10 3X	ATV750B-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 11 LA	ATV750B-15DM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88726 11 3X	ATV750B-15LM/883	22-Input, 10-Output and-or-Logic Array	15
5962-88726 12 LA	ATV750B-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-88726 12 3X	ATV750B-25LM/883	22-Input, 10-Output and-or-Logic Array	25

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-89755			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**TPD (ns)**
5962-89755 01 LA	AT22V10L-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 01 3X	AT22V10L-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89755 04 LA	AT22V10L-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-89755 04 3X	AT22V10L-20NM/883	22-Input, 10-Output and-or-Logic Array	20

5962-89841			
Atmel Order Number	**Atmel Similar Part Number**	**Circuit Description**	**TPD (ns)**
5962-89841 03 LA	ATF22V10B-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 03 3X	ATF22V10B-15NM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 04 LA	ATF22V10B-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89841 04 3X	ATF22V10B-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-89841 05 LA	ATF22V10B-15GM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 05 3X	ATF22V10B-15NM/883	22-Input, 10-Output and-or-Logic Array	15
5962-89841 06 LA	ATF22V10B-10GM/883	22-Input, 10-Output and-or-Logic Array	10
5962-89841 06 3X	ATF22V10B-10NM/883	22-Input, 10-Output and-or-Logic Array	10

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-91545

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-91545 02M QA	ATV2500H-25DM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 02M XX	ATV2500H-25LM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 02M YX	ATV2500H-25KM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 03M QA	ATV2500L-30DM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 03M XX	ATV2500L-30LM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 03M YX	ATV2500L-30KM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 04M XX	ATV2500B-15LM/883	38-Input, 24-Output and-or-Logic Array	15
5962-91545 04M YX	ATV2500B-15KM/883	38-Input, 24-Output and-or-Logic Array	15
5962-91545 05M XX	ATV2500BL-20LM/883	38-Input, 24-Output and-or-Logic Array	20
5962-91545 05M YX	ATV2500BL-20KM/883	38-Input, 24-Output and-or-Logic Array	20
5962-91545 06M XX	ATV2500BQ-25LM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 06M YX	ATV2500BQ-25KM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 06M QA	ATV2500BQ-25DM/883	38-Input, 24-Output and-or-Logic Array	25
5962-91545 07M XX	ATV2500BQL-30LM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 07M YX	ATV2500BQL-30KM/883	38-Input, 24-Output and-or-Logic Array	30
5962-91545 07M QA	ATV2500BQL-30DM/883	38-Input, 24-Output and-or-Logic Array	30

5962-93245

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-93245 01M LA	AT22LV10-25DM/883	22-Input, 10-Output and-or-Logic Array	25
5962-93245 01M 3X	AT22LV10-25LM/883	22-Input, 10-Output and-or-Logic Array	25
5962-93245 03M LA	AT22LV10-30DM/883	22-Input, 10-Output and-or-Logic Array	30
5962-93245 03M 3X	AT22LV10-30LM/883	22-Input, 10-Output and-or-Logic Array	30

Table 2. Atmel SMD Part Types, Listed by SMD Number *(continued)*

5962-93248

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-93248 02M XX	ATV5000-35UM/883	60-Input, 52-Output and-or-Logic Array	35
5962-93248 02M YX	ATV5000-35KM/883	60-Input, 52-Output and-or-Logic Array	35
5962-93248 03M XX	ATV5000L-35UM/883	60-Input, 52-Output and-or-Logic Array	35
5962-93248 03M YX	ATV5000L-35KM/883	60-Input, 52-Output and-or-Logic Array	35

5962-94524

Atmel Order Number	Atmel Similar Part Number	Circuit Description	TPD (ns)
5962-94524 01M LA	ATV750-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-94524 01M 3X	ATV750-25NM/883	22-Input, 10-Output and-or-Logic Array	25
5962-94524 03M LA	ATV750-20GM/883	22-Input, 10-Output and-or-Logic Array	20
5962-94524 03M 3X	ATV750-20NM/883	22-Input, 10-Output and-or-Logic Array	20
5962-94524 05M LA	ATV750L-25GM/883	22-Input, 10-Output and-or-Logic Array	25
5962-94524 05M 3X	ATV750L-25NM/883	22-Input, 10-Output and-or-Logic Array	25

Contents

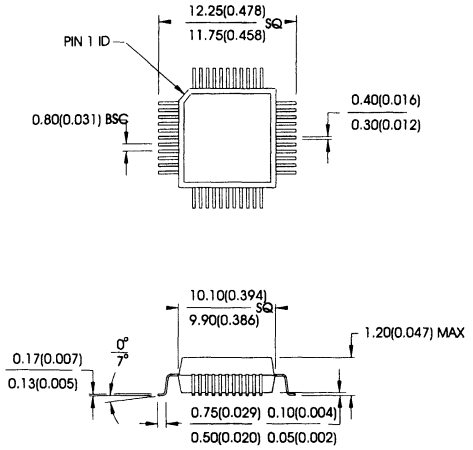
10

Standard Package Outlines

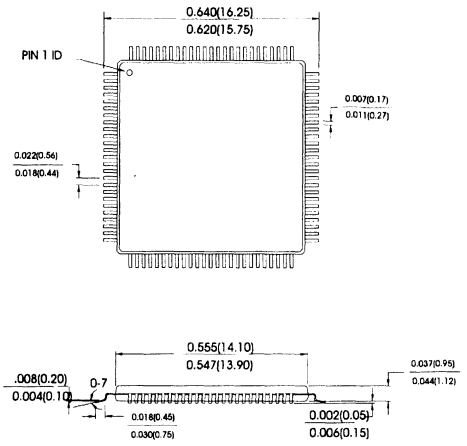
Each Atmel data sheet includes an Ordering Information Section which specifies the package types available. This section provides size specifications and outlines for all package types.[1]

Note: 1. Dimensions shown do not include lead plating or mold flash.

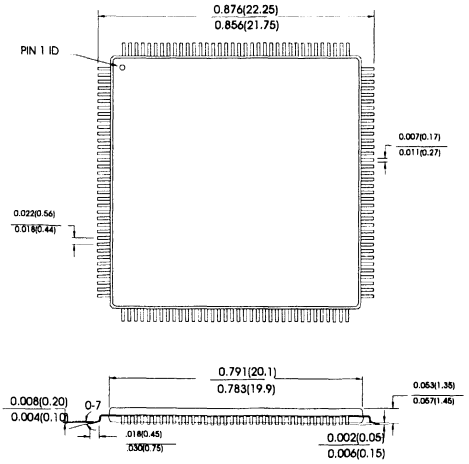
44A, 44 Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Inches and (Millimeters)



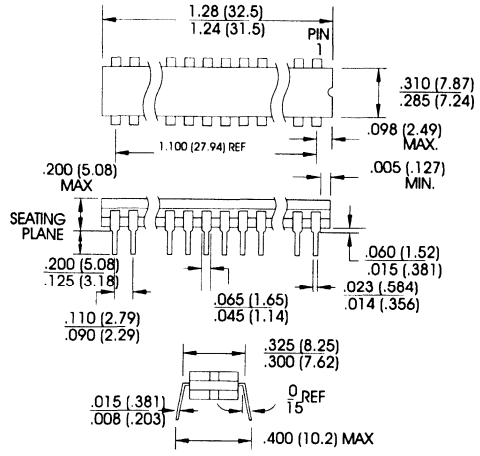
100A, 100 Lead, Very Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (VQFP)
Dimensions in Inches and (Millimeters)



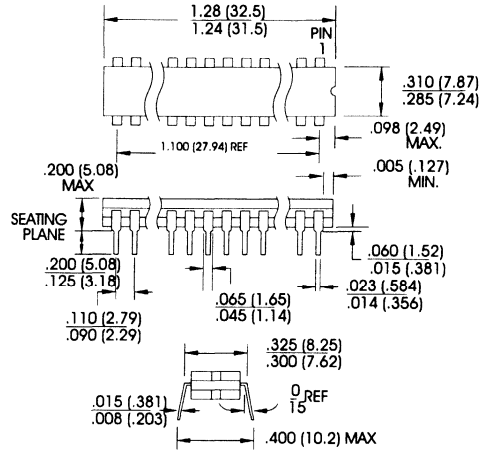
144A, 144 Lead, Thin (1.4 mm) Plastic Gull Wing Quad Flat Package (TQFP)
Dimensions in Inches and (Millimeters)



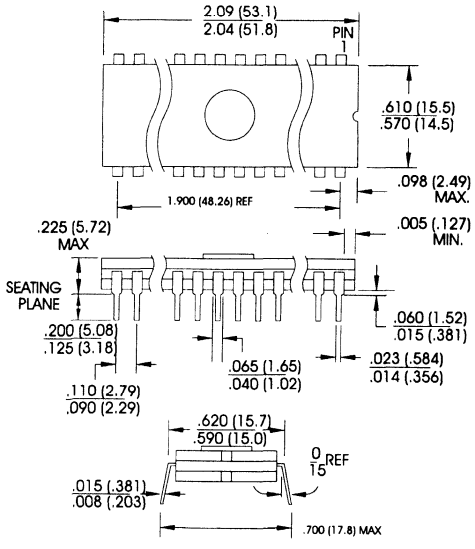
24D3, 24 Lead, 0.300" Wide, Non-Windowed
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A



24DW3, 24 Lead, 0.300" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-9 CONFIG A

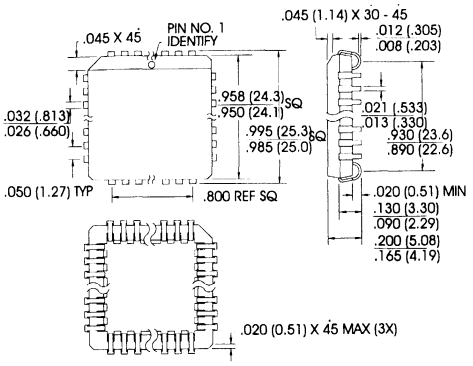


40DW6, 40 Lead, 0.600" Wide, Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A

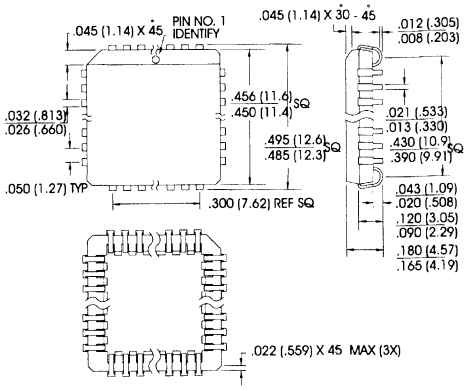


10

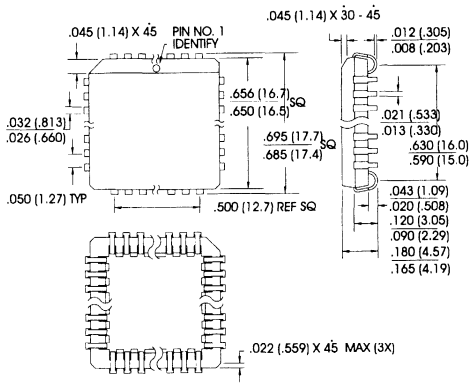
20J, 20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)



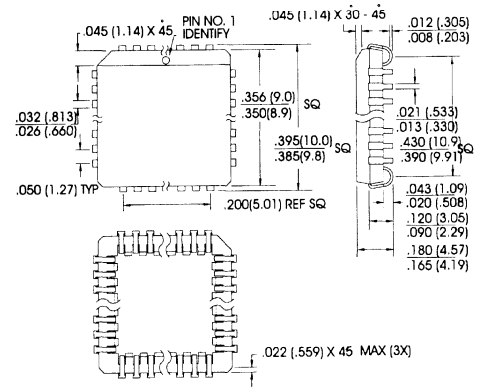
28J, 28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE M0-047 AB



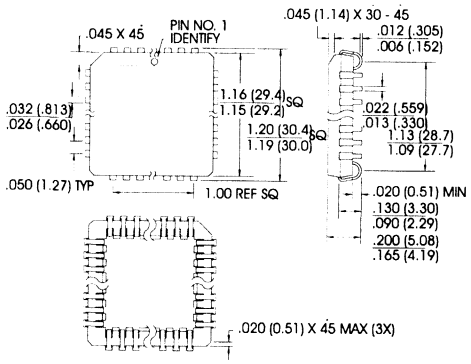
44J, 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AC



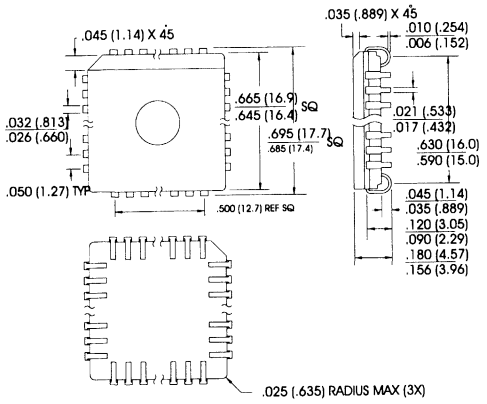
68J, 68 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-047 AE



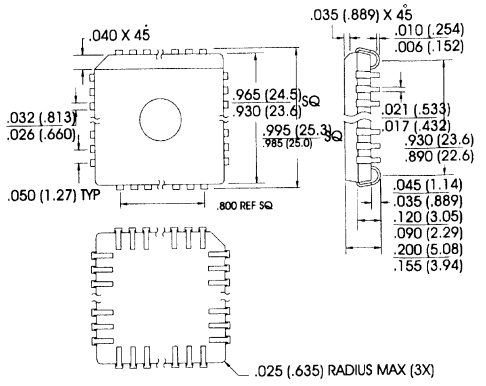
84J, 84 Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-47 AF



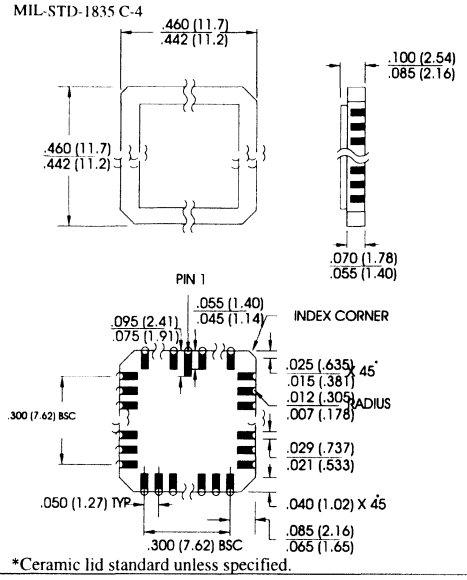
44KW, 44 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J1



68KW, 68 Lead, Windowed,
Ceramic J-Leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 C-J2
JEDEC OUTLINE MO-087 AD

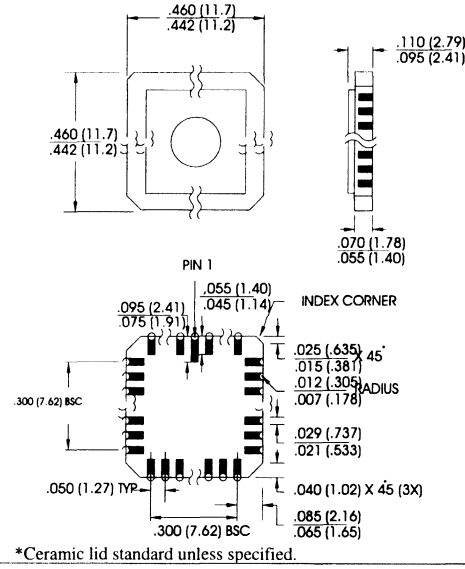


28L, 28 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



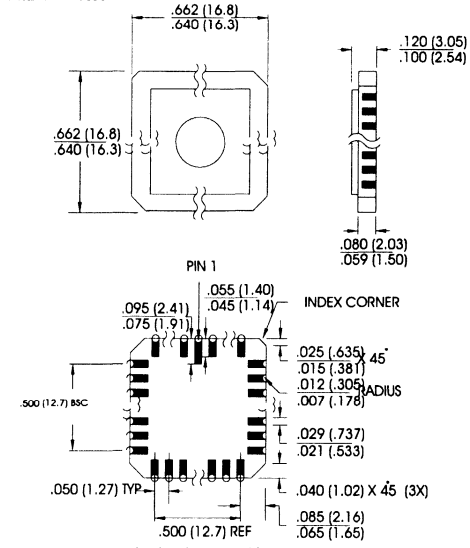
*Ceramic lid standard unless specified.

28LW, 28 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-4



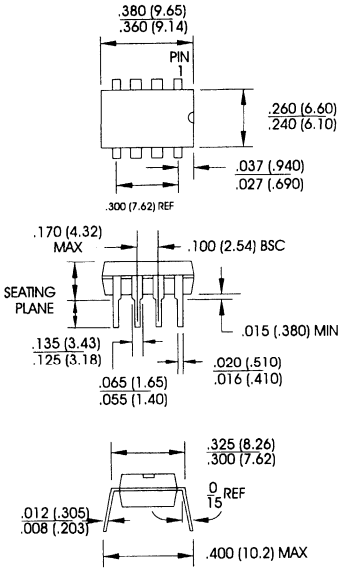
*Ceramic lid standard unless specified.

44LW, 44 Pad, Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5

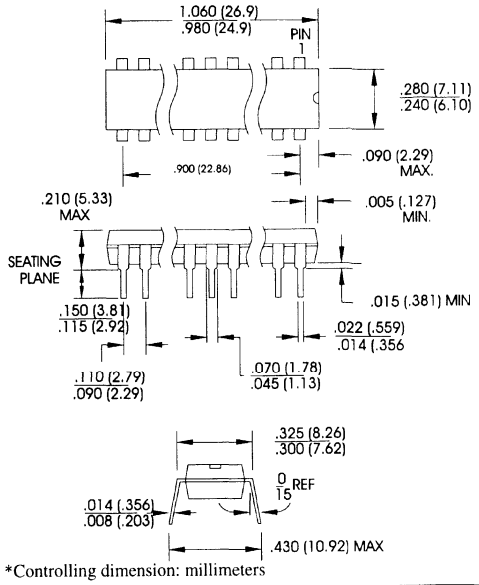


*Ceramic lid standard unless specified.

8P3, 8 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

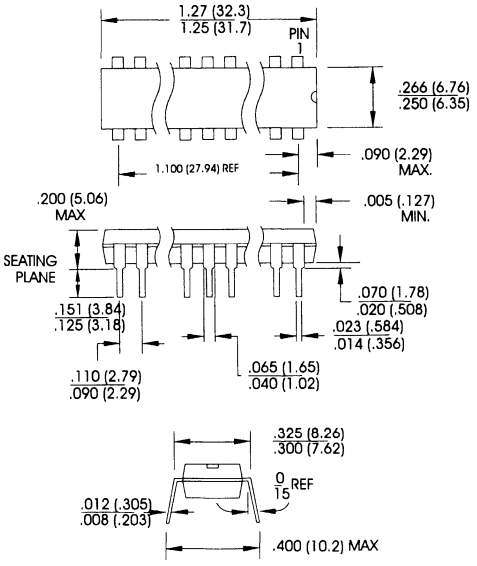


20P3, 20 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

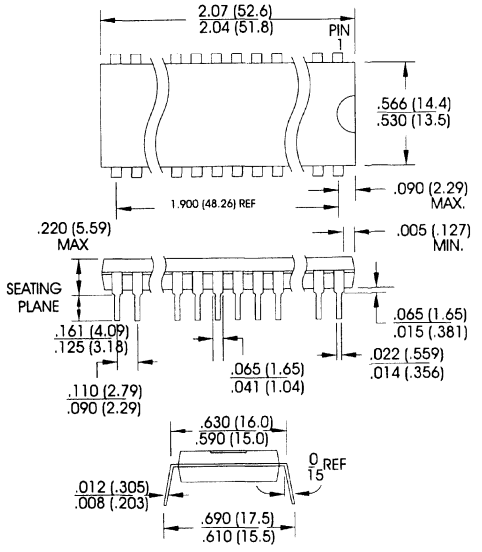


*Controlling dimension: millimeters

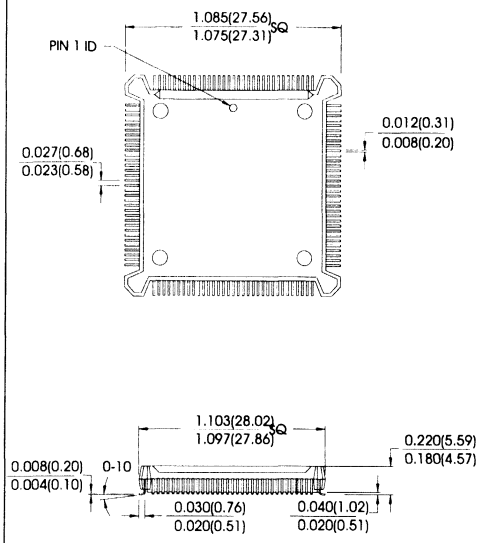
24P3, 24 Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



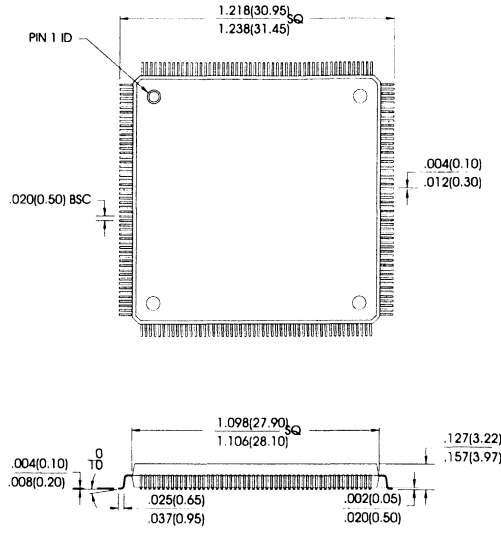
40P6, 40 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



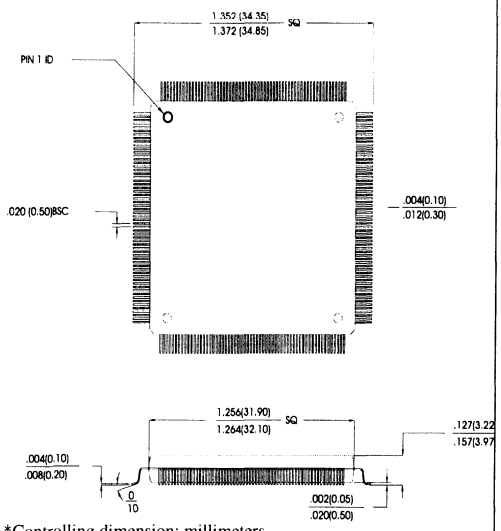
132Q, 132 Lead, Bumpered Plastic Gull Wing Quad Flat Package (BQFP)



208Q, 208 Lead, Plastic Gull Wing Quad Flat Package (PQFP)

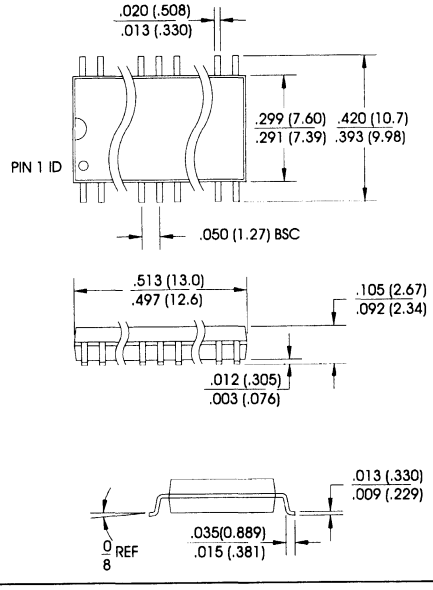


240Q, 240 Lead, Plastic Gull Wing Quad Flat package (PQFD)
Dimensions in Inches and (Millimeters)

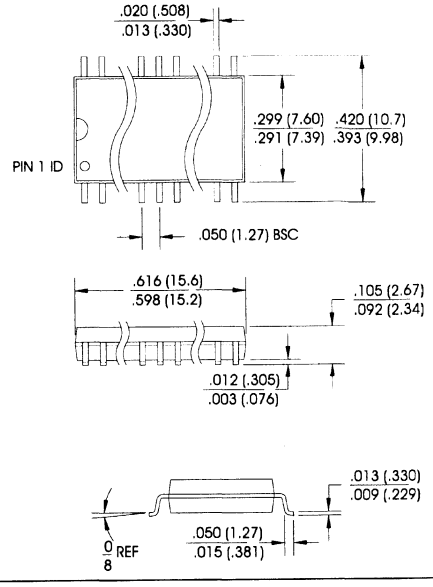


*Controlling dimension: millimeters

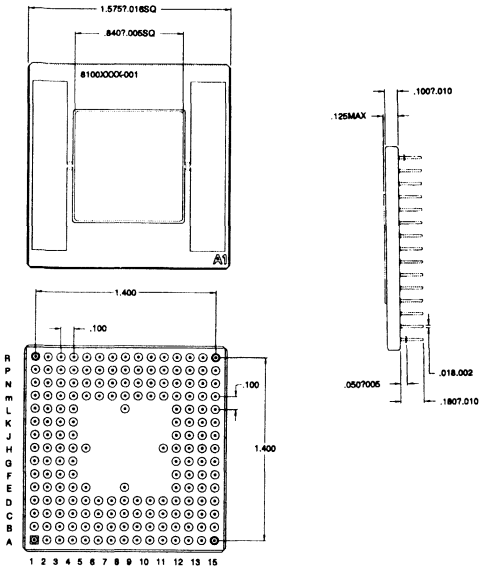
20S, 20 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



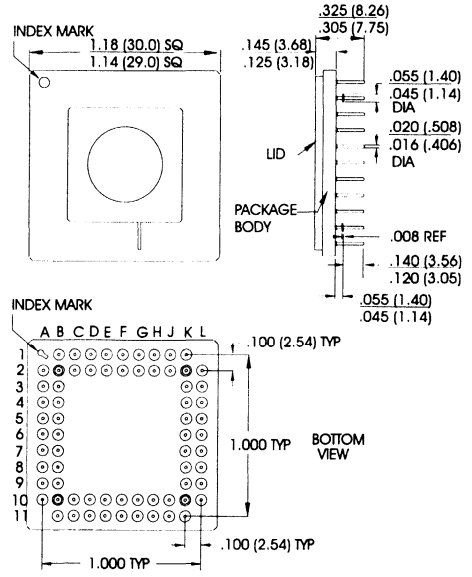
24S, 24 Lead, 0.300" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



180U, 180Pin, Ceramic Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



68UW, 68 Pin, Windowed, Ceramic
Pin Grid Array (PGA)
Dimensions in Inches and (Millimeters)



10

Thermal Characteristics of Atmel Packages

The thermal performance of the semiconductor package is a very important consideration for the board designer. The reliability and functional life of the device is directly related to its junction operating temperature. As the temperature of the device increases, the stability of its junctions decline, as does its reliable life. The thermal performance is also important to the board design, because it may limit the board density, or dictate the board location of high power-dissipating devices, or require expensive cooling methods for the system. As devices have become more complex and boards have become denser, the need to account for the thermal characteristics of packages has shifted from being a minor consideration to being a necessary consideration.

The thermal performance of a package is measured by its ability to dissipate the power required by the device into its surroundings. The electrical power drawn by the device generates heat on the top surface of the die. This heat is conducted through the package to the surface and then transferred to the surrounding air by convection. Each heat transfer step has a corresponding *resistance* to the heat flow, which is given the value θ, the thermal resistance coefficient. Subscripts are added to the coefficient to specify the two points that the heat is transferred between. Commonly used coefficients are θ_{JA} (junction to ambient air), θ_{JC} (junction to package case), and θ_{CA} (case to ambient air).

An electrical analogy can be made, as shown in the figure below, to illustrate the heat flow of a package. The heat transfer can be characterized mathematically by the following equation,

$$Tj - Ta = P \times \theta_{JA}$$

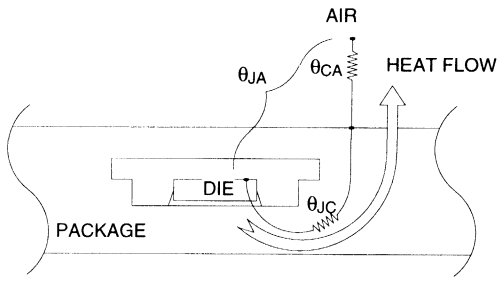
where,

P = Device operating power [watts]

Tj = Temperature of a junction on the device [°C]

Ta = Temperature of the surrounding ambient air [°C]

Two conclusions can be made after examining this analogy. First, the lower the value of θ_{JA}, the better the heat dissipation of the package. Secondly, the value of θ_{JA} is directly dependent upon both the conductive (θ_{JC}) and convective (θ_{CA}) properties of the package. θ_{JC} is a function of the package material, the adhesion between the package materials, and device size. θ_{CA} is a function of the package size and configuration, package mounting method, and air flow across



Thermal Characteristics of Atmel Packages (Continued)

the package. Lower θ_{JA} values can be achieved by specifying ceramic packages instead of plastic packages, choosing larger packages, or improving air flow across the package.

The thermal resistance values of Atmel standard packages are listed on the following page. The figures shown are maximum values for θ, typical values are lower dependent upon the device type.

Thermal Resistance Coefficients

		θ_{JC} [°C/W]	θ_{JA} [°C/W] Airflow = 0 ft/min
Ceramic DIP	24D3/DW3	9	65
	40DW6	7	40
Plastic DIP	24P3	22	82
	40P6	30	68
Leadless Chip Carrier (LCC)	28L/LW	12	68
	44LW	8-10	60
Plastic Leaded Chip Carrier (PLCC)	28J	16	60
	44J	14	50
	68J	10	45
J-Leaded Chip Carrier (JLCC)	28K/KW	16	72
	32K/KW	16	72
	44K/KW	16	68
	68KW	10-14	47
Ceramic Pin Grid Array (PGA)	68UW	4-6	30-40

Contents

System Serial Configuration E^2PROMS

Part Number	Memory Size	Description	Availability
AT34C64	65,536 x 1	64K System Configuration E^2PROM	3Q-95
AT34C128	131,072 x 1	128K System Configuration E^2PROM	3Q-95
AT34C256	262,144 x 1	256K System Configuration E^2PROM	4Q-95

Logic

Part Number	Speeds	Description	Availability
AT40281	16-40 MHz	80386SX PC/AT Core Logic Controller, with Posted-Write Cache	Now
AT40283	16-33 MHz	80386SX PC/AT Core Logic Controller	Now
AT40285	16-40 MHz	80386SX/486SLC/486SLC2 PC/AT Core Logic Controller	Now
AT40391B	25-40 MHz	80386DX PC/AT System & Cache Controller	Now
AT40392	25-50 MHz	80386DX PC/AT Memory Controller	Now
AT40410	25-50 MHz	ISA/PCI/VL PC/AT Core Logic Chipset	Now
AT40493	25-50 MHz	80486 PC/AT System & Cache Controller	Now
AT40495	25-50 MHz	80486 PC/AT System & Cache Controller	Now

Secure Memory ICs

Part Number	Memory Size	Description	Availability
AT88SC101	1024 x 1	1K Serial E^2PROM with Security, 1 Memory Zone, 1024 Bits	Now
AT88SC102	1024 x 1	1K Serial E^2PROM with Security, 2 Memory Zones, 512 Bits Each	Now
AT88SC103	1536 x 1	1K Serial E^2PROM with Security, 3 Memory Zones, 512 Bits Each	Now
AT88SC200	2048 x 1	2K Serial E^2PROM with Gate Array	Now
RF ID ASICs	Up to 16K x 1	Analog, Digital & Memory on Single-Chip ASIC	Now

Flash PEROMs

Part Number	Organization	Speeds	Description	Availability
Battery-Voltage™ **(2.7V to 3.6V)**				
AT29BV010A	128K x 8	200-350 ns	1-Mbit, 2.7-Volt Read and 2.7-Volt Write Flash PEROM	Now
AT29BV020	256K x 8	250-350 ns	2-Mbit, 2.7-Volt Read and 2.7-Volt Write Flash PEROM	Now
AT29BV040A	512K x 8	250-350 ns	4-Mbit, 2.7-Volt Read and 2.7-Volt Write Flash PEROM	Now
Low Voltage (3V to 3.6V)				
AT29LV256	32K x 8	150-250 ns	256K, 3-Volt Read and 3-Volt Write Flash PEROM	Now
AT29LV512	64K x 8	200-250 ns	512K, 3-Volt Read and 3-Volt Write Flash PEROM	Now
AT29LV010A	128K x 8	200-250 ns	1-Mbit, 3-Volt Read and 3-Volt Write Flash PEROM	Now
AT29LV1024	64K x 16	150-250 ns	1-Mbit, 3-Volt Read and 3-Volt Write Flash PEROM	Now
AT29LV020	256K x 8	200-250 ns	2-Mbit, 3-Volt Read and 3-Volt Write Flash PEROM	Now
AT29LV040A	512K x 8	200-250 ns	4-Mbit, 3-Volt Read and 3-Volt Write Flash PEROM	Now
Standard Voltage (5V)				
AT29C256	32K x 8	70-250 ns	256K, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C257	32K x 8	70-250 ns	256K, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C512	64K x 8	70-200 ns	512K, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C1024	64K x 16	70-200 ns	1-Mbit, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C010A	128K x 8	70-200 ns	1-Mbit, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C020	256K x 8	100-200 ns	2-Mbit, 5-Volt Read and 5-Volt Write Flash PEROM	Now
AT29C040A	512K x 8	120-250 ns	4-Mbit, 5-Volt Read and 5-Volt Write Flash PEROM	Now

Serial E^2PROMs

Part Number	Organization	V	Description	Availability
AT24C01	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 2-Wire Bus Serial E^2PROM, Non-Cascadable	Now
AT24C21	128 x 8	2.5 - 5.0 V	1K, 2-Wire Bus Serial E^2PROM, Dual Mode, Plug & Play Operation	Now
AT24C01A	128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 2-Wire Bus Serial E^2PROM	Now
AT24C02	256 x 8	1.8, 2.5, 2.7, 5.0 V	2K, 2-Wire Bus Serial E^2PROM	Now
AT24C04	512 x 8	1.8, 2.5, 2.7, 5.0 V	4K, 2-Wire Bus Serial E^2PROM	Now
AT24C08	1024 x 8	1.8, 2.5, 2.7, 5.0 V	8K, 2-Wire Bus Serial E^2PROM	Now
AT24C16	2048 x 8	1.8, 2.5, 2.7, 5.0 V	16K, 2-Wire Bus Serial E^2PROM	Now
AT24C164	2048 x 8	1.8, 2.5, 2.7, 5.0 V	16K, 2-Wire Bus Serial E^2PROM with Cascadable Feature	Now
AT24C32	4096 x 8	1.8, 2.5, 2.7, 5.0 V	32K, 2-Wire Bus Serial E^2PROM with Cascadable Feature	Now
AT24C64	8192 x 8	1.8, 2.5, 2.7, 5.0 V	64K, 2-Wire Bus Serial E^2PROM with Cascadable Feature	Now
AT25C01	128 x 8	1.8, 2.7, 5.0 V	1K, SPI Bus Serial E^2PROM, Supports SPI Mode 1	Consult Factory
AT25C02	256 x 8	1.8, 2.7, 5.0 V	2K, SPI Bus Serial E^2PROM, Supports SPI Mode 1	Consult Factory
AT25C04	512 x 8	1.8, 2.7, 5.0 V	4K, SPI Bus Serial E^2PROM, Supports SPI Mode 1	Consult Factory
AT25010	128 x 8	1.8, 2.7, 5.0 V	1K, SPI Bus Serial E^2PROM, Supports SPI Mode 0 and 3	3Q-95
AT25020	256 x 8	1.8, 2.7, 5.0 V	2K, SPI Bus Serial E^2PROM, Supports SPI Mode 0 and 3	3Q-95
AT25040	512 x 8	1.8, 2.7, 5.0 V	4K, SPI Bus Serial E^2PROM, Supports SPI Mode 0 and 3	3Q-95
AT93C46	64 x 16 / 128 x 8	1.8, 2.5, 2.7, 5.0 V	1K, 3-Wire Bus Serial E^2PROM	Now
AT93C46A	64 x 16	1.8, 2.5, 2.7, 5.0 V	1K, 3-Wire Bus Serial E^2PROM	Now
AT93C56	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 3-Wire Bus Serial E^2PROM	Now
AT93C57	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 3-Wire Bus Serial E^2PROM with Special Address	Now
AT93C66	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K, 3-Wire Bus Serial E^2PROM	Now
AT59C11	64 x 16 / 128 x 8	2.5, 2.7, 5.0 V	1K, 4-Wire Bus Serial E^2PROM	Now
AT59C22	128 x 16 / 256 x 8	2.5, 2.7, 5.0 V	2K, 4-Wire Bus Serial E^2PROM	Now
AT59C13	256 x 16 / 512 x 8	2.5, 2.7, 5.0 V	4K, 4-Wire Bus Serial E^2PROM	Now

Parallel E^2PROMs

Part Number	Organization	Speeds	Description	Availability
High Speed				
AT28HC64B	8K x 8	55-120 ns	64K E^2PROM with 64-Byte Page, Software Data Protection	Now
AT28HC256	32K x 8	70-120 ns	256K E^2PROM with 64-Byte Page & Software Data Protection	Now
AT28HC256E	32K x 8	70-120 ns	256K E^2PROM with Extended Endurance, Standard & Low Power	Now
AT28HC256F	32K x 8	70-120 ns	256K E^2PROM with Fast Write, Standard & Low Power	Now
Battery-Voltage™ **(2.7V to 3.6V)**				
AT28BV16	2K x 8	250-300 ns	16K E^2PROM, 2.7-Volt	Now
AT28BV64	8K x 8	300 ns	64K E^2PROM, 2.7-Volt	Now
Low Voltage (3.0V to 3.6V)				
AT28LV64B	8K x 8	200-300 ns	64K E^2PROM with 64-Byte Page & Software Data Protection, 3.0-Volt	Now
AT28LV256	32K x 8	200-300 ns	256K E^2PROM with 64-Byte Page & Software Data Protection, 3.0-Volt	Now
AT28LV010	128K x 8	200-250 ns	1-Mbit E^2PROM with 128-Byte Page & Software Data Protection, 3.0-Volt	Now
Standard Voltage (5V)				
AT28C16	2K x 8	150-250 ns	16K E^2PROM	Now
AT28C16E	2K x 8	150-250 ns	16K E^2PROM with Extended Endurance & Fast Write	Now
AT28C17	2K x 8	150-250 ns	16K E^2PROM with Ready/$\overline{\text{Busy}}$	Now
AT28C17E	2K x 8	150-250 ns	16K E^2PROM with Ready/$\overline{\text{Busy}}$ & Extended Endurance & Fast Write	Now
AT28C64	8K x 8	120-350 ns	64K E^2PROM	Now
AT28C64E	8K x 8	120-350 ns	64K E^2PROM with Extended Endurance & Fast Write	Now
AT28C64X	8K x 8	150-450 ns	64K E^2PROM without Ready-$\overline{\text{Busy}}$	Now
AT28C64B	8K x 8	150-250 ns	64K E^2PROM with 64-Byte Page & Software Data Protection	Now
AT28C256	32K x 8	150-350 ns	256K E^2PROM with 64-Byte Page & Software Data Protection	Now
AT28C256E	32K x 8	150-350 ns	256K E^2PROM with Extended Endurance	Now
AT28C256F	32K x 8	150-350 ns	256K E^2PROM with Fast Write & Software Data Protection	Now
AT28C010	128K x 8	120-250 ns	1-Mbit E^2PROM with 128-Byte Page & Software Data Protection	Now
AT28C010E	128K x 8	120-250 ns	1-Mbit E^2PROM with 128-Byte Page & Extended Endurance & Software Data Protection	Now
AT28C040	512K x 8	150-250 ns	4-Mbit E^2PROM with 256-Byte Page & Software Data Protection	Now

PROMs

Part Number	Organization	Speeds	Description	Availability
AT27HC641R	8K x 8	35-90 ns	High Speed 64K Reprogrammable [UV] PROM	Now
AT27HC642R	8K x 8	35-90 ns	High Speed 64K Reprogrammable [UV] PROM	Now

Flash Memory Card

Part Number	Organization	V	Description	Availability
AT5FC001	1 Mbyte	5.0 V	PCMCIA Compatible Flash Memory Card	Now
AT5FC002	2 Mbyte	5.0 V	PCMCIA Compatible Flash Memory Card	Now
AT5FC004	4 Mbyte	5.0 V	PCMCIA Compatible Flash Memory Card	Now
AT5FC008	8 Mbyte	5.0 V	PCMCIA Compatible Flash Memory Card	Now

EPROMs

Part Number	Organization	Speeds	Description	Availability
Battery-Voltage ™ **(2.7V)**				
AT27BV010	128K x 8	90-150 ns	1-Mbit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV020	256K x 8	120-150 ns	2-Mbit, 2.7-Volt to 3.6-Volt EPROM	Now
AT27BV040	512K x 8	150 ns	4-Mbit, 2.7-Volt to 3.6-Volt EPROM	Now
Low Voltage (3 to 5.5V)				
AT27LV256R	32K x 8	150-250 ns	256K 3-Volt EPROM	Now
AT27LV512R	64K x 8	150-250 ns	512K 3-Volt EPROM	Now
AT27LV1024	64K x 16	150-250 ns	1-Mbit, 3-Volt EPROM	Now
AT27LV010	128K x 8	150-250 ns	1-Mbit, 3-Volt EPROM	Now
AT27LV020	256K x 8	150-300 ns	2-Mbit, 3-Volt EPROM	Now
AT27LV4096	256K x 16	200-300 ns	4-Mbit, 3-Volt EPROM	Now
AT27LV040	512K x 8	200-300 ns	4-Mbit, 3-Volt EPROM	Now
AT27LV080	1024K x 8	250-300 ns	8-Mbit, 3-Volt EPROM	4Q-96
Standard Voltage (5V)				
AT27C256R	32K x 8	45-200 ns	256K EPROM	Now
AT27C512R	64K x 8	45-200 ns	512K EPROM	Now
AT27C1024	64K x 16	55-200 ns	1-Mbit EPROM	Now
AT27C010,L	128K x 8	45-200 ns	1-Mbit EPROM, Standard & Low Power	Now
AT27C020	256K x 8	70-200 ns	2-Mbit EPROM	Now
AT27C4096	256K x 16	85-200 ns	4-Mbit EPROM	Now
AT27C040	512K x 8	80-200 ns	4-Mbit EPROM	Now
AT27C080	1024K x 8	100-200 ns	8-Mbit EPROM	Now

Microcontroller

Part Number	Memory Size	Description	Availability
AT89C51	4K x 8	80C31 Microcontroller with 4 Kbytes Flash	Now
AT89LV51	4K x 8	2.7-Volt, 80C31 Microcontroller with 4 Kbytes Flash	Now
AT89C52	8K x 8	80C32 Microcontroller with 8 Kbytes Flash	Now
AT89LV52	8K x 8	2.7-Volt, 80C32 Microcontroller with 8 Kbytes Flash	Now
AT89C1051	1K x 8	2.7-Volt, 80C31 Microcontroller with 1 Kbytes Flash, 20-Pin Package	Now
AT89C2051	2K x 8	2.7-Volt, 80C31 Microcontroller with 2 Kbytes Flash, 20-Pin Package	Now

Mixed Signal

Part Number	Frequency	Description	Availability
AT76C176A	50-135 MHz	Triple 6-Bit Color Palette DAC with Power-Down	Now

Atmel Sales Offices

North American Sales Offices

NORTHEAST

300 Granite Street, Suite 106
Braintree, MA 02184
TEL (617) 849-0220
FAX (617) 848-0012

135 Michael Cowpland Dr.
Suite 203
Kanata, Ontario K2M 2E9
Canada
TEL (613) 599-5338
FAX (613) 599-5337

MID-ATLANTIC

101 Carnegie Center
Suite 205
Princeton, NJ 08540
TEL (609) 520-0606
FAX (609) 520-9175

SOUTHEAST

809 Spring Forest Road, Suite 600
Raleigh, NC 27609
TEL (919) 850-9889
FAX (919) 850-9894

NORTH CENTRAL

1721 Moon Lake Blvd., Suite 430
Hoffman Estates, IL 60194
TEL (708) 310-1200
FAX (708) 310-1650

SOUTH CENTRAL

11782 Jollyville Rd.
Austin, TX 78759
TEL(512)219-4050
FAX(512)219-4051

17304 Preston Road, Suite 720
Dallas, TX 75252
TEL (214) 733-3366
FAX (214) 733-3163

NORTHWEST

2125 O'Nel Drive
San Jose, CA 95131
TEL (408) 436-4270
FAX (408) 436-4314

SOUTHWEST

8101 Kaiser, Suite 140
Anaheim Hills, CA 92808
TEL (714) 282-8080
FAX (714) 282-0500

International Sales Offices

UNITED KINGDOM

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

FINLAND

Atmel OY
Sinikalliontie 5
02630 Espoo
Finland
TEL (358) 0-5023026
FAX (358) 0-5023126

FRANCE

Atmel Southern Europe
55 Avenue Diderot
94100 St. Maur Des Fosses
Paris, France
TEL (33) 1-48855522
FAX (33) 1-48855596

GERMANY

Atmel GmbH
Ginnheimer Strasse 45
60487 Frankfurt 90
Germany
TEL (49) 69-7075910
FAX (49) 69-7075912

Atmel GmbH
Niederlassung Sud
Litzdorfer Strasse 11
D83064 Raubling
Germany
TEL (49) 8066-8592
FAX (49) 8066-8489

HONG KONG

Atmel Asia, Ltd.
Room 1219, Chinachem Golden Plaza
77 Mody Road, Tsimshatsui East
Kowloon
Hong Kong
TEL (852) 27219778
FAX (852) 27221369

ITALY

Ufficio di Milano
Centro Direzionale Colleoni
Palazzo Andromeda 3
20041 Agrate Brianza
Italy
TEL (39) 39 605 69 55
FAX (39) 39 605 69 69

JAPAN

Atmel Japan K.K.
Thomas Bldg., 16-1
Nihonbashi Hakosaki-Cho
Chuo-Ku, Tokyo 103
Japan
TEL (81) 3-5641-0211
FAX (81) 3-5641-0217

KOREA

Atmel Korea, Ltd.
Room 1509, Gurosunkyoung Officetel
106-4, 7 Guro 5-Dong
Guro-Gu
Seoul, Korea
TEL (82) 2-8396341
FAX (82) 2-8396343

SINGAPORE

Atmel Singapore PTE., Ltd.
6001 Beach Road
Golden Mile Tower #21-01
Singapore 0719
TEL (65) 2999-212
FAX (65) 2910-955

SWEDEN

Atmel Sweden
P.O. Box 142
S-19422 Upplands Vasby
Sweden
TEL (46) 8-590-74910
FAX(46) 8-590-74910

TAIWAN

Atmel Taiwan Ltd.
FL 15-4, No. 83, Sec. 1
Nan-Kan Road
Lu Chu Hsiang, Taoyuan Hsien
Taiwan, R.O.C.
TEL (886) 3-3229133
FAX (886) 3-3229131

North American Distributors

Alabama

ALL AMERICAN SEMICONDUCTOR
4900 University Square
Suite 34
Huntsville, AL 35816
TEL (205) 837-1555
FAX (205) 837-7733

INSIGHT ELECTRONICS
4835 University Square
Suite 19
Huntsville, AL 35818
TEL (205) 830-1222
FAX (205) 830-1225

MARSHALL INDUSTRIES
3313 Memorial Parkway South
Huntsville, AL 35801
TEL (205) 881-9235
FAX (205) 881-1490

MILGRAY/HUNTSVILLE
5021 Bradford Drive
Suite 202
Huntsville, AL 35805
TEL (205) 722-9709
FAX (205) 722-0161

NU HORIZONS
4801 University Square
Suite 11
Huntsville, AL 35816
TEL (205) 722-9330
FAX (205) 722-9348

PIONEER STANDARD ELECTRONICS
4835 University Square
Suite 5
Huntsville, AL 35816
TEL (205) 837-9300
FAX (205) 837-9358

Arizona

INSIGHT ELECTRONICS
1515 West University
Suite 103
Tempe, AZ 85281
TEL (602) 829-1800
FAX (602) 967-2658

MARSHALL INDUSTRIES
9831 S. 51st Street
Suite C107-109
Phoenix, AZ 85044
TEL (602) 496-0290
FAX (602) 893-9029

PIONEER STANDARD ELECTRONICS
1438 West Broadway
Suite B-140
Tempe, AZ 85282
TEL (602) 350-9335
FAX (602) 350-9376

California

ALL AMERICAN SEMICONDUCTOR
230 Devcon Drive
San Jose, CA 95112
TEL (408) 441-1300
FAX (408) 437-8970

26010 Mureau Road, # 120
Calabasas, CA 91302
TEL (818) 878-0555
FAX (818) 878-0533

10805 Holder Street, Suite 100
Cypress, CA 90630
TEL (714) 229-8600
FAX (714) 229-8603

5060 Shoreham Place, Suite 115
San Diego, CA 92122
TEL (800) 382-3441
FAX (619) 458-5866

31225 LaBaya Drive, Suite 113
Westlake Village, CA 91362
TEL (818) 706-1775
FAX (818) 706-1871

INSIGHT ELECTRONICS
4333 Park Terrace Drive
Westlake Village, CA 91316
TEL (818) 707-2101
FAX (818) 707-0321

2 Venture Plaza, Suite 340
Irvine, CA 92718
TEL (714) 727-3291
FAX (714) 727-1804

9980 Huennekens Street
San Diego, CA 92121
TEL (619) 587-1100
FAX (619) 587-1380

1295 Oakmead Parkway
Sunnyvale, CA 94086
TEL (408) 720-9222
FAX (408) 720-8390

JAN DEVICES
6925 Canby Avenue, Building 109
Reseda, CA 91335
TEL (818) 757-2000
FAX (818) 708-7436

MARSHALL INDUSTRIES
9320 Telstar Avenue
El Monte, CA 91731
TEL (818) 307-6000
FAX (818) 307-6173

3039 Kilgore Avenue
Rancho Cordova, CA 95670
TEL (916) 635-9700
FAX (916) 635-6044

336 Los Coches Street
Milpitas, CA 95035
TEL (408) 942-4600
FAX (408) 262-1224

One Morgan
Irvine, CA 92718
TEL (714) 859-5050
FAX (714) 581-5255

26537 Agoura Road
Calabasas, CA 91302
TEL (818) 878-7000
FAX (818) 880-6846

5961 Kearny Villa
San Diego, CA 92123
TEL (619) 627-4184
FAX (619) 627-4163

MILGRAY ELECTRONICS, INC.
2880 Zanker Road, Suite 102
San Jose, CA 95134
TEL (408) 456-0900
FAX (408) 456-0300

275 E. Hillcrest Dr., Suite 145
Thousand Oaks, CA 91360
TEL (805) 371-9399
FAX (805) 371-9317

MILGRAY/ORANGE COUNTY
25 Mauchly, Suite 329
Irvine, CA 92718
TEL (714) 753-1282
FAX (714) 753-1682

6835 Flanders Drive, Suite 300
San Diego, CA 92121
TEL (619) 457-7545
FAX (619) 457-9750

PIONEER STANDARD ELECTRONICS
5126 Clareton Drive, Suite 160
Agoura Hills, CA 91301
TEL (818) 865-5800
FAX (818) 865-5814

217 Technology Drive
Suite 110
Irvine, CA 92718
TEL (714) 753-5090
FAX (714) 753-5074

333 River Oaks Pkwy
San Jose, CA 95134
TEL (408) 954-9100
FAX (408) 954-9113

Colorado

INSIGHT ELECTRONICS

384 Inverness Drive South
Suite 105
Englewood, CO 80112
TEL (303) 649-1800
FAX (303) 649-1818

MARSHALL INDUSTRIES

12351 North Grant
Thornton, CO 80241
TEL (303) 451-8383
FAX (303) 457-2899

MILGRAY/COLORADO

5650 D T C Parkway
Suite 202
Englewood, CO 80111
TEL (303) 721-7702
FAX (303) 721-7803

Connecticut

MARSHALL INDUSTRIES

20 Sterling Drive
Barnes Industrial Park North
P.O. Box 200
Wallingford, CT 06492-0200
TEL (203) 265-3822
FAX (203) 284-9285

MILGRAY/CONNECTICUT

326 West Main Street
Milford, CT 06460
TEL (203) 878-5538
FAX (203) 878-6970

PIONEER STANDARD ELECTRONICS

Two Trap Falls
Shelton, CT 06484
TEL (203) 929-5600
FAX (203) 929-9791

Florida

ALL AMERICAN SEMICONDUCTOR

16115 N.W. 52nd Avenue
Miami, FL 33014
TEL (305) 621-8282
FAX (305) 620-7831

14450 46th Street
Shelter 116
Clearwater, FL 34622
TEL (813) 532-9800
FAX (813) 538-5567

1400 East Newport Center Drive
Suite 205
Deerfield Beach, FL 33442
TEL (305) 429-2800
FAX (305) 429-0391

MARSHALL INDUSTRIES

2700 W. Cypress Creek Road
Suite D114
Ft. Lauderdale, FL 33309
TEL (305) 977-4880
FAX (305) 977-4887

380 S. Northlake Boulevard
Suite 1024
Altamonte Springs, FL 32701
TEL (407) 767-8585
FAX (407) 767-8676

2840 Scherer Drive, Suite 410
St. Petersburg, FL 33716
TEL (813) 573-1399
FAX (813) 573-0069

MILGRAY/FLORIDA

755 Rinehart Road, Suite 100
Lake Mary, FL 32746
TEL (407) 321-2555
FAX (407) 322-4225

NU HORIZONS

3421 N.W. 55th Street
Fort Lauderdale, FL 33309
TEL (305) 735-2555
FAX (305) 735-2880

600 S. Northlake Boulevard
Suite 270
Altamonte Springs, FL 32701
TEL (407) 831-8008
FAX (407) 831-8862

PIONEER STANDARD ELECTRONICS

674 S. Military Trail
Deerfield Beach, FL 33442
TEL (305) 428-8877
FAX (305) 481-2950

337 S. Northlake Boulevard
Suite 1000
Altamonte Springs, FL 32701
TEL (407) 834-9090
FAX (407) 834-0865

Georgia

INSIGHT ELECTRONICS

3005 Breckinridge Blvd.
Suite 201A
Duluth, GA 30138
TEL (404) 717-8566
FAX (404) 717-8588

MARSHALL INDUSTRIES

5300 Oakbrook Parkway
Suite 140
Norcross, GA 30093
TEL (404) 923-5750
FAX (404) 923-2743

MILGRAY/ATLANTA

3000 Northwoods Parkway
Suite 115
Norcross, GA 30071
TEL (404) 446-9777
FAX (404) 446-1186

NU HORIZONS

5555 Oakbrook Parkway
Suite 340
Norcross, GA 30093
TEL (404) 416-8666
FAX (404) 416-9060

PIONEER STANDARD ELECTRONICS

4250C Rivergreen Parkway
Duluth, GA 30136
TEL (404) 623-1003
FAX (404) 623-0665

Illinois

INSIGHT ELECTRONICS

1365 Wiley Road
Suite 142
Schaumburg, IL 60173
TEL (708) 885-9700
FAX (708) 885-9701

MARSHALL INDUSTRIES

50 East Commerce Drive, Unit 1
Schaumburg, IL 60173
TEL (708) 490-0155
FAX (708) 490-0569

MILGRAY/CHICAGO

Kennedy Corporate Center 1
1530 E. Dundee Road, Suite 310
Palatine, IL 60067-8319
TEL (708) 202-1900
FAX (708) 202-1985

PIONEER STANDARD ELECTRONICS

2171 Executive Drive
Suite 200
Addison, IL 60101
TEL (708) 495-9680
FAX (708) 495-9831

Indiana

MARSHALL INDUSTRIES

6990 Corporate Drive
Indianapolis, IN 46278
TEL (317) 297-0483
FAX (317) 297-2787

MILGRAY/INDIANA

5226 Elmwood Avenue
Indianapolis, IN 46203
TEL (317) 781-9997
FAX (317) 781-6970

North American Distributors

PIONEER STANDARD ELECTRONICS
9350 N. Priority Way, W. Drive
Indianapolis, IN 46240
TEL (317) 573-0880
FAX (317) 573-0979

Kansas

MARSHALL INDUSTRIES
10413 West 84th Terrace
Pine Ridge Business Park
Lenexa, KS 68214
TEL (913) 492-3121
FAX (913) 492-6205

MILGRAY/KANSAS CITY
6400 Glenwood, Suite 313
Overland Park, KS 66202
TEL (913) 236-8800
FAX (913) 384-6825

Maryland

ALL AMERICAN
14636 Rothged Drive
Rockville, MD 20850
TEL (800) 426-0420
FAX (301) 251-8574

MARSHALL INDUSTRIES
9130B Guilford Road
Columbia, MD 21046-1803
TEL (301) 470-2800
FAX (301) 622-0451

MILGRAY/WASHINGTON
6460 Dobbin Road, Suite D
Columbia, MD 21045
TEL (410) 730-6119
FAX (410) 730-8940

NU HORIZONS
8975 Guilford Road, Suite 120
Columbia, MD 21046
TEL (410) 995-6330
FAX (410) 995-6332

PIONEER STANDARD ELECTRONICS
9100 Gaither Road
Gaithersburg, MD 20877
TEL (301) 921-0660
FAX (301) 921-4255

15810 Gaither Road
Gaithersburg, MD 20877
TEL (301) 921-3822
FAX (301) 921-3858

Massachusetts

MARSHALL INDUSTRIES
33 Upton Drive
Wilmington, MA 01887
TEL (508) 658-0810
FAX (508) 658-7608

MILGRAY/NEW ENGLAND
Ballardvale Park
187 Ballardvale Street
Wilmington, MA 01887
TEL (508) 657-5900
FAX (508) 658-7989

NU HORIZONS
107 Audubon Road
Wakefield, MA 01880
TEL (617) 246-4442
FAX (617) 246-4462

PIONEER STANDARD ELECTRONICS
44 Hartwell Avenue
Lexington, MA 02173
TEL (617) 861-9200
FAX (617) 863-1547

Michigan

MARSHALL INDUSTRIES
31067 Schoolcraft
Livonia, MI 48150
TEL (313) 525-5850
FAX (313) 525-5855

PIONEER STANDARD ELECTRONICS
4467 Byron Center Avenue
Wyoming, MI 49509
TEL (616) 534-6074
FAX (616) 534-3922

44190 Plymouth Oaks Drive
Plymouth, MI 48270
TEL (313) 416-2157
FAX (313) 416-2415

Minnesota

ALL AMERICAN SEMICONDUCTOR
7716 Golden Triangle Drive
Eden Prairie, MN 55344
TEL (612) 944-2151
FAX (612) 944-9803

INSIGHT ELECTRONICS
5353 Gamble Drive
Suite 330
St. Louis Park, MN 55416
TEL (612) 525-9999
FAX (612) 525-9998

MARSHALL INDUSTRIES
14800 28th Avenue, North
Suite 175
Minneapolis, MN 55447
TEL (612) 559-2211
FAX (612) 559-8321

PIONEER STANDARD ELECTRONICS
7625 Golden Triangle
Eden Prairie, MN 56344
TEL (612) 944-3355
FAX (612) 944-3794

Missouri

MARSHALL INDUSTRIES
514 Earthcity Expressway
Suite 131
Earthcity, MO 63045
TEL (314) 770-1749
FAX (314) 770-1486

PIONEER STANDARD ELECTRONICS
111 West Port Plaza
Suite 625
St. Louis, MO 63146
TEL (314) 542-3077
FAX (314) 542-3078

New Jersey

MARSHALL INDUSTRIES
101 Fairfield Road
Fairfield, NJ 07004
TEL (201) 882-0320
FAX (201) 882-0095

158 Gaither Drive
Mt. Laurel, NJ 08054
TEL (609) 234-9100
FAX (609) 778-1819

MILGRAY/DELAWARE VALLEY
523 Fellowship Road
Suite 275
Mt. Laurel, NJ 08054
TEL (609) 778-1300
FAX (609) 778-7669

MILGRAY/NEW JERSEY
3799 Route 46 East
Suite 303
Parsippany, NJ 07054
TEL (201) 335-1766
FAX (201) 335-2110

NU HORIZONS
39 U.S. Route 46
Pine Brook, NJ 07058
TEL (201) 882-8300
FAX (201) 882-8398

1800 Horizon Way, Suite 200
Mt. Laurel, NJ 08054
TEL (609) 231-0900
FAX (609) 231-9510

PIONEER STANDARD ELECTRONICS
14A Madison Road
Fairfield, NJ 07006
TEL (201) 575-3510
FAX (201) 575-3454

New York

ALL AMERICAN SEMICONDUCTOR

275B Marcus Boulevard
Hauppauge, NY 11788
TEL (516) 981-3935
FAX (516) 434-9394

MARSHALL INDUSTRIES

100 Marshall Drive
Endicott, NY 13760
TEL (607) 785-2345
FAX (607) 785-5546

1250 Scottsville Road
Rochester, NY 14624
TEL (716) 235-7620
FAX (716) 235-0052

3505 Veterans Memorial Highway
Suite L.
Ronkonkoma, NY 11779
TEL (516) 737-9300
FAX (516) 737 9580

MILGRAY/NEW YORK

77 Schmitt Boulevard
Farmingdale, NY 11735
TEL (516) 391-3000
FAX (516) 420-0685

MILGRAY/UPSTATE NEW YORK

One Corporate Place, Suite 200
1170 Pittsford Victor Road
Pittsford, NY 14534
TEL (716) 381-9700
FAX (716) 381-9495

NU HORIZONS

6000 New Horizons Boulevard
Amityville, NY 11701
TEL (516) 226-6000
FAX (516) 226-5886

333 Metro Park
E. Rochester, NY 14623
TEL (716) 292-0777
FAX (716) 292-0750

PIONEER STANDARD ELECTRONICS

1249 Upper Front, Suite 201
Binghamton, NY 13901
TEL (607) 722-9300
FAX (607) 722-9562

840 Fairport Park
Fairport, NY 14450
TEL (716) 381-7070
FAX (716) 381-5955

One Penn Plaza #2032
New York, NY 10119
TEL (212) 631-4700
FAX (212) 971-0374

60 Crossways Park West
Woodbury, NY 11797
TEL (516) 921-8700
FAX (516) 921-2143

North Carolina

MARSHALL INDUSTRIES

5224 Greens Dairy Road
Raleigh, NC 27604
TEL (919) 878-9882
FAX (919) 872-2431

MILGRAY/RALEIGH

2925 Huntleigh Drive
Suite 101
Raleigh, NC 27604
TEL (919) 790-8094
FAX (919) 872-8851

PIONEER STANDARD ELECTRONICS

2200 Gateway Center Blvd.
Suite 215
Morrisville, NC 27560
TEL (919) 460-1530
FAX (919) 460-1540

Ohio

INSIGHT ELECTRONICS

9700 Rockside Road
Suite 105
Valley View, OH 44125
TEL (216) 487-2522
FAX (216) 487-3412

MARSHALL INDUSTRIES

30700 Bainbridge Road, Unit A
Solon, OH 44139
TEL (216) 248-1788
FAX (216) 248-2312

3520 Park Center Drive
Dayton, OH 45414
TEL (513) 898-4480
FAX (513) 898-9363

MILGRAY/CLEVELAND

6155 Rockside Road, Suite 206
Cleveland, OH 44131
TEL (216) 447-1520
FAX (216) 447-1761

NU HORIZONS/OHIO

6200 Som Center Road
Suite A-15
Solon, OH 44139
TEL (216) 349-2008
FAX (216) 349-2080

PIONEER STANDARD ELECTRONICS

2385 Edison Blvd.
Twinsburg, OH 44087
TEL (216) 487-5500
FAX (216) 487-0256

4800 East 131st Street
Cleveland, OH 44105
TEL (216) 587-3600
FAX (216) 587-3906

4433 Interpoint Boulevard
Dayton, OH 45424
TEL (513) 236-9900
FAX (513) 236-8133

100 Old Wilson Bridge Road
Suite 105
Worthington, OH 43085
TEL (614) 848-4854
FAX (614) 848-4889

Oklahoma

PIONEER STANDARD ELECTRONICS

9717 E. 42nd Street, Suite 105
Tulsa, OK 74146
TEL (918) 665-7840
FAX (918) 665-1891

Oregon

ALL AMERICAN/PORTLAND

1815 N.W. 169th Place
Suite 6025
Beaverton, OR 97006
TEL (800) 531-3334
FAX (503) 531-3695

INSIGHT ELECTRONICS

8705 S.W. Nimbus Avenue
Suite 200
Beaverton, OR 97005
TEL (503) 644-3300
FAX (503) 641-4530

MARSHALL INDUSTRIES

9705 S.W. Gemini Drive
Beaverton, OR 97005
TEL (503) 644-5050
FAX (503) 646-8256

MILGRAY/OREGON

8705 S.W. Nimbus Ave., Suite 260
Beaverton, OR 97008
TEL (503) 626-4040
FAX (503) 641-0650

Pennsylvania

PIONEER STANDARD ELECTRONICS

500 Enterprise Road
Horsham, PA 19044
TEL (215) 674-4000
FAX (215) 674-3107

259 Kappa Drive
Pittsburgh, PA 15238
TEL (412) 782-2300
FAX (412) 963-8255

North American Distributors

Texas

ALL AMERICAN SEMICONDUCTOR
11210 Steeplecrest, Suite 206
Houston, TX 77065
TEL (713) 955-1993
FAX (713) 955-2215

ALL AMERICAN/DALLAS
1771 International Parkway
Suite 101
Richardson, TX 75081
TEL (800) 541-1435
FAX (214) 437-0353

AMIGA SALES & MARKETING C/O JAN DEVICES
12342 Hunters Chase Blvd.
Suite 3127
Austin, TX 78729
TEL (818) 757-2005
FAX (818) 708-7436

INSIGHT ELECTRONICS, INC.
1778 Plano Road, Suite 320
Richardson, TX 75081
TEL (214) 783-0800
FAX (214) 680-2402

11500 Metric Boulevard
Suite 215
Austin, TX 78758
TEL (512) 719-3090
FAX (512) 719-3091

MARSHALL INDUSTRIES
8504 Cross Park Drive
Austin, TX 79764
TEL (512) 837-1991
FAX (512) 832-9810

Corporate Square Tech
Center III
1551 North Glenville Drive
Richardson, TX 75081
TEL (214) 705-0600
FAX (214) 705-0675

10681 Haddington Drive
Suite 160
Houston, TX 77043
TEL (713) 467-1666
FAX (713) 467-9805

MILGRAY/AUSTIN
11824 Jollyville Road
Suite 103
Austin, TX 78759
TEL (512) 331-9961
FAX (512) 331-1070

MILGRAY/DALLAS
16610 North Dallas Parkway
Suite 1300
Dallas, TX 75248
TEL (214) 248-1603
FAX (214) 248-0218

MILGRAY/HOUSTON
12919 S.W. Freeway, Suite 130
Stafford, TX 77477
TEL (713) 240-5360
FAX (713) 240-5404

NU HORIZONS
2081 Hutton Drive
Suite 119
Carrollton, TX 75006
TEL (214) 488-2255
FAX (214) 488-2265

PIONEER STANDARD ELECTRONICS
1826-D Kramer Lane
Austin, TX 78758
TEL (512) 835-4000
FAX (512) 835-9829

13765 Beta Road
Dallas, TX 75244
TEL (214) 386-7300
FAX (214) 490-6419

10530 Rockley Road
Houston, TX 77099
TEL (713) 495-4700
FAX (713) 495-5642

8200 Interstate 10 West
Suite 705
San Antonio, TX 78230
TEL (512) 377-3440
FAX (512) 378-3626

Utah

ALL AMERICAN/UTAH
4455 South 700 East
Suite 301
Salt Lake City, UT 84107
TEL (800) 682-8313
FAX (801) 261-3885

MARSHALL INDUSTRIES
2355 S. 1070 West, Suite D
Salt Lake City, UT 84119
TEL (801) 973-2288
FAX (801) 973-2296

MILGRAY/UTAH
310 E. 4500 South, Suite 110
Murray, UT 84107
TEL (801) 261-2999
FAX (801) 261-0880

Washington

INSIGHT ELECTRONICS
12002 115th Avenue N.E.
Kirkland, WA 98034
TEL (206) 820-8100
FAX (206) 821-2976

MARSHALL INDUSTRIES
11715 N. Creek Parkway South
Suite 112
Bothell, WA 98011
TEL (206) 466-5747
FAX (206) 486-6964

PIONEER STANDARD ELECTRONICS
2800 156th Avenue SE, Suite 100
Bellevue, WA 98007
TEL (206) 644-7500
FAX (206) 644-7300

Wisconsin

INSIGHT ELECTRONICS
10855 West Potter Road
Suite 14
Wauwatosa, WI 53222
TEL (414) 258-5338
FAX (414) 258-5360

MARSHALL INDUSTRIES
Crossroads Corporate Center 1
20900 Swenson Drive, Suite 150
Waukesha, WI 53186
TEL (414) 797-8400
FAX (414) 797-8270

PIONEER STANDARD ELECTRONICS
120 Bishops Way, Suite 163
Brookfield, WI 53005
TEL (414) 784-3480
FAX (414) 784-8207

Canada

FARNELL ELECTRONIC SERVICES
300 North Rivermede Road
Concord, Ontario L4K 2Z4
Canada
TEL (905) 738-1071
FAX (905) 738-4183

39 Robertson Road
Suite 506 Bell Mews
Nepean, Ontario K2H 8R2
Canada
TEL (613) 596-6980
FAX (613) 596-6987

6600 Trans Canada Hwy
6th Floor, Suite 620
Pointe Claire, Quebec H9R 4S2
Canada
TEL (514) 697-8149
FAX (514) 697-1210

8525 Baxter Place
Unit 101, Production Court
Burnaby, B.C., V5A 4V7
Canada
TEL (604) 421-6222
FAX (604) 421-0582

3015 5th Avenue N.E., Suite 210
Calgary, Alberta T2A 6T8
Canada
TEL (403) 273-2780
FAX (403) 273-7458

MARSHALL INDUSTRIES

148 Brunswick Boulevard
Pointe Claire, Quebec H9R 5P9
Canada
TEL (514) 694-8142
FAX (514) 694-6989

6285 Northam Dr.
Mississauga, Ontario L4V 1X5
Canada
TEL (905) 465-1771
FAX (905) 612-1988

MILGRAY/TORONTO

2783 Thamesgate Drive
Mississauga, Ontario L4T 1G5
Canada
TEL (905) 678-0958
FAX (905) 678-1213

MILGRAY/MONTREAL

6600 Trans Canada, Suite 209
Pointe Claire, Quebec H9R-4S2
Canada
TEL (514) 426-5900
FAX (514) 426-5836

PIONEER STANDARD ELECTRONICS

560 1212-31 Avenue NE
Calgary, Alberta T2E 7S8
Canada
TEL (403) 291-1988
FAX (403) 291-0740

Plaza 124.708 10216-124 Street
Edmonton, Alberta T5N 4A3
Canada
TEL (403) 482-3038
FAX (403) 482-1336

148 York Street, Suite 209
London, Ontario N6A 1A9
Canada
TEL (519) 672-4666
FAX (519) 672-3528

3415 American Drive
Mississauga, Ontario L4V 1T6
Canada
TEL (905) 405-8300
FAX (905) 405-6425

223 Colonnade Road, Unit 12
Nepean, Ontario K2E 7K3
Canada
TEL (613) 226-8840
FAX (613) 226-6352

4455 #6 Road
Richmond, B. C. V6V 1P8
Canada
TEL (604) 273-5575
FAX (604) 273-2413

Place Iberville IV
2954 Blvd. Laurier, Suite 100
Ste-Foy, Quebec G1V 4T2
Canada
TEL (418) 654-1077
FAX (418) 654-2958

520 McCaffrey Street
Ville St. Laurent, Quebec H4T 1N1
Canada
TEL (514) 737-9700
FAX (514) 737-5212

808-240 Graham Avenue
Winnipeg, Manitoba R3C 0J7
Canada
TEL (204) 989-1957
FAX (204) 633-9255

North American Representatives

Alabama

ELECTRONIC MARKETING ASSOC.

7501 S. Memorial Parkway
Suite 106
Huntsville, AL 35802
TEL (205) 880-8050
FAX (205) 880-8054

Arizona

COMPASS MARKETING

11801 North Tatum Boulevard
Suite 101
Phoenix, AZ 85028
TEL (602) 996-0635
FAX (602) 996-0586

California

PROMERGE SALES, INC.

100 Century Center Court
Suite 710
San Jose, CA 95112
TEL (408) 467-0600
FAX (408) 467-0610

PROLINE TECHNOLOGIES

P.O. Box 1326
Healdsburg, CA 95448
TEL (707) 431-2937
FAX (707) 431-1809

HARPER & STRONG

2798 Junipero Avenue
Signal Hill, CA 90806
TEL (310) 424-3030
FAX (310) 424-6622

SILICON TECHNICAL SALES, INC.

140 Lomas Santa Fe Drive
Suite 102A
Solana Beach, CA 92075
TEL (619) 793-3330
FAX (619) 793-4188

Colorado

THORSON ROCKY MOUNTAIN

7108 D South Alton Way, Suite A
Englewood, CO 80112
TEL (303) 773-6300
FAX (303) 773-6302

Connecticut

DELTA-CONN TECHNICAL SALES

One Prestige Drive, 2nd Floor
Suite 206
Meriden, CT 06450
TEL (203) 634-8558
FAX (203) 238-1240

Florida

COMPONENT DESIGN MARKETING

800 Corporate Drive, Suite 230
Ft. Lauderdale, FL 33334
TEL (305) 492-1160
FAX (305) 492-1167

1900 S.W. 85th Avenue
North Lauderdale, FL 33068
TEL (305) 726-5444
FAX (305) 726-5155

2318 Stag Run Boulevard
Clearwater, FL 34625
TEL (813) 725-4894
FAX (813) 796-7252

7616 Southland Boulevard
Suite 103
Orlando, FL 32809
TEL (407) 240-3903
FAX (407) 240-4305

4502 West Elm Street
Tampa, FL 33614
TEL (813) 886-9721
FAX (813) 888-7816

Calle Hucar 38 (Bajos)
BO Sabanetas
Mercedita 00715
Puerto Rico
TEL (809) 844-3840
FAX (809) 844-3915

Georgia

ELECTRONIC MARKETING ASSOC.

5855 Jimmy Carter Blvd.
Suite 190
Norcross, GA 30071
TEL (404) 448-1215
FAX (404) 446-9363

Iowa

DY-TRONIX, INC.

23 Twixt Town Road N.E.
Cedar Rapids, IA 52402
TEL (319) 377-8275
FAX (319) 377-9163

Illinois

PHASE II MARKETING

2220 Hicks Road, Suite 206
Rolling Meadows, IL 60008
TEL (708) 577-9401
FAX (708) 577-9491

Indiana

CORRAO MARSH, INC.

6211 Stoney Creek Drive
Fort Wayne, IN 46825
TEL (219) 482-2725
FAX (219) 484-7491

3063 West U.S. 40
Greenfield, IN 46140
TEL (317) 462-4446
FAX (317) 462-6568

Kansas

DY-TRONIX, INC.

5001 College Boulevard, Suite 106
Leawood, KS 66211
TEL (913) 339-6333
FAX (913) 339-9449

1999 Amidon, Suite 322
Wichita, KS 67203
TEL (316) 838-0884
FAX (316) 838-2645

Maryland

AVTEK ASSOCIATES, INC.

9030 Red Branch Road, Suite 220
Columbia, MD 21045
TEL (410) 740-5100
FAX (410) 740-5103

Massachusetts

CTC ASSOCIATES, INC.

12 Southwest Park
Westwood, MA 02090
TEL (617) 320-1818
FAX (617) 320-8282

Michigan

TRILOGY MARKETING, INC.

691 N. Squirrel Road, Suite 110
Auburn Hills, MI 48326
TEL (810) 377-4900
FAX (810) 377-4906

Minnesota

PSI

8000 Town Line Avenue S.
Suite 206
Bloomington, MN 55438
TEL (612) 944-8545
FAX (612) 944-6249

Missouri

DY-TRONIX, INC.

3407 Bridgeland Drive
Bridgeton, MO 63044
TEL (314) 291-4777
FAX (314) 291-3861

Nevada

PROLINE TECHNOLOGIES

P.O. Box 1326
Healdsburg, CA 95448
TEL (707) 431-2937
FAX (707) 431-1809

New Jersey

NORTH EAST COMPONENTS

19 Spear Road, Suite 205
Ramsey, NJ 07446
TEL (201) 825-0233
FAX (201) 934-1310

TRITEK SALES, INC.

1 Mall Drive, Suite 410
Cherry Hill, NJ 08002
TEL (609) 667-0200
FAX (609) 667-8741

New Mexico

COMPASS MARKETING

4100 Osuna Road, Suite 109
Albuquerque, NM 87109
TEL (505) 344-9990
FAX (505) 345-4848

New York

EMPIRE TECHNICAL ASSOC.

29 Fennell Street, Suite A
Skaneateles, NY 13152
TEL (315) 685-5703
FAX (315) 685-5979

349 West Commercial Street
Suite 2920
E. Rochester, NY 14445
TEL (716) 381-8500
FAX (716) 381-0911

North Carolina

ELECTRONIC MARKETING ASSOC.

6600 Six Forks Road, Suite 201
Raleigh, NC 27615
TEL (919) 847-8800
FAX (919) 848-1787

9407 King Falls Dr.
Charlotte, NC 28210
TEL (704) 544-9948
FAX (704) 544-9941

Ohio

CENTURY TECHNICAL SALES, INC.

8977 Columbia Rd.
Suite G
Cincinnati, OH 45140
TEL (513) 677-5088
FAX (513) 677-1775

6610 Busch Blvd.
Suite 250
Columbus, OH 43229
TEL (614) 433-7500
FAX (614) 433-9085

24610 Detroit Rd.
Suite 170
Westlake, OH 44145
TEL (216) 899-0071
FAX (216) 899-1072

Oklahoma

QUAD STATE SALES
& MARKETING

110 W. Commercial Street
Suite 210
Broken Arrow, OK 74013
TEL (918) 258-7723
FAX (918) 258-7653

Oregon

ELECTRONIC SOURCES, INC.

6850 SW 105th, Suite B
Beaverton, OR 97008
TEL (503) 627-0838
FAX (503) 627-0238

Pennsylvania

CENTURY TECHNICAL
SALES, INC.

130 Spang Road
Baden, PA 15005
TEL (412) 934-2326
FAX (412) 934-3031

TRITEK SALES, INC.

1 Mall Drive, Suite 410
Cherry Hill, NJ 08002
TEL (609) 667-0200
FAX (609) 667-8741

Texas

QUAD STATE SALES
& MARKETING

8310 Capital of Texas Hwy, North
Suite 365
Austin, TX 78731
TEL (512) 346-7002
FAX (512) 346-3601

12160 Abrams Road, Suite 406
Dallas, TX 75243
TEL (214) 669-8567
FAX (214) 669-8834

10565 Katy Fwy, Suite 212
Houston, TX 77024
TEL (713) 467-7749
FAX (713) 467-5942

Utah

THORSON ROCKY MOUNTAIN

5505 South 900 East
Suite 140
Salt Lake City, UT 84117
TEL (801) 264-9665
FAX (801) 264-9881

Washington

ELECTRONIC SOURCES, INC.

1603 116th Ave, N.E., Suite 115
Bellevue, WA 98004
TEL (206) 451-3500
FAX (206) 451-1038

Wisconsin

PHASE II MARKETING

11040 W. Bluemound Road
Suite 211
Wauwatosa, WI 53226
TEL (414) 771-9986
FAX (414) 771-9935

Canada

CLARK-HURMAN ASSOCIATES

78 Donegani , Suite 200
Pointe Claire, Quebec H9R 2V4
Canada
TEL (514) 426-0453
FAX (514) 426-0455

308 Palladium Drive, Suite 200
Kanata, Ontario K2V 1A1
Canada
TEL (613) 599-5626
FAX (613) 599-5707

20 Regan Road, Unit 14
Brampton, Ontario L7A 1C3
Canada
TEL (905) 840-6066
FAX (905) 840-6091

International Representatives

Australia

GEC ELECTRONICS DIVISION

38 South Street
Rydalmere, N.S.W. 2116
Australia
TEL (61) 2898-7422
FAX (61) 2638-1798

Austria

CODICO

Muhlgasse 86-88
A-2380
Perchtoldsdorf/A
Austria
TEL (43) 1-863-3050
FAX (43) 1-863-0598

INELTEK, GES. MB

Franzensbruckenstr. 3/33
A-1020 Wien
Austria
TEL (43) 1-272-0984
FAX (43) 1-212-0987

Belgium

ALCOM ELECTRONICS BV

Singel 3
2550 Kontich
Belgium
TEL (32) 3-4583033
FAX (32) 3-4583126

Brazil

COLGIL, INC.

Rua Marques de Itu, 306, Conj. 94
CEP 01223-000
Sao Paulo
Brazil
TEL (55) 11-223-6954
FAX (55) 11-223-4989

Headquarters
New York
United States
TEL (212) 832-1340
FAX (212) 826-3623

Tucuman 1567, Officina 14
Buenos Aires
Argentina
TEL (54) 1-46-2128
FAX (54) 1-46-2128

HASTEC

Rua Ferreira Do Alentecj, 90/92
CEP 04728
Sao Paulo
Brazil
TEL (55) 11-522-1799
FAX (55) 11-522-5366

Bulgaria

CODICO

AP 9
5500 Lovetsch
Bulgaria 86
TEL (3592) 68-44812
FAX (3592) 68-44812

Denmark

MER-EL A/S

Ved Klaedebo 18
Post Boks 219
DK-2970 Horsholm
Denmark
TEL (45) 42-571000
FAX (45) 42-572299

Finland

OY BEXAB FINN-CRIMP AB

P.O. Box 51
SF-02631 Espoo
Finland
TEL (358) 0-61352690
FAX (358) 0-61352655

France

MICRO PUISSANCE

Immeuble Femto
1 Avenue de Norvege
Z.A. de Courtaboeuf B.P. 79
91943 Les Ulis Cedex
France
TEL (33) 1-69071211
FAX (33) 1-69076712

NEWTEK

8 Rue De L'Estrerel
Silic 583
94663 Rungis Cedex
France
TEL (33) 1-46872200
FAX (33) 1-46878049

Germany

INELTEK GMBH

Hauptstrasse 45
89522 Heidenhiem
Germany
TEL (49) 7321-93850
FAX (49) 7321-938595

INELTEK MITTE

Stehnweg 2
63500 Seligenstadt
Germany
TEL (49) 6182-5066
FAX (49) 6182-65953

INELTEK MURNAU

Am Fugsee 21
82418 Murnau-Riedhausen
Germany
TEL (49) 8841-47775
FAX (49) 8841-2660

INELTEK NORD

Billstrasse 30
20539 Hamburg 26
Germany
TEL (49) 78942-274
FAX (49) 78942-220

Greece

MICRELEC LTD.

339 Thivon Street
GR 12244 Aegaleo
Athens, Greece
TEL (30) 1-5395042-4
FAX (30) 1-5390269

Hong Kong

TLG ELECTRONICS, LTD.

Room 1404, Hang Shing Bldg.
363-373, Nathan Road
Yanumatei, Kowloon
Hong Kong
TEL (852) 388-7613
FAX (852) 783-0198

WES TECH ELECTRONICS, LTD.

Room 1601, Star Centre
433-451, Castle Peak Road
Kwai Chung, N.T.
Hong Kong
TEL (852) 418-9818
FAX (852) 429-2355

Hungary

CODICO KFT

Ostrom Utca 23-25
1015 Budapest
TEL (36) 1-156-63-30
FAX (36) 1-156-43-76

India

ORIOLE SERVICES
Post Box No. 9275
5 Kurla Industrial Estate
Ghatkopar, Bombay 400 086
India
TEL (022) 5119940
FAX (022) 5115810

Ireland

ZEC SERVICES

Valleymount
Blessington
Co. Wicklow
Ireland
TEL (353) 456-4259
FAX (353) 467-4075

Israel

ISAMTEK LTD.

53 Herzel Street
P.O. Box 13902
Netanya 42-137
Israel
TEL (972) 9-826445
FAX (972) 9-826447

Italy

LASI ELETTRONICA S.P.A.

Viale Fulvio Testi 280
20126 Milano
Italy
TEL (39) 2-66101370
FAX (39) 2-66101385

NEWTEK ITALIA SPA

Via Tonoli 1
20145 Milano
Italy
TEL (39) 2-33105308
FAX (39) 2-33103694

Japan

MCM JAPAN LTD.

Santower Bldg.
2-11-22, Sangenjyaya
Setagaya-Ku, Tokyo 154
Japan
TEL (81) 3-3487-8477
FAX (81) 3-3487-8825

Tama Sales Office
Tachikawa Center Bldg.
2-22-20, Akebono Cho
Tachikawa
Tokyo 190
Japan
TEL (81) 425-22-8600
FAX (81) 425-23-8603

TAKACHIHO KOHEKI CO., LTD.

1-2-8, Yotsuya
Shinjuku-Ku
Tokyo 160
Japan
TEL (81) 3-3355-6695
FAX (81) 3-3357-5034

Fukoku Seimei Bldg.
2-4, Komatsubara-Cho
Kita-Ku, Osaka 530
Japan
TEL (81) 6-313-0671
FAX (81) 6-313-3380

RYOYO ELECTRO CORP.

Konwa Bldg., 1-12-22
Tsukiji, Chuo-Ku
Tokyo 104
Japan
TEL (81) 3-3546-5011
FAX (81) 3-3546-5044

Osaka Branch
Nissin Syokuhin Bldg., 4-1-1
Nishi Nakajima, Yodogawa-ku
Osaka 532
Japan
TEL (81) 6-301-1221
FAX (81) 6-302-1002

UNI ELECTRONICS, INC.

P.O. Box 68, S umitomo Bldg.
2-6-1 Nishi Shinjukn
Shinjuku-ku
Tokyo 163
Japan
TEL (81) 3-3347-8878
FAX (81) 3-3347-8808

Osaka Branch
5-13-9, Mitejima
Nishi Yodogawa-ku
Osaka 555
Japan
TEL (81) 6-473-8429
FAX (81) 6-473-5513

Korea

D & S CORPORATION

Room 1412, A-Dong
Champs Elysees Center
889-5, Daechi-Dong, Kangnam-Gu
Seoul 135-280
Korea
TEL (82) 2-5388431
FAX (82) 2-5682008

I & C MICROSYSTEMS CO. LTD

3rd Floor, Jungnam Building
191-3 Poi-Dong, Kangnam-Ku
Seoul, Korea
TEL (82) 2-577-9131
FAX (82) 2-577-9130

PAL BOK CO LTD.

Young Jin Building
16-18, Hangangro
Yong San-ku
Seoul, Korea
TEL (82) 2-703-8561
FAX (82) 2-703-8550

SHINHWA CORPORATION

2F, The Christian Literature,
Society of Korea Bldg.
169-1, Samsung-Dong,
Kangnam-Ku
Seoul, Korea
TEL (82) 2-554-6431
FAX (82) 2-554-7649

UNIQUEST KOREA

Suite 1110 Daejong Bldg.
143-48, Samsung-Dong,
Kangnam-Gu
Seoul, Korea
TEL (82) 2-562-8805
FAX (82) 2-562-6646

Mexico

ADELSA

Club Cuicacalli #66
CTO Cronistas
Zona Azul CD Satelite
Naucalpan De Juarez
C.P. 53100 EDO de Mexico
Mexico
TEL (525) 374-0981
FAX (525) 374-0997

Netherlands

ALCOM ELECTRONICS BV

Essebaan 1
2908 LG Capelle Aan Den Yssel
Netherlands
TEL (31) 10-4519533
FAX (31)10-4586482

New Zealand

APEX ELECTRONICS LTD.

175 Vivian Street
Wellington, New Zealand
TEL (64) 4-3853404
FAX (64) 4-3853483

GEC ELECTRONICS

5 Reliable Way
Penrose Auckland
New Zealand
TEL (64) 9-526-0107
FAX (64) 9-525-7923

Norway

NC NORDCOMP AS

PO Box 190
2020 Skedsmokorset
Norway
TEL (47) 63-879330
FAX (47) 63-879000

Poland

CODICO

Ul Bora Komorowskiego 6/17
86-300 Grudziadz
Poland
TEL (48) 51-23223
FAX (48) 51-23223

Portugal

ANATRONIC-PORTUGAL S.A.

Rua Padre Antonio Vieira, No 31-B
Povoa De Santo Adriao - 2675 Odivelas
Portugal
TEL (351) 1-9376267
FAX (351) 1-9371834

Romania

CODICO

BD Decebal NR 11 BLS 14
SC 2, Apt. 41, Sect. 3
Bucharest
TEL (40) 1-3210431
FAX (40) 1-3210431

Singapore

NUCLEUS ELECTRONICS PTE LTD.

5001 Beach Road #18-03
Golden Mile Tower
Singapore 0719
TEL (65)297-6883
FAX (65) 297-6882

SINGASOF COMPUTERS PTE., LTD.

2 Kallang Pudding Road #09-04
Mactech Industrial Bldg.
Singapore 1334
TEL (65) 747-3012
FAX (65) 747-5279

South Africa

ADVANCED SEMICONDUCTOR DEVICES (PTY), LTD.

P.O. Box 3853
Rivonia 2128
South Africa
TEL (27) 11-444-2333
FAX (27) 11-444-1706

Spain

ANATRONIC S.A.

AVDA. De Valladolid, 27
28008 Madrid
Spain
TEL (34) 1-542-44-55
FAX (34) 1-559-69-75

Bailen, 176. Entresuelo 1º
08037 Barcelona
Spain
TEL (34) 3-458-19-06
FAX (34) 3-458-71-28

Las Mercedes 25 3º Dpto. 1
48930 Las Arenas-Vizcaya
Spain
TEL (34) 4-463-60-66
FAX (34) 4-463-42-35

Sweden

KELTECH COMPONENTS AB

Box 505 Kemistvagen 10 A
S-183 25
Taby
Sweden
TEL (46) 86308590
FAX (46) 87562143

Switzerland

ANATEC AG

Sumpfstrasse 7
CH 6300
ZUG
Switzerland
TEL (41) 42-412441
FAX (41) 42-413124

Taiwan

ALLREACH ENTERPRISE CO., LTD.

6F, No. 50-1, Sec. 1
Hsin Sheng South Road
Taipei, Taiwan
R.O.C.
TEL (886) 2-321-4229
FAX (886) 2-321-5849

APPLIED COMPONENT TECHNOLOGY CORP.

8F, No. 233-1 Pao Chiao Road
Hsin Tien City
Taipei Hsien
Taiwan, R.O.C.
TEL (886) 2-917-0858
FAX (886) 2-917-1895

NEOLEC INTERNATIONAL INC.

3F, Jen Jen Bldg
No. 29, Jen Ai Road, Sec. 3,
Taipei 106
Taiwan, R.O.C.
TEL (886) 2-778-8716
FAX (886) 2-778-6076

PRINCETON TECHNOLOGY CORP.

2F, No. 233-1, Bao Chiao Road
Hsin Tien, Taipei Hsien
Taiwan, R.O.C.
TEL (886) 2-917-8856
FAX (886) 2-917-3836

TOPTREND TECHNOLOGIES CORP.

8F, No. 669, Sec. 5
Chung Hsiao East Road
Taipei, Taiwan
R.O.C.
TEL (886) 2-769-6220
FAX (886) 2-769-6228

Thailand

SEMIKON COMPANY, LTD.

4F, Room 406, Phansak Bldg.
Phetburi Road
Rajthevee, Bangkok, 10400
Thailand
TEL (662) 215-0760
FAX (662) 215-6857

Turkey

AZTECH ELECTRONIK, LTD.

Kaptanpasa Sok No. 25/2
06700 G.O.P.
Ankara, Turkey
TEL (90) 312-447-0384
FAX (90) 312-447-0387

United Kingdom

GD TECHNIK, LTD.

Tudor House
24 High Street
Twyford, Berks RG10 9AG
England
TEL (44) 734-342277
FAX (44) 734-342896

PRONTO ELECTRONIC SYSTEMS, LTD.

City Gate House
399-425 Eastern Ave.
Gants Hill
Ilford, Essex I92 6LR
England
TEL (44) 81-554-6222
FAX (44) 81-518-3222